

**HB0870 Handbook**  
**CoreUHD\_SDITX v2.0**



---

a  **MICROCHIP** company



a  MICROCHIP company

**Microsemi Headquarters**

One Enterprise, Aliso Viejo,  
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Sales: +1 (949) 380-6136

Fax: +1 (949) 215-4996

Email: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

[www.microsemi.com](http://www.microsemi.com)

©2019 Microsemi, a wholly owned subsidiary of Microchip Technology Inc. All rights reserved. Microsemi and the Microsemi logo are registered trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

**About Microsemi**

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at [www.microsemi.com](http://www.microsemi.com).

# Contents

---

1	Revision History	1
1.1	Revision 1.0	1
2	Introduction	2
2.1	Overview	2
2.2	Features	2
2.3	Core Version	2
2.4	Supported Families	2
2.5	Device Utilization and Performance	2
3	Interface	3
3.1	Configuration Parameters	3
3.2	Ports	3
4	Functional Description	6
4.1	Stream Detect Block	7
4.2	Stream Control Block	7
4.3	Line Number Insertion Block	7
4.4	VPID Insertion Block	7
4.5	CRC Generation Block	8
4.6	CRC Insertion Block	8
4.7	Sync Bits Insertion Block	8
4.8	Channel Encoder Block	8
5	Timing Diagrams	9
5.1	Type1 Multiplex Data Stream	9
5.2	Type2 Multiplex Data Stream	9
6	Tool Flow	10
6.1	License	10
6.2	Using core in Libero SmartDesign	10
6.3	Simulation Flows	12
6.4	Synthesis in Libero	12
6.5	Place-and-Route in Libero	12
7	Testbench	13
8	System Integration	14
9	References	16

# Figures

---

Figure 1	CoreUHD_SDITX Block Diagram in 6G-SDI Mode .....	6
Figure 2	CoreUHD_SDITX Block Diagram in 12G-SDI Mode .....	7
Figure 3	Timing Diagram for Type1 10-bit Multiplex Data Stream .....	9
Figure 4	Timing Diagram for Type2 10-bit Multiplex Data Stream .....	9
Figure 5	Core Instance Full I/O View in SmartDesign .....	11
Figure 6	Configuring the Core in SmartDesign .....	12
Figure 7	User Testbench .....	13
Figure 8	System Integration .....	15

# Tables

---

Table 1	Device Utilization and Performance .....	2
Table 2	Parameter/Generic Descriptions .....	3
Table 3	Input and Output Signals .....	3

# 1 Revision History

---

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

This is the first publication of this document.

## 2 Introduction

### 2.1 Overview

CoreUHD\_SDITX DirectCore IP is a Serial Digital Interface (SDI) Framer. Core supports 6 Gigabits per second SDI (6G-SDI) and 12 Gigabits per second SDI (12G-SDI) SDI standards defined by the Society of Motion Picture and Television Engineers (SMPTE).

### 2.2 Features

Core has the following features:

- Compliant with SMPTE ST 2081-1 (6G-SDI) standard.
- Compliant with SMPTE ST 2082-1 (12G-SDI) standard.
- Supports data rates 5.94 Gb/s and 5.94/1.001 Gb/s for 6G-SDI standard.
- Supports data rates 11.88 Gb/s and 11.88/1.001 Gb/s for 12G-SDI standard.
- Performs generation and insertion of Line Number (LN) packets.
- Performs generation and insertion of CRC packets.
- Performs generation and insertion of Video Payload Identification (VPID) packets.
- Performs insertion of sync-bits in timing reference words.
- Performs scrambling and NRZI encoding.

### 2.3 Core Version

This handbook is for CoreUHD\_SDITX version 2.0.

### 2.4 Supported Families

- PolarFire®

### 2.5 Device Utilization and Performance

Device Utilization and Performance data is provided in [Table 1](#) for the supported device families. The data described in this table is only indicative. The overall device utilization and performance of the core is system dependent.

**Table 1 • Device Utilization and Performance**

Family (Device)	Configuration Parameters		Utilization (Logic Elements)				Performance (MHz)
	TX_SDI_STD	TX_SDI_DW	Sequential (DFF)	Combinatorial (4LUT)	Total	%	TX_CLK Frequency
PolarFire (MPF300T)	4	40	942	1482	2424	0.40	187
	5	80	1718	3074	4792	0.80	186

**Note:** The data in this table is achieved using typical synthesis and layout settings. Frequency (MHz) was set to 148.5 and the speed grade was -1.

## 3 Interface

### 3.1 Configuration Parameters

The following table describes the configurable parameter/generic of the Core. All the parameters/generics are integer types.

**Table 2 • Parameter/Generic Descriptions**

Parameter Name	Valid Range	Default	Description
TX_SDI_STD	4, 5	5	<b>SDI STANDARD</b> Configure the core for required SDI standard. <ul style="list-style-type: none"> <li>4 – 6G-SDI</li> <li>5 – 12G-SDI</li> </ul>
TX_SDI_DW	40, 80	80	<b>SDI DATA WIDTH</b> Configure the data width of the parallel SDI data stream on the transceiver interface of the core. <ul style="list-style-type: none"> <li>40 – Select 40-bits in 6G-SDI mode (when TX_SDI_STD parameter is set to 4)</li> <li>80 – Select 80-bits in 12G-SDI mode (when TX_SDI_STD parameter is set to 5)</li> </ul>

### 3.2 Ports

All the input and output ports of the core are listed in the table below.

**Table 3 • Input and Output Signals**

Port	Width	Direction	Description
<b>Clock and Reset</b>			
TX_CLK	1	Input	Transmit clock input. All input signals are required to be clocked on rising edge to this clock. All the output signals are clocked on rising edge of this clock. Recommended to connect to LANEx_TX_CLK of Transceiver. The required clock frequency is <b>148.5 (1.001) MHz</b> in both 6G-SDI mode and 12G-SDI mode.
TX_RESETN	1	Input	Active low asynchronous reset input. The reset input is required to be synchronous to clock TX_CLK.
<b>Transceiver Interface</b>			
TX_SDI_DATA	TX_SDI_DW	Output	Transmit data to Transceiver. SDI data stream output. Recommended to connect to LANEx_TX_DATA of Transceiver.
TX_CLK_STABLE	1	Input	Transmit Clock Stable from the Transceiver. The core resets whenever TX_CLK_STABLE is not asserted. Recommended to connect to LANEx_TX_CLK_STABLE of Transceiver.
<b>Data Stream Inputs</b>			
TX_DATA_DS1	10	Input	Data Stream 1 input. DS1 in 12G-SDI and 6G-SDI modes.
TX_DATA_DS2	10	Input	Data Stream 2 input. DS2 in 12G-SDI and 6G-SDI modes.
TX_DATA_DS3	10	Input	Data Stream 3 input. DS3 in 12G-SDI and 6G-SDI modes.



**Table 3 • Input and Output Signals (continued)**

Port	Width	Direction	Description
TX_DATA_DS4	10	Input	Data Stream 4 input. DS4 in 12G-SDI and 6G-SDI modes.
TX_DATA_DS5	10	Input	Data Stream 5 input. DS5 in 12G-SDI mode.
TX_DATA_DS6	10	Input	Data Stream 6 input. DS6 in 12G-SDI mode.
TX_DATA_DS7	10	Input	Data Stream 7 input. DS7 in 12G-SDI mode.
TX_DATA_DS8	10	Input	Data Stream 8 input. DS8 in 12G-SDI mode.
<b>Line Number Inputs</b>			
TX_LN_DS1	11	Input	Line number to be inserted in DS1 data stream.
TX_LN_DS2	11	Input	Line number to be inserted in DS2 data stream.
TX_LN_DS3	11	Input	Line number to be inserted in DS3 data stream.
TX_LN_DS4	11	Input	Line number to be inserted in DS4 data stream.
TX_LN_DS5	11	Input	Line number to be inserted in DS5 data stream.
TX_LN_DS6	11	Input	Line number to be inserted in DS6 data stream.
TX_LN_DS7	11	Input	Line number to be inserted in DS7 data stream.
TX_LN_DS8	11	Input	Line number to be inserted in DS8 data stream.
<b>VPID Data Inputs</b>			
TX_VPID_DS1	32	Input	VPID data bytes to be inserted in DS1 data stream.
TX_VPID_DS2	32	Input	VPID data bytes to be inserted in DS2 data stream.
TX_VPID_DS3	32	Input	VPID data bytes to be inserted in DS3 data stream.
TX_VPID_DS4	32	Input	VPID data bytes to be inserted in DS4 data stream.
TX_VPID_DS5	32	Input	VPID data bytes to be inserted in DS5 data stream.
TX_VPID_DS6	32	Input	VPID data bytes to be inserted in DS6 data stream.
TX_VPID_DS7	32	Input	VPID data bytes to be inserted in DS7 data stream.
TX_VPID_DS8	32	Input	VPID data bytes to be inserted in DS8 data stream.
<b>VPID Line Number Inputs</b>			
TX_VPID_LN_DS1	11	Input	Line number for VPID insertion in DS1 data stream.
TX_VPID_LN_DS2	11	Input	Line number for VPID insertion in DS2 data stream.
TX_VPID_LN_DS3	11	Input	Line number for VPID insertion in DS3 data stream.
TX_VPID_LN_DS4	11	Input	Line number for VPID insertion in DS4 data stream.
TX_VPID_LN_DS5	11	Input	Line number for VPID insertion in DS5 data stream.
TX_VPID_LN_DS6	11	Input	Line number for VPID insertion in DS6 data stream.
TX_VPID_LN_DS7	11	Input	Line number for VPID insertion in DS7 data stream.
TX_VPID_LN_DS8	11	Input	Line number for VPID insertion in DS8 data stream.
<b>Control Inputs</b>			

**Table 3 • Input and Output Signals (continued)**

Port	Width	Direction	Description
TX_INSERT_LN	1	Input	Input to enable or disable line number insertion in the data stream. When high, core inserts line number (LN) packets in each data stream, generated from line number data provided on the line number input port of the respective data stream. When low, line number packets are not inserted in SDI data stream, instead data available on the data stream is retained. This input must remain high for the complete duration of the line for which the LN packet insertion is required.
TX_INSERT_CRC	1	Input	Input to enable or disable CRC insertion in the data stream. When high, core inserts CRC packets in each data stream, generated from the data input of respective data streams. When low, CRC packets are not inserted in SDI data stream instead data available on the data stream is retained. This input must remain high for the complete duration of the line for which the CRC packet insertion is required.
TX_INSERT_VPID	1	Input	Input to enable or disable VPID insertion in the data stream. When high, core inserts VPID packets in each data stream, generated from the VPID byte provided on the VPID data input of respective data streams. When low, VPID packets are not inserted in SDI data stream instead data available on the data stream is retained. This input must remain high for the complete duration of the line for which VPID insertion is required.
<b>Status Outputs</b>			
TX_DS_MUX	1	Output	This output signal indicates the data stream multiplex type of the input data streams. If this output is low, it indicates Type1 multiplex is detected on the input data streams (one instances of TRS Words, Line Number Words, CRC Words, etc. in each data stream). If the output is high, it indicates Type2 multiplex is detected on the input data streams (two instances of TRS Words, Line Number Words, CRC Words, etc. in each data stream). Once multiplex type is detected, the output remains unchanged until there is change in multiplex type on the input data stream.
TX_TRS	1	Output	This output signal indicates that data on the SDI data stream output is first TRS word of the SDI data stream.
TX_BAD_TRS	1	Output	This output indicates that the TRS information on the SDI data stream is not valid TRS as mentioned in SMPTE standard. This output goes high whenever bad TRS is detected. This does not affect the data stream framing performed by the core.

**Note:** x can be 0, 1, 2, and 3.

**Note:** All the ports with suffix \_DS1, \_DS2, \_DS3, and \_DS4 are available in both 6G-SDI mode and 12G-SDI mode.

**Note:** All the ports with suffix \_DS5, \_DS6, \_DS7, and \_DS8 are available only in 12G-SDI mode.

**Note:** The VPID Data Inputs are 32-bit each. Bits [7:0] is the Byte1, Bits [15:8] is the Byte2, Bits [23:16] is the Byte3, Bits [31:24] is the Byte4.

# 4 Functional Description

CoreUHD\_SDITX is SDI Framer. The core accepts the raw video data and performs the framing of the SDI data stream. The framing is performed as per the SMPTE SDI protocol specification for the SDI mode configured.

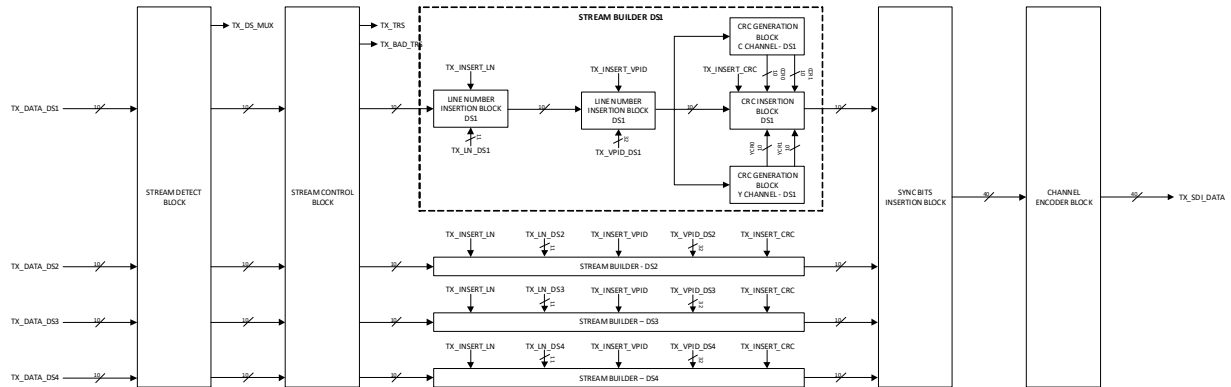
As per the SMPTE 6G-SDI and 12G-SDI specifications the individual data streams of the SDI data stream can be of either Type1 multiplex type or Type2 multiplex type based on the image mapping modes.

- **Type1 multiplex:** Each data stream has a single instance of TRS words, Line Numbers, CRC Words and so on.
- **Type2 multiplex:** Each data stream has two instances of TRS words, Line Numbers, CRC Words and so on.

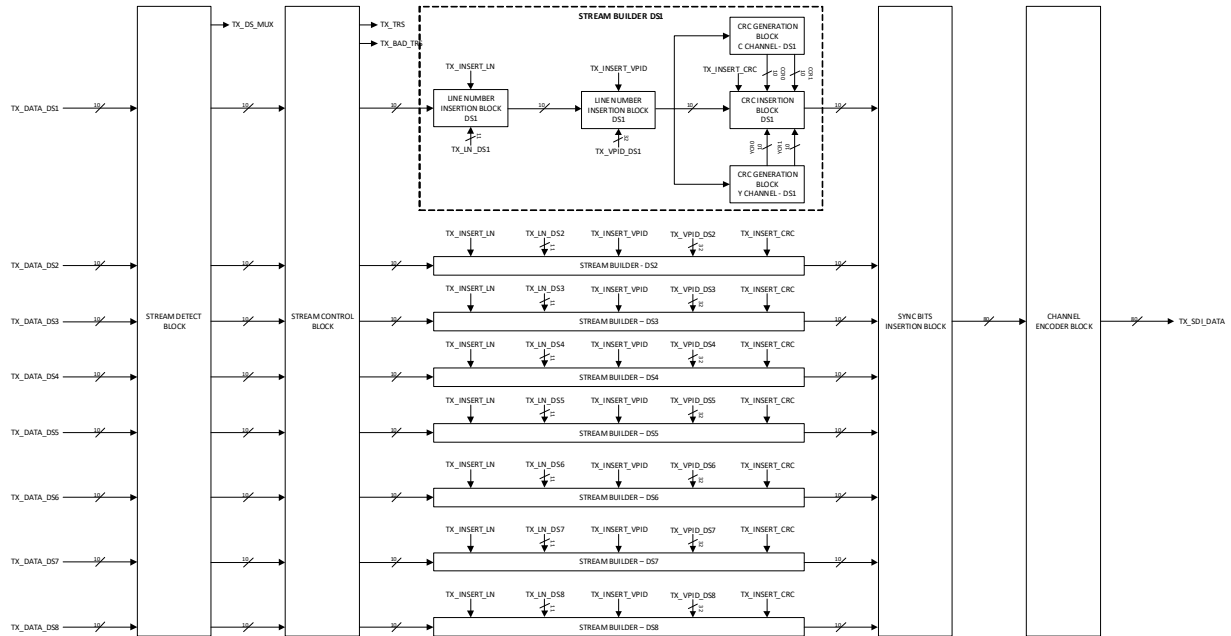
The core is capable of accepting both Type1 and Type2 multiplex SDI data stream. The core detects the type of the multiplexing and reports it on the TX\_DS\_MUX output.

In case of the Type2 multiplex data streams, the core performs LN insertion, VPID insertion and CRC generation and insertion on both channels of the multiplexed data stream.

**Figure 1 • CoreUHD\_SDITX Block Diagram in 6G-SDI Mode**



**Figure 2 • CoreUHD\_SDITX Block Diagram in 12G-SDI Mode**



The functional blocks of the core are described below:

## 4.1 Stream Detect Block

Stream Detect Block detects the timing reference words in the input data streams and generates the control signals required for the stream control block.

The block generates a signal to indicate the first word of the timing reference words. Also, the block detects the multiplex type of the data stream input based on the timing reference words.

## 4.2 Stream Control Block

Stream Control Block generates the control signals for the line number insertion block, VPID insertion block, CRC generation block, CRC insertion block and syncs bits insertion block.

The block generates TX\_TRS status signal indicating the first word of TRS is output on TX\_SD\_DATA output signal. Also the block detects, if a bad TRS signal is available on the input data streams.

## 4.3 Line Number Insertion Block

Line Number Insertion Block encodes the line number input into LN0 and LN1 line number packets as defined in the SMPTE specification. The encoded line number packets LN0 and LN1 are inserted into the data stream at the appropriate positions as defined in the SMPTE specification.

The block performs the line number packet insertion in the data stream if the TX\_INSERT\_LN input is high. This signal shall be high for the complete duration of the line for which line number packets insertion is required. If this signal is low, the block does not perform the line number insertion.

## 4.4 VPID Insertion Block

The VPID Insertion Block inserts the VPID packets into the data stream at the appropriate positions as recommended in the SMPTE specification. The user defined words of VPID packets are encoded from the VPID bytes input. Along with the user defined words, the block inserts the ancillary data flags, the data identification, the secondary data identification, the data count packets and the checksum words which are part of VPID packet. The VPID packets are inserted in the line number provided on the VPID line number input for each frame.

The block performs the line number packet insertion in the data stream if the TX\_INSERT\_VPID input is high. This signal shall be high for the complete duration of the frame for which VPID packets insertion is required. If this signal is low, the block does not perform the VPID insertion.

## 4.5 CRC Generation Block

CRC Generation Block computes the CRC value for each line of the input data stream. The CRC computation is as per CRC polynomial specified in the SMPTE specification.

$$\mathbf{CRC(X) = X^{18} + X^5 + X^4 + 1}$$

The 18-bit CRC is generated and encoded to form CR0 and CR1 CRC packets as defined in the SMPTE specification.

## 4.6 CRC Insertion Block

CRC Insertion Block inserts the CR0 and CR1 CRC packets into the data stream, at the appropriate positions as defined in the SMPTE specification.

The block performs the CRC packet insertion in the data stream if the TX\_INSERT\_CRC input is high. This signal shall be high for the complete duration of the line for which line number packets insertion is required. If this signal is low, the block does not perform the CRC insertion.

## 4.7 Sync Bits Insertion Block

Sync Bits Insertion Block performs the sync bit insertion on the 10-bit 3FF and 10-bit 000 timing reference words. The two LSB of 3FF word is replaced by 01b and that of 000 word is replaced by 10b.

The block inserts the sync bits only on the required timing reference signals as defined in SMPTE SDI specification retaining the 3FF 000 000 sequence which is required for the receiver to achieve synchronization and word alignment. The sync bits insertion depends on the SDI mode, and the input data stream multiplexing type.

## 4.8 Channel Encoder Block

Channel Encoder Block performs the scrambled NRZI encoding on the concatenated SDI data stream. The channel encoding is performed as per the polynomials specified in the SMPTE specification.

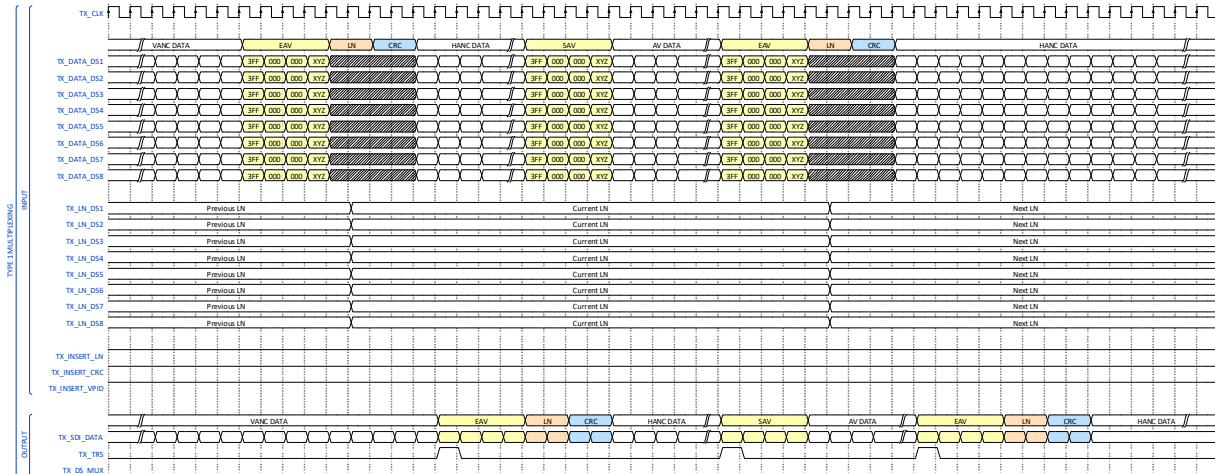
$$\mathbf{G_1(X) = X^9 + X^4 + 1 \text{ and } G_2(X) = X + 1}$$

# 5 Timing Diagrams

## 5.1 Type1 Multiplex Data Stream

The following figure shows the timing diagram for Type1 10-bit multiplex data stream.

**Figure 3 • Timing Diagram for Type1 10-bit Multiplex Data Stream**

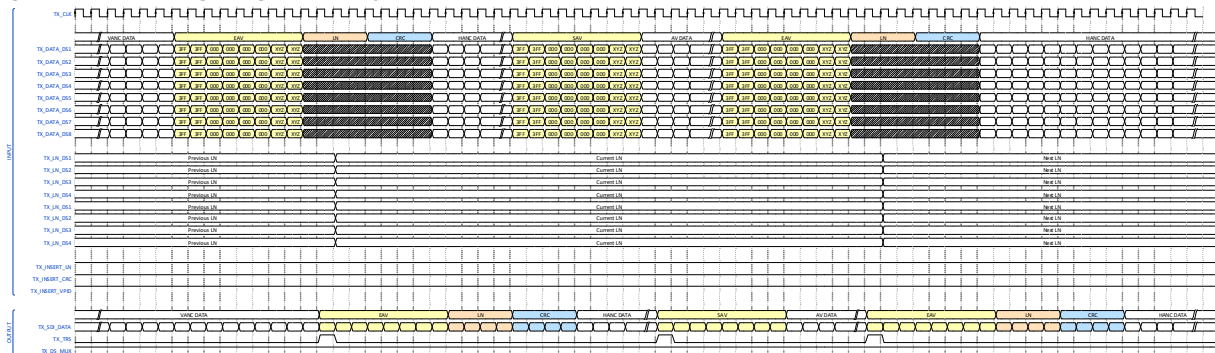


**Note:** In 6G-SDI mode, ignore the ports with suffix \_DS5, \_DS6, \_DS7, and \_DS8.

## 5.2 Type2 Multiplex Data Stream

The following figure shows the timing diagram for Type2 10-bit multiplex data stream.

**Figure 4 • Timing Diagram for Type2 10-bit Multiplex Data Stream**



**Note:** In 6G-SDI mode, ignore the ports with suffix \_DS5, \_DS6, \_DS7, and \_DS8.

## 6 Tool Flow

---

### 6.1 License

Core is available in two versions:

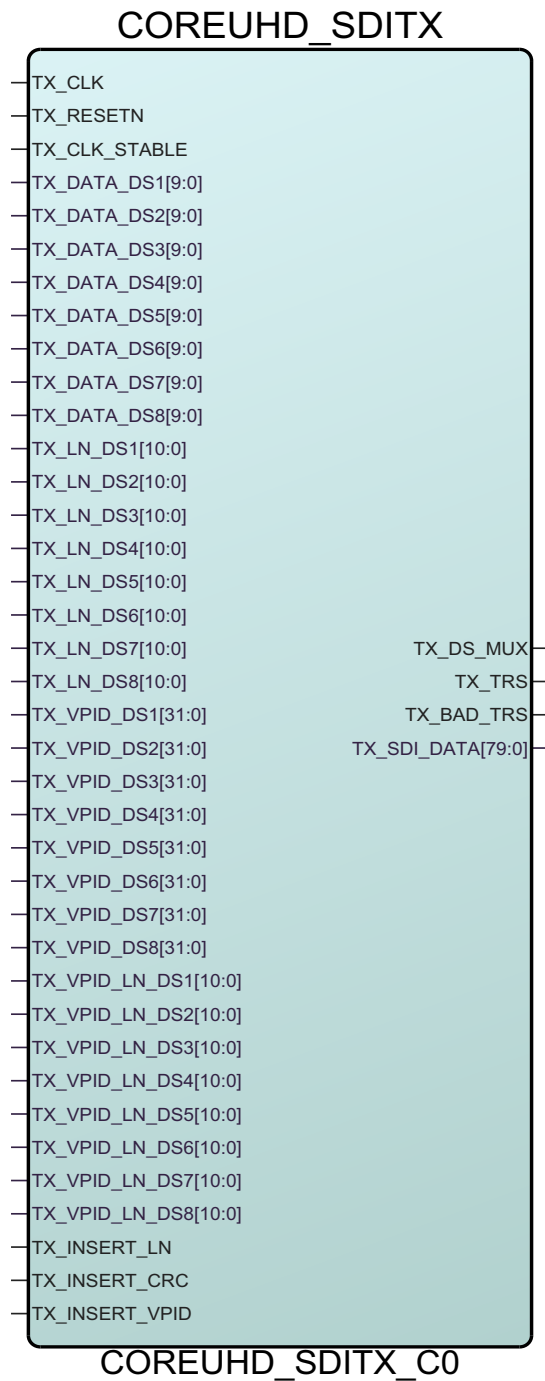
- **Evaluation:** Evaluation version is available for free and supports four hours of functionality on silicon.
- **Obfuscated:** Obfuscated version is license locked and is available only with Libero Platinum license.

### 6.2 Using core in Libero SmartDesign

Core is pre-installed in the SmartDesign IP deployment design environment or Core is downloaded from the online repository.

An example of the core instantiated in Libero SmartDesign is shown in the following figure.

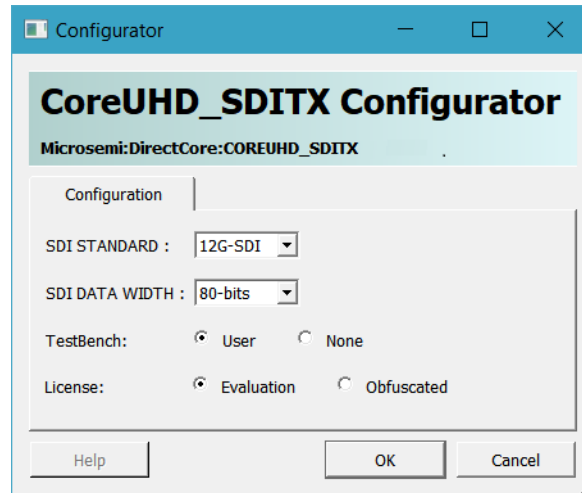
Figure 5 • Core Instance Full I/O View in SmartDesign



The core can be configured using the configuration GUI in the SmartDesign, as shown in the following figure.



**Figure 6 • Configuring the Core in SmartDesign**



For more information on using the SmartDesign to instantiate and generate cores, refer to the [Using DirectCore in Libero® SoC User Guide](#).

## 6.3 Simulation Flows

The User Testbench is provided along with the core.

To run the user testbench simulations, do the following steps:

1. Select **User** option for the Testbench flow in the **Core Configuration** window. When SmartDesign generates the design files, it also generates the user testbench files.
2. Set the design root to the core instantiation in the Libero design hierarchy pane and
3. Click **Simulation** in the Libero **Design Flow** window. This invokes ModelSim and automatically runs the user testbench simulation.

## 6.4 Synthesis in Libero

To run synthesis on the core, do the following steps:

1. Set the design root to the IP component instance.
2. Run the **Synthesis** tool from the Libero **Design Flow** pane.

## 6.5 Place-and-Route in Libero

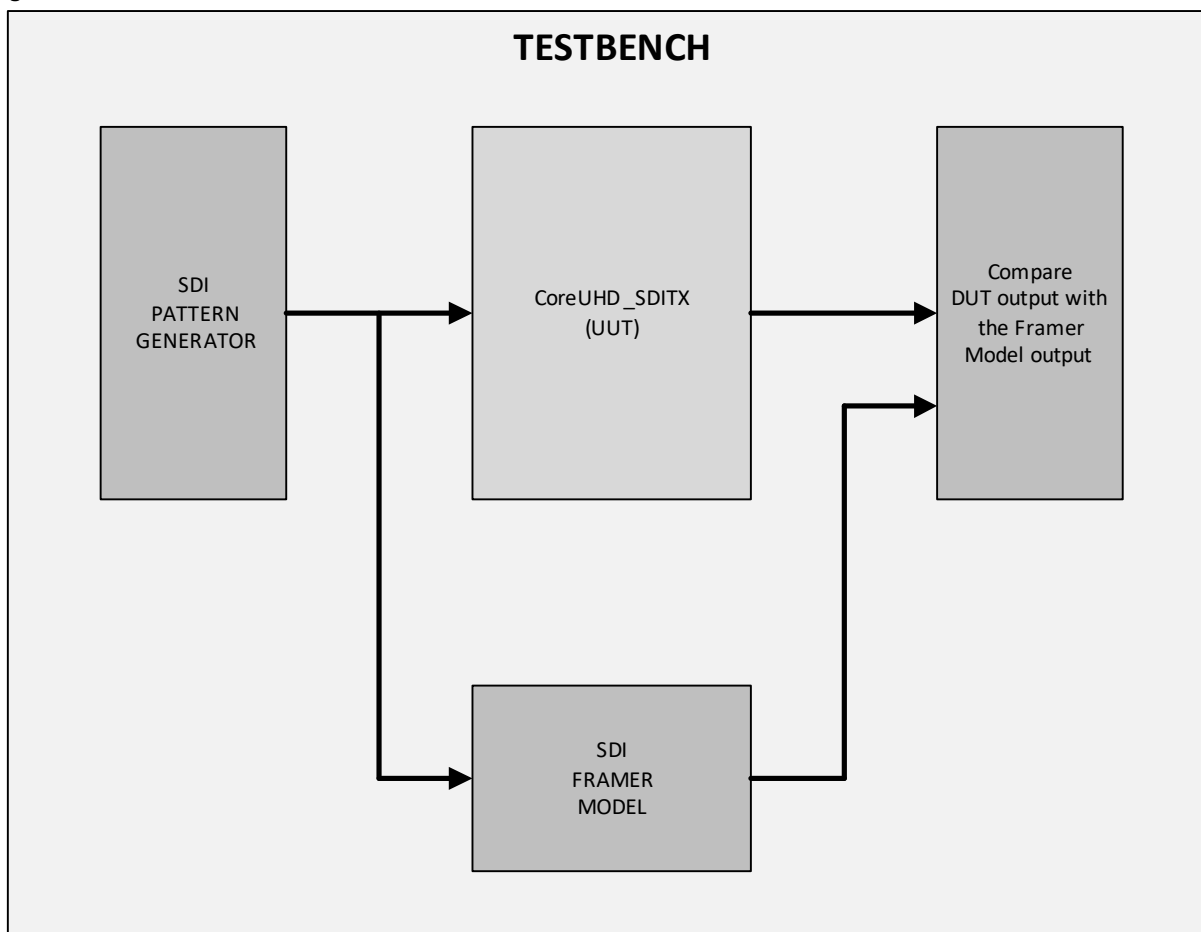
When the design is synthesized:

1. Run the **Place-And-Route** tool from the Libero **Design Flow** pane.

## 7 Testbench

UserTtestbench is provided with the core that verifies a few of the features.

**Figure 7 • User Testbench**



The user testbench has instance of the core - Unit Under Test (UUT), an SDI Pattern Generator, an SDI Framer Model, and a data comparator module.

The testbench configures the SDI Pattern Generator, UUT, and the SDI Framer Model with the parameters for which the core is being configured from configurator GUI.

The pattern generator generates the data streams, line number data, VPID data, VPID line number data, and control signals required to connect to the UUT, and the SDI Framer Model based on the configured mode.

The UUT performs the framing of the raw video into the SDI data stream. The SDI Framer Model also performs the framing of the raw video into the SDI data stream. The SDI data output of both UUT and SDI Framer Model is provided as inputs to the data comparator module.

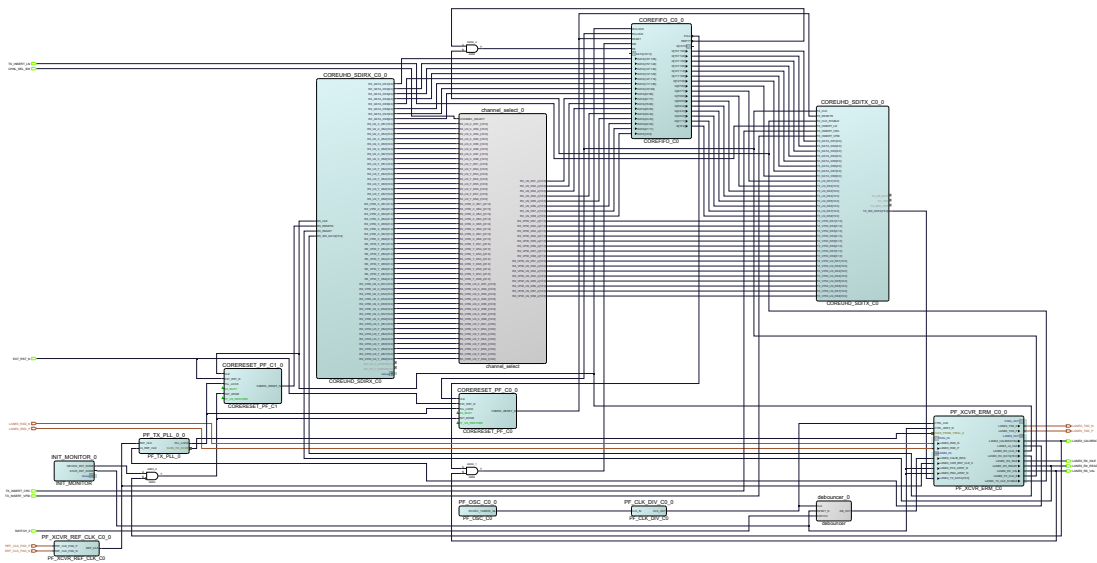
The data comparator checker compares the SDI data output from the UUT with the SDI data output from the SDI Framer Model. The module reports if there is any data mismatch between the output of the UUT and SDI Framer Model.

## 8 System Integration

In this example design:

- CoreUHD\_SDIRX (COREUHD\_SDIRX\_C0\_0) is configured in required SDI mode (6G-SDI or 12G-SDI). This core de-frames the SDI data stream into raw video data.
- CoreUHD\_SDITX (COREUHD\_SDITX\_C0\_0) is configured in required SDI mode (6G-SDI or 12G-SDI), same as COREUHD\_SDIRX\_C0\_0. COREUHD\_SDITX\_C0\_0 frames the raw data into SDI data stream.
- In 6G-SDI mode, PF\_XCVR\_ERM (PF\_XCVR\_ERM\_C0\_0) is configured for data rate of 5940 Mbps in PMA mode with Receiver Calibration set to “CDR”, 40-bit interface data width, and 148.5 MHz reference clock.
- In 12G-SDI mode, PF\_XCVR\_ERM\_C0\_0 is configured for data rate of 11880 Mbps in PMA mode with Receiver Calibration set to “On Demand and First Lock”, 80-bit interface data width, and 148.5 MHz reference clock.
- XCVR\_INIT\_DONE signal of PF\_INIT\_MONITOR (INIT\_MONITOR\_0) is connected to PCS\_RST\_N, PMA\_RST\_N, and CTRL\_ARST\_N reset inputs of PF\_XCVR\_ERM\_C0\_0.
- LANE0\_CDR\_REF\_CLK\_0 input of PF\_XCVR\_ERM\_C0\_0 is driven by 148.5 MHz clock from REF\_CLK of PF\_XCVR\_REF\_CLK (PF\_XCVR\_REF\_CLK\_C0\_0).
- CTRL\_CLK (ERM clock) of PF\_XCVR\_ERM\_C0\_0 is driven by 40MHz clock generated from 160 MHz clock driven by OSC (PF\_OSC\_C0\_0) using clock divider (PF\_CLK\_DIV\_C0\_0).
- The JA\_CLK port of the PF\_XCVR\_ERM\_C0\_0 is enabled for jitter cleaning purpose.
- PF\_TXPLL (PF\_TX\_PLL\_0\_0) is configured in jitter cleaning mode. REF\_CLK of PF\_XCVR\_REF\_CLK\_C0\_0 drives the REF\_CLK input of PF\_TX\_PLL\_0\_0. JA\_CLK port of the PF\_XCVR\_ERM\_C0\_0 drives the JA\_REF\_CLK input port of PF\_TX\_PLL\_0\_0.
- FABRIC\_RESET\_N from CoreRESET\_PF (CORERESET\_PF\_C0\_0) is connected to TX\_RESETN input of COREUHD\_SDITX\_C0\_0. FABRIC\_RESET\_N from CoreRESET\_PF (CORERESET\_PF\_C1\_0) is connected to RX\_RESETN input of COREUHD\_SDIRX\_C0\_0.
- RX\_CLK of COREUHD\_SDIRX\_C0\_0 is driven from LANE0\_RX\_CLK\_R of PF\_XCVR\_ERM\_C0\_0 and TX\_CLK of COREUHD\_SDITX\_C0\_0 is driven from LANE0\_TX\_CLK\_R of PF\_XCVR\_ERM\_C0\_0. The LANE0\_RX\_CLK\_R and LANE0\_TX\_CLK\_R clock frequency is 148.5 MHz in both 6G-SDI and 12G-SDI modes.
- The raw video data from COREUHD\_SDIRX\_C0\_0 is looped back onto COREUHD\_SDITX\_C0\_0 through CoreFIFO (COREFIFO\_C0\_0).
- The TX\_INSERT\_LN, TX\_INSERT\_CRC, and TX\_INSERT\_VPID inputs of COREUHD\_SDITX\_C0\_0 are connected to DIP switches for enabling or disabling the insertion of line number, CRC, and payload ID respectively.
- The Channel\_select (channel\_select\_0) is a custom module used to select between the line number data and VPID data bytes extracted from C channel or Y channel of data stream from COREUHD\_SDIRX\_C0\_0 for providing it on the line number data and VPID data byte inputs of COREUHD\_SDITX\_C0\_0 for LN and VPID insertion. Selection is done based on DIP switch.

Figure 8 • System Integration



## 9 References

---

- SMPTE ST 2081-1 - 6 Gb/s Signal / Serial Digital Interface
- SMPTE ST 2082-1 - 12 Gb/s Signal / Serial Digital Interface
- SMPTE ST 352 - Payload Identification Codes for Serial Digital Interface
- UG0667 - Microsemi PolarFire FPGA User Guide