Serial Memory Technology White Paper

OVERVIEW

Innovations in memory infrastructure are poised to significantly improve the performance and cost effectiveness of mainstream data center applications. Business applications are under significant pressure to collect, analyze, store and deliver time-sensitive value to end customers while simultaneously driving down costs.

These applications are drawing upon large quantities of global data sources — sensor data, historical data, location data, and customer-specific data — all of which must be scrutinized in real time. Memory infrastructure innovation is occurring along two vectors: near memory innovations and far memory innovations.

Near memory innovation improves business application performance by driving up the number of SoC and CPU memory channels, and improving the bandwidth of those individual memory channels while enabling innovative and lower cost memory technologies to be connected seamlessly to the SoC.

Far memory innovation delivers shareable pools of memory resources that both drive up aggregate system memory utilization (and therefore drive down cost), and improve application performance as arrays of SoC devices can simultaneously operate on the shared memory pool. Memory infrastructure encompasses a broad range of new and emerging media types and interface technologies.

A broad range of silicon SoC devices, including mainstream CPU processors, application-specific artificial intelligence (AI) devices, network processors, and other Application Specific Standard Products (ASSP), can all benefit from innovations in memory hierarchy. Multiple examples of new memory interface technology, such as Open Memory Interface (OMI), Compute Express Link (CXL), and Gen-Z, have emerged. SoC devices adopting these memory interface technologies can increase the number of independent memory channels while using far fewer SoC pins and therefore reducing the cost of SoC packaging. These new interface technologies also are media independent. System builders can change the cost and performance profile of their deployed equipment by changing the type of media connected to these SoC interfaces. This type of SoC memory direct attachment is called near memory technology.

This white paper focuses on the Open Memory Interface (OMI) and how it addresses the needs of near memory.

INTRODUCTION TO OPEN MEMORY INTERFACE (OMI)

The Open Memory Interface is an industry standard. It contains the memory semantics subset of the full OpenCAPI 3.1 standard from the OpenCAPI Consortium.

Overcoming the Challenges of Parallel Memory

Silicon devices using traditional parallel attached DRAM memory channels cannot continue adding more channels to meet their workload requirements. This product provides a standards-based serial interface so silicon devices can add 4X the number of channels. Secondly, silicon devices with traditional parallel attached DRAM memory cannot support multiple types of memory media with different cost and performance metrics. OMI provides an abstraction layer so that silicon devices can attach different types of media, such as to DDR4 DRAM memory, in this case.

OMI Ecosystem

The key ecosystem elements for broad use of Open Memory Interface (OMI) by CPU and SoC developers are in place. The key elements include design IP, verification IP, open standards, and memory component suppliers. On IP – the OpenCAPI Consortium provides royalty-free Host and Target IP, as well as sponsors compliance activities that foster interoperability. Commercial verification IP is available from multiple sources. Since OMI is an open industry standard, multiple firms, including Microchip, can develop semiconductor products in this emerging memory infrastructure market. DRAM and Storage Class Memory suppliers can utilize these standard semiconductor products and mount them alongside their memory components to build industry standard memory module solutions for servers and other types of end market equipment.

BENEFITS OF THE SMC 1000

The SMC 1000 provides three key benefits:

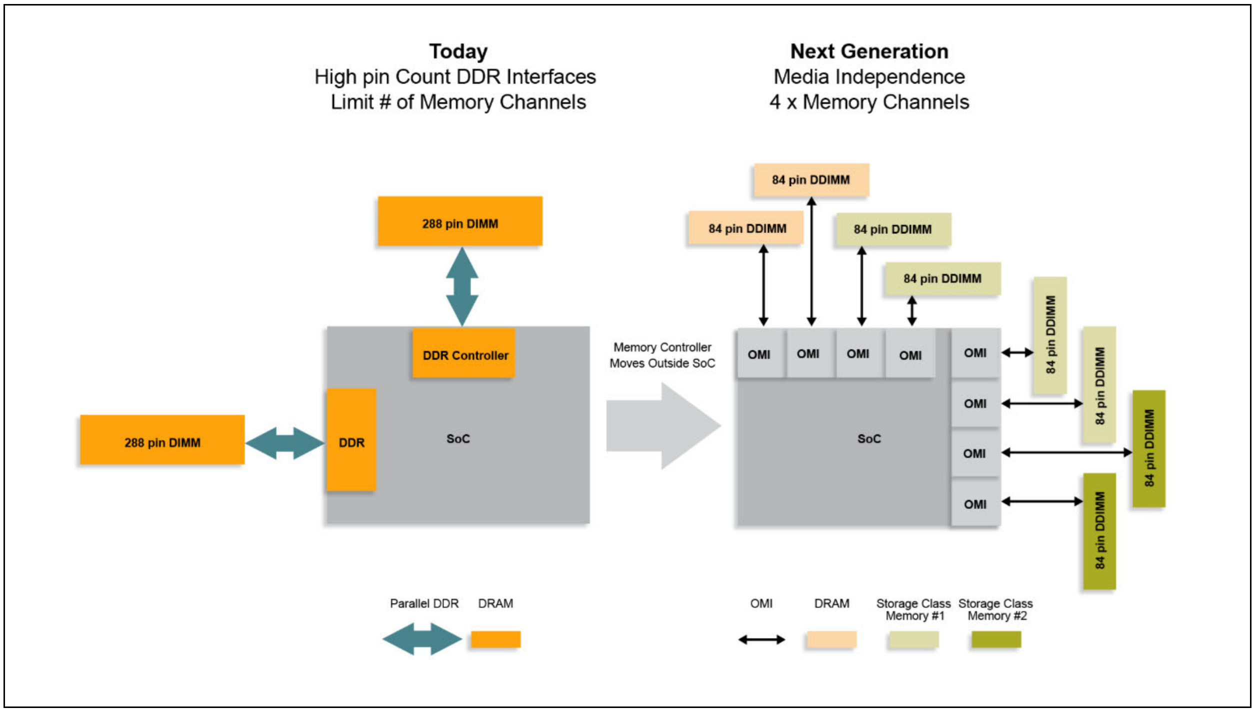
- Increased Memory Bandwidth:
  - OMI requires approximately 75 signals plus power/ground pins per memory channel while traditional parallel DDR memory channels require up to 300
  - OMI therefore delivers up to 4 times the number of memory channels in the same package size
- Memory media type independence:
  - OMI provides a standards-based abstraction layer above the downstream media type and speed (such as DDR, LPDDR, storage class memory, etc.)
  - CPUs and SoCs utilizing OMI can therefore utilize different media types without changing their OMI interface on the SoC
- Lower Solution Cost:
  - OMI enables CPU and SoC builders to reduce their die cost, package cost, and IP costs, and overall R&D cost

Bandwidth Improvements

OMI improves memory bandwidth by enabling the SoC to increase the number of memory channels and therefore increase the memory bandwidth. For example, if traditional DDR4-3200 memory channels that utilize upwards of 300 pins can deliver 25 GB/s, an OMI memory channel that utilizes upwards of 75 pins can deliver the same 25 GB/s. Therefore, the SoC can utilize four OMI memory channels in the same pin count and deliver upwards of 100 GB/s of memory bandwidth.

The diagram below compares a traditional parallel DDR SoC to an equivalent pin count SoC using serial memory technology such as OMI.

FIGURE 1:



Media Independence

The SMC 1000 translates OMI Load/Store memory commands/data into DDR4-3200 commands/data. Future similar products could translate that identical OMI Load/Store memory commands/data into other media types such as alternative DDR technology (LPDDR, GDDR) or storage class memory, which may have very different physical interfaces and timing requirements compared to traditional DRAM.

Security

Security is a key product requirement for semiconductor products. Silicon security ensures not only the integrity of your data, but also prevents denial-of-service attacks. The SMC 1000 8x25G utilizes an on-board processor for control plane operations with associated firmware. Microchip has included integrated proven hardware root-of-trust so CPU and SoC builders can validate the authenticity of the SMC 1000 8x25G device. In addition, the SMC 1000 8x25G supports secure firmware boot and secure firmware updates to ensure the authenticity of the associated firmware image.

Latency

Microchip has innovated to deliver an exceptionally low latency product. Everything from the OMI SERDES, OMI protocol, DDR memory controller and DDR PHY have been implemented to minimize delay through the product.

Data center application workloads require OMI-based DDIMM memory products to deliver the same high-performance bandwidth and low latency results of today's parallel-DDR based memory products. Microchip's SMC 1000 8x25G features an innovative low latency design that delivers less than 4 ns incremental latency over a traditional integrated DDR controller with LRDIMM. This results in OMI-based DDIMM products having virtually identical bandwidth and latency performance to comparable LRDIMM products.

LATENCY IN A SYSTEM

Under typical operation, many load/store commands are in-flight and are being queued in the memory controller — which in this case is queued in the SMC1000 8x25G. In this case, the only difference in latency between a native traditional parallel DDR memory and an OMI based memory is the OMI SERDES delay back to the SoC, which is just under 4 ns.

The following table compares the read latency of an LRDIMM vs a DDIMM, including the DRAM. Write latency is not impacted.

TABLE 1: READ LATENCY OF LRDIMM VS DDIMM

	Read (ns)
LRDIMM	41.5
DDIMM (Loaded)	45.4

Power

In addition, the SMC 1000 8x25G also provides automatic low-power modes. When the traffic to the memory is low, the OMI interface automatically reduces the number of active lanes from 8 down to 4 or even 2. In a system with 16 channels of DDR, utilization of low-power modes could add up to 12 watts of power savings.

IMPLEMENTATION OPTIONS FOR SERIAL MEMORY

There are several options available for solution providers. The most accessible is the DDIMM form factor. There are options to implement planar applications and NVDIMM-N applications as well.

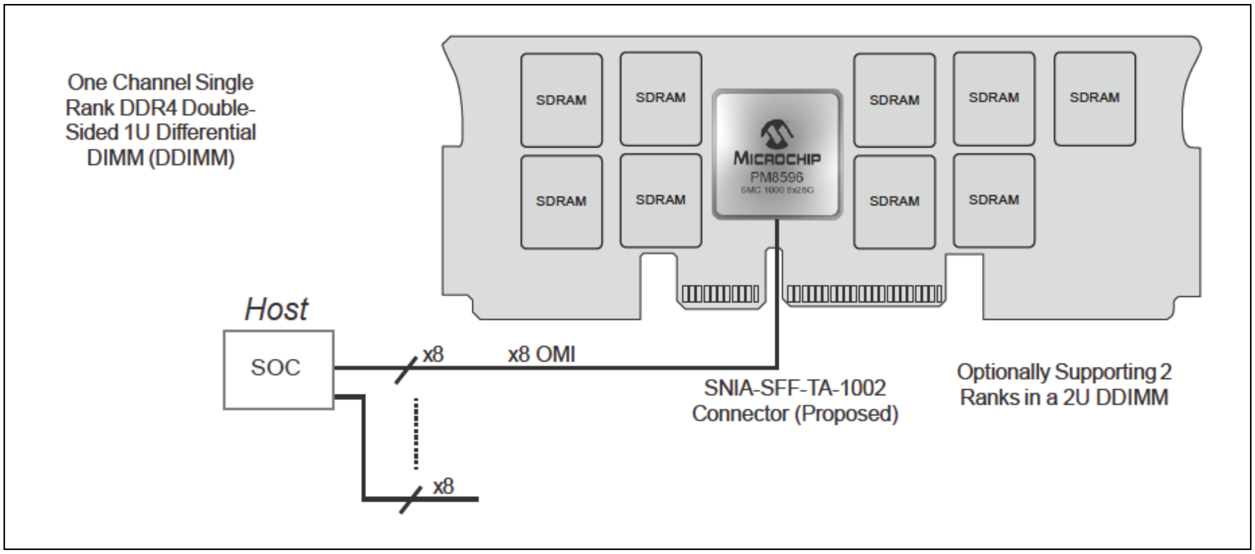
The DDIMM Form Factor

SMC 1000 based DDIMM is available from SMART Modular, Samsung Electronics, and Micron in the 1U and 2U DDIMM format.

DDIMMs will be available in at least 16 GB, 32 GB, 64 GB, 128 GB and 256 GB sizes.

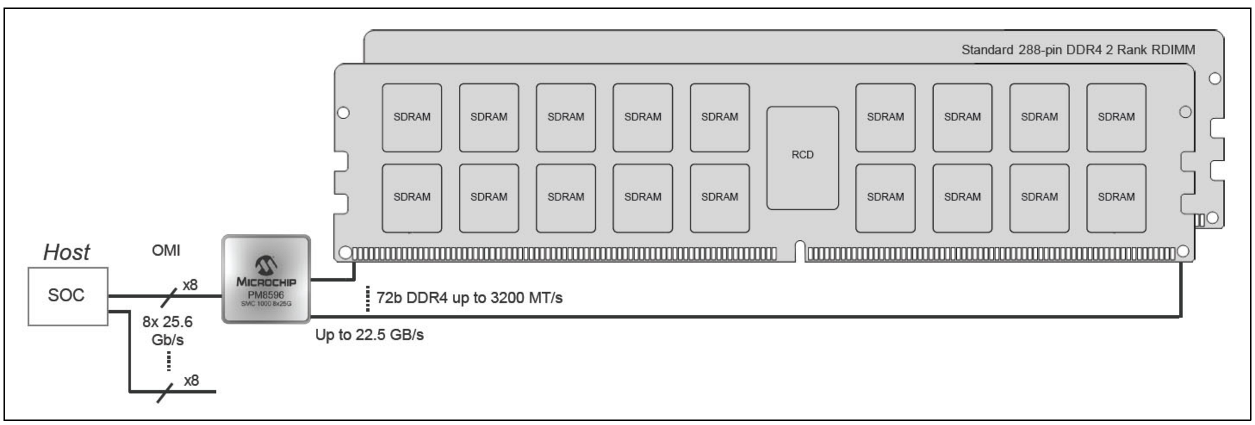
The diagrams below show the relative physical size of a 1U DDIMM vs a DDR4 LRDIMM.

FIGURE 2:



The 1U DDIMM is 85 mm wide and 30.35 mm the from edge connector to the top of the DDIMM. It utilizes the SNIA-SFF-TA-1002 84-pin connector, with 22 signal pins, as well as power pins. It contains the SMC 1000 OMI 8x25G serial to parallel memory controller, a power management controller, regulators, SEEPROM, SPI Flash and the DRAMs. It has components populated on both sides. The 2U DDIMM has the same width and interface connector but is 67.85mm in height.

FIGURE 3:

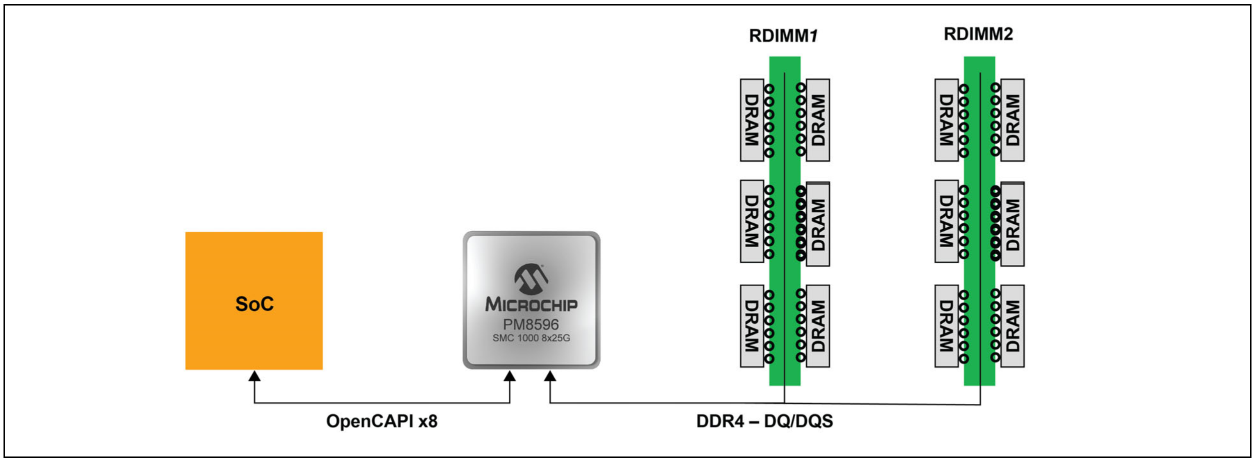


By comparison, a DDR4 LRDIMM is approximately 133 mm wide and 31 mm high and utilizes a 288-pin connector.

Planar Applications

Planar, or chip-down applications are also supported. The SMC 1000 can connect up to four rank loads and two and four-high 3DS per rank. A planar application with commercial off-the-shelf RDIMMs can easily be realized.

FIGURE 4:



NVDIMM-N Support

An alternative planar application would be to leverage industry standard NVDIMM-Ns behind an SMC 1000. This would enable an OMI interface to the NV-DIMM-Ns. NVDIMM-N is a non-volatile memory product. It provides high-speed load/store access to DRAM, and also contains a non-volatile NAND. When power goes down, data in the NVDIMM-N's DRAM must be flushed to the NAND. Microchip's product provides functionality to ensure that all data/commands are flushed to the NVDIMM-N in scenarios like this.

SMART MEMORY PRODUCTS FROM MICROCHIP

Current Serial Memory Products from Microchip

Microchip provides industry standard serial memory controller products.

TABLE 2: ORDERING INFORMATION

Orderable Part Number	Product Name	SOC Interface	Memory Interface	Packaging
PM8596A1-FEI	SMC 1000 8x25G	x4/x8 25 Gbps OMI	72 b DDR4 3200 MT/s	17x17 mm FCBGA

Commercially Available DDIMMs Utilizing Microchip Products

The following is a preliminary partial list of DDIMM commercial products available from memory module companies utilizing the Microchip SMC 1000 8x25G. Contact the vendors below to get the most up to date list.

TABLE 3: DDIMMS

Vendor	Orderable Part Number	Form Factor	Memory
Samsung Electronics	M353A2K40DB0	1U	16 GB DDR4
Samsung Electronics	M354A4K40DB0	2U	32 GB DDR4
Samsung Electronics	M354A8G40AB0	2U	64 GB DDR4
Samsung Electronics	M354AAG40M30	2U	128 GB DDR4
SMART Modular	SR2047DD420425HC	1U	16 GB DDR4
SMART Modular	SR4097DD440425HA	1U	32 GB DDR4
SMART Modular	SR4097DE420425HC	2U	32 GB DDR4
SMART Modular	SR8197DE440425HA	2U	64 GB DDR4
Micron	MTA36AHF4G72NZ-3G2E1B5	2U	32 GB DDR4
Micron	MTA36AHF8G72NZ-3G2B1B5	2U	64 GB DDR4
Micron	MTA72AHS16G72NZ-3S2B1B5	2U	128 GB DDR4

Future Memory Infrastructure Products

As a leader in Memory Infrastructure, Microchip is planning a variety of enabling technologies to support both near and far-memory applications. To learn more, please contact Microchip, or visit our Memory Products page:
www.microchip.com/smartmemory

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