Microsemi Clock Generators for SmartFusion and IGLOO FPGA Families

Introduction

Today's FPGA offerings address requirements across a wide set of applications including wireless and wired networks, software-defined networking, video, industrial networking and cloud computing. Furthermore, as a result of an FPGA's ability to incorporate standards-based IP, high speed serial transceivers, low power dissipation and system level integration, FPGA's are quickly replacing alternative ASIC and ASSP solutions. As the capabilities of an FPGA increase so do the performance requirements of the reference clocks used by an FPGA. Microsemi offers several synthesis and rate conversion/jitter attenuation devices that exceed reference clock requirements. The following pages of this document provide Microsemi solutions for the various FPGA products surveyed.

Microsemi clock generation devices listed in Table 1 meet the phase noise requirements needed by the FPGA's reference clock(s). To be a valid Ref Clock source, the clock generator's jitter performance must be better than the FPGA's Ref Clock jitter requirement.

Table 1. Recommended Clock Generators

FPGA Family	Ref Clock Freq (MHz)	Microsemi Jitter Performance Typical (ps RMS)		
		10 kHz	100 kHz	1 MHz
		ZL30250/1 ZL30244/5	ZL30252/3 ZL30255	ZL30262/3 ZL30266/7
IGLOO®2 M2GL005, M2GL010 M2GL025, M2GL050 M2GL060, M2GL090 M2GL150 IGLOO/e IGLOO nano IGLOO PLUS	100[1]	0.193	0.277	0.245
	125.0	0.182	0.263	0.202
	156.25	0.180	0.266	0.185
	250	0.172	0.254	0.189
	312.5	0.169	0.254	0.207
	625	0.160	0.249	0.165
SmartFusion®2 M2S005, M2S010 M2S025, M2S050 M2S060, M2S090 M2S150	100[1]	0.193	0.277	0.245
	125.0	0.182	0.263	0.202
	156.25	0.180	0.266	0.181
	250	0.172	0.254	0.189
	312.5	0.169	0.254	0.207
	625	0.160	0.249	0.165

Table 1 Notes:

1. PCIe Gen 3, Gen 2 and Gen 1 compliant.

If you do not find the information you are looking for here please contact clocktree@microsemi.com

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