UG0877
User Guide
SLVS-EC Receiver for PolarFire FPGA

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

The first publication of this document.

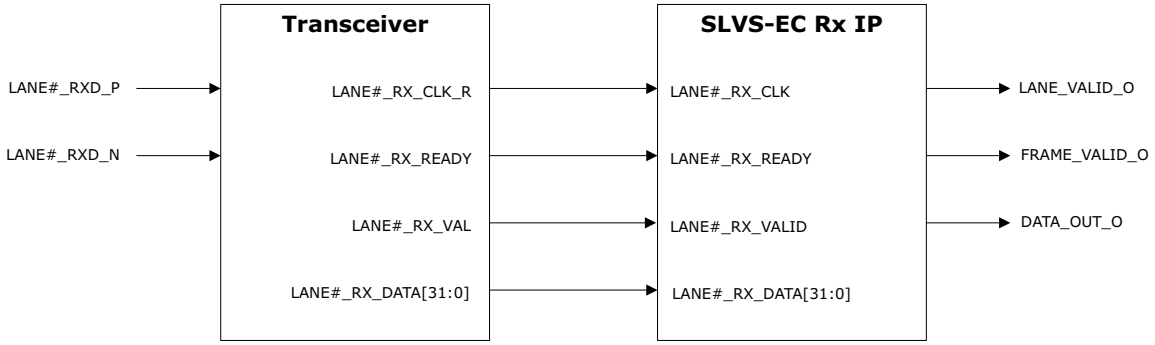
2 SLVS-EC IP

SLVS-EC is Sony's high-speed interface for next-generation high-resolution CMOS image sensors. This standard is tolerant of lane-to-lane skew because of embedded clock technology. It makes a board-level design easy in terms of high-speed and long-distance transmission.

SLVS-EC Rx IP core provides SLVS-EC interface for PolarFire FPGA to receive image sensor data. The IP core supports one lane and two lanes for RAW8 data type.

The following figure shows the system diagram for the SLVS-EC camera solution.

Figure 1 • **SLVS-EC IP Block Diagram**

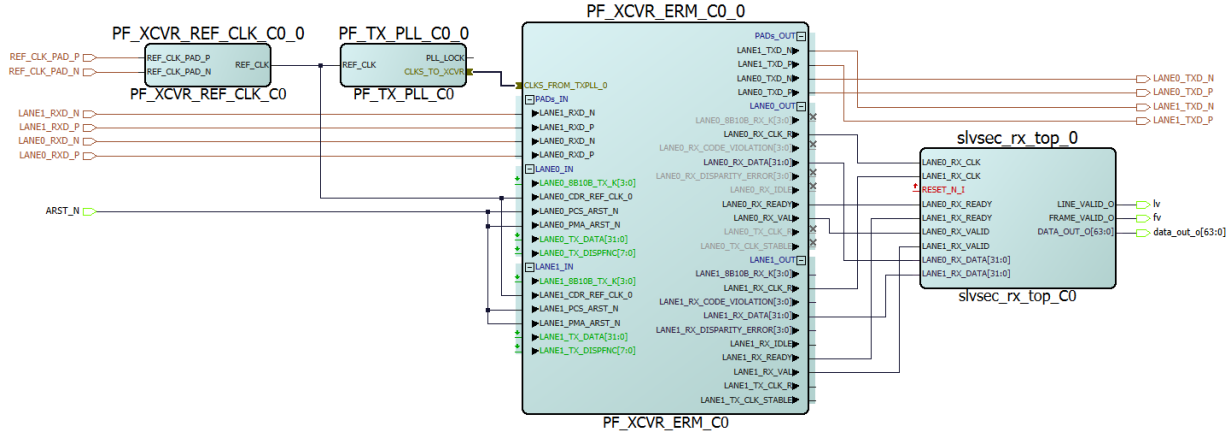


PolarFire® transceiver is used as the PHY interface for the SLVS-EC sensor since the SLVS-EC interface uses embedded clock technology. It also uses 8b10b encoding, which can be recovered using the PolarFire transceiver. PolarFire FPGA has up to 24 low-power 12.7 Gbps transceiver lanes. These transceiver lanes can be configured as the SLVS-EC PHY receiver lanes. As shown in the preceding figure, the transceiver outputs are connected to SLVS-EC Rx IP core.

2.1 SLVS-EC Receiver Solution

The following figure shows the Libero SoC software top level design implementation of SLVS-EC IP and the required components for the SLVS-EC receiver solution.

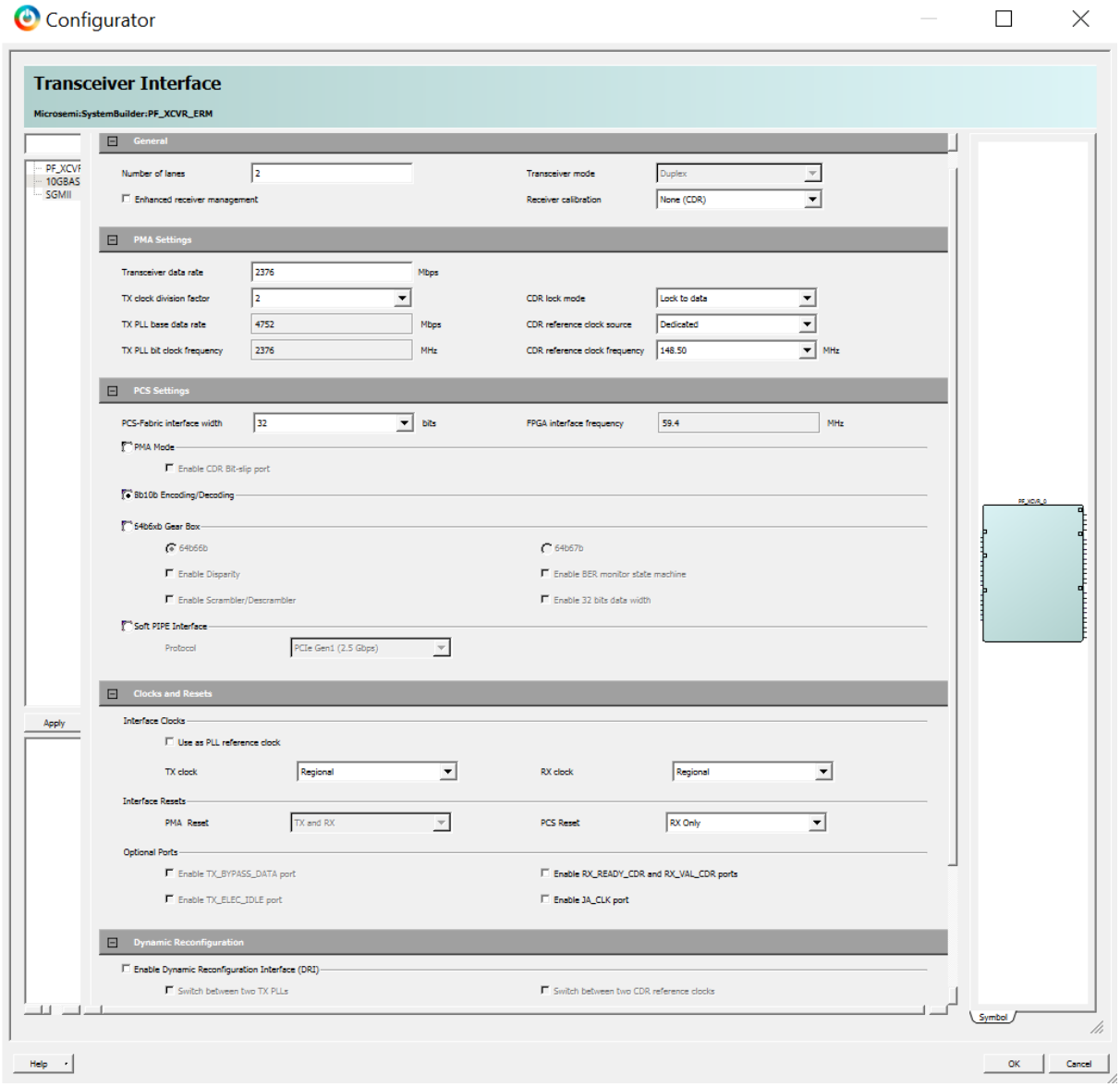
Figure 2 • **SLVS-EC IP SmartDesign**



2.2 Transceiver Configuration

The following figure shows the transceiver interface configuration.

Figure 3 • **Transceiver Interface Configurator**



The Transceiver can be configured to either one lane or two lanes. Also, the speed of the transceiver can be set at the "Transceiver data rate". SLVS-EC interface supports two baud rates as listed in following table.

Table 1 • **SLVS-EC Baud Rate**

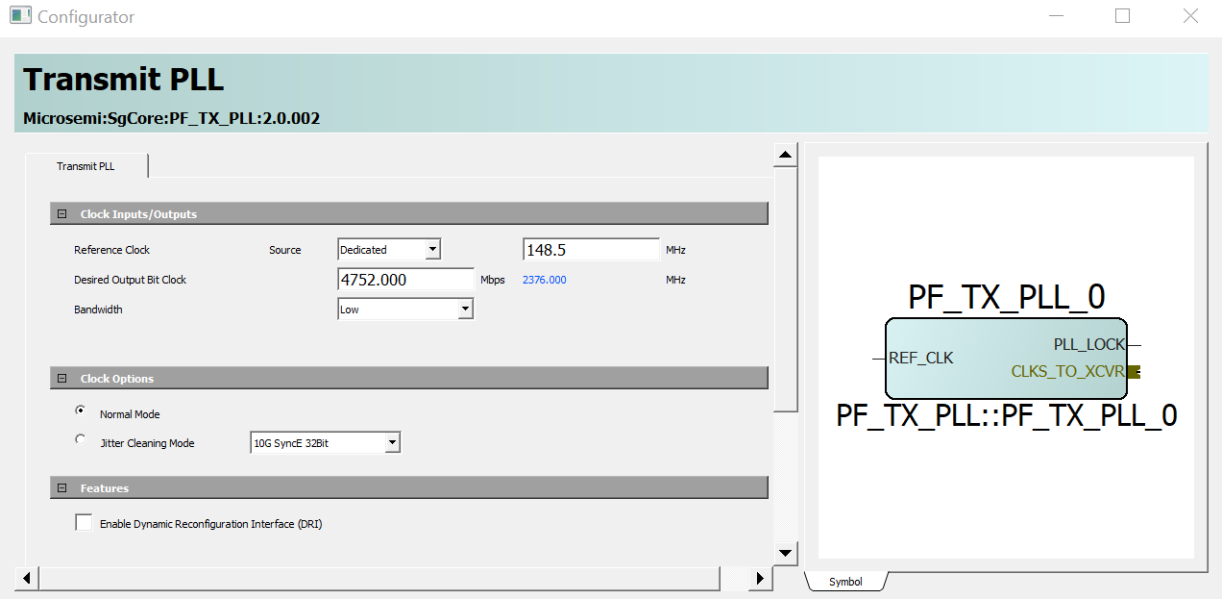
Baud Grade	Baud Rate in Mbps
1	1152
2	2304

Set the reference clock to 148.5 MHz at CDR reference clock frequency as set in the Transceiver interface configurator.

2.2.1 Transmit PLL

A transmit PLL (PF_TX_PLL) is required to configure the clocks to the transceiver. PF_TX_PLL generates the clocks required for the transceiver. Configure the PF_TX_PLL as shown in following figure.

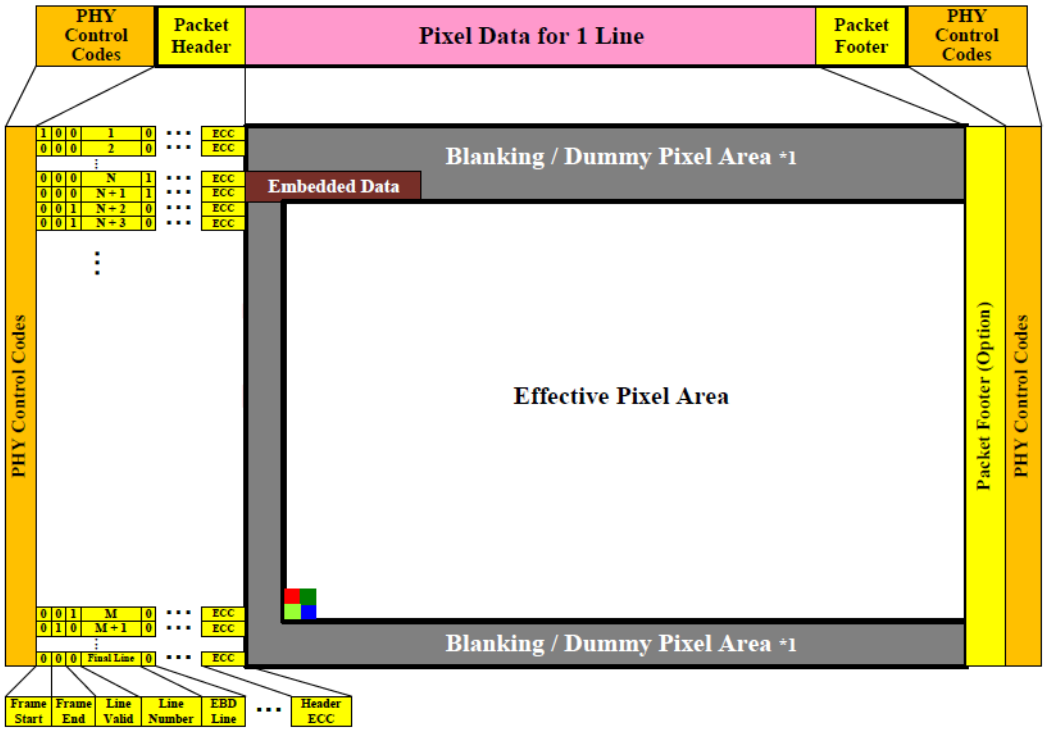
Figure 4 • **Transmit PLL Configurator**



2.3 Design Description

The following figure shows the SLVS-EC Frame Format structure.

Figure 5 • **SLVS-EC Frame Format Structure**



The Packet header contains information about the frame start and end signals along with the Valid lines. PHY control codes are added above the packet header to form the SLVS-EC packet. The following table lists the different PHY control codes used in the SLVS-EC protocol.

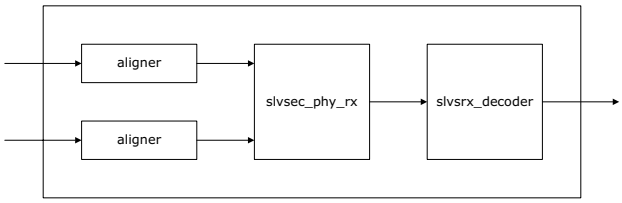
Table 2 • **PHY Control Code**

PHY Control Code	8b10b Symbol Combination
Start Code	K.28.5 - K.27.7 - K.28.2 - K.27.7
End Code	K.28.5 - K.29.7 - K.30.7 - K.29.7
Pad Code	K.23.7 - K.28.4 - K.28.6 - K.28.3
Sync Code	K.28.5 - D.10.5 - D.10.5 - D.10.5
Idle Code	D.00.0 - D.00.0 - D.00.0 - D.00.0

2.3.1 SLVS-EC RX IP Core

This section describes the hardware implementation details of SLVS-EC Receiver IP. The following figure shows the Sony SLVS-EC receiver solution that contains the PolarFire SLVS-EC RX IP. This IP is used in conjunction with the PolarFire transceiver interface block. The following figure shows the internal blocks of the SLVS-EC Rx IP.

Figure 6 • **Internal Blocks of the SLVS-EC RX IP**



2.3.1.1 aligner

This module receives the data from the PolarFire transceiver blocks and aligns to the sync code. This module looks for the sync code in the bytes received from the transceiver and locks to the byte boundary.

2.3.1.1.1 slvsec_phy_rx

This module receives the data from the aligner and decodes the incoming SLVS PHY packets. This module passes through the synchronization sequence and then, generates the pkt_en signal starting from Start code and ends at the end code. It also removes the PAD code from the data packets and sends the data to the next module that is slvsrx_decoder.

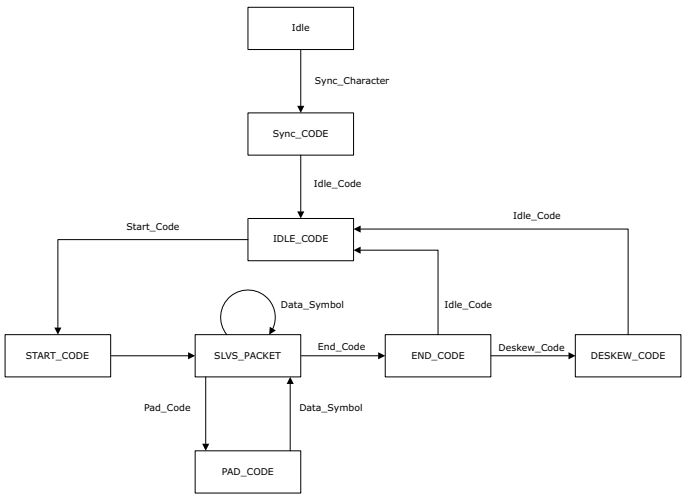
2.3.1.1.2 slvsrx_decoder

This module receives the data from the slvsec_phy_rx module and extracts the pixel data from the payload. This module extracts four pixels per clock per lane and sends to the output. It generates the line valid signal for the active lines validating the active video data. It also generates the Frame valid signal by looking at the frame start and frame end bits in the packet header of the SLVS-EC packets.

2.3.2 FSM with Data Decoding States

The following figure shows the FSM for SLVS-EC RX IP.

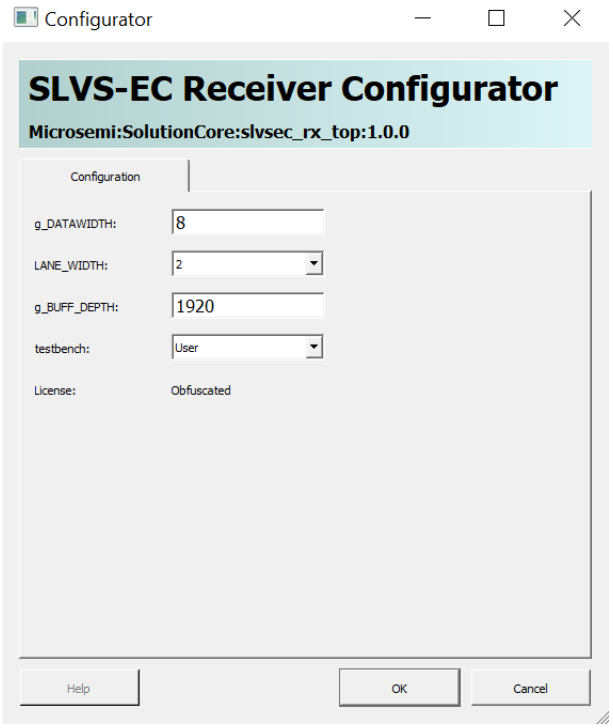
Figure 7 • **FSM for SLVS-EC RX IP**



2.3.2.1 SLVS-EC Receiver IP Configuration

The following figure shows the SLVS-EC receiver IP configurator.

Figure 8 • **SLVS-EC Receiver IP Configurator**



2.3.3 Configuration Parameters

The following table lists the description of the configuration parameters used in the hardware implementation of SLVS-EC receiver IP block. These are generic parameters and can vary based on the application requirements.

Table 3 • **Configuration Parameters**

Name	Description
g_DATAWIDTH	Input pixel data width. Supports 8-bit.
LANE_WIDTH	Number of MIPI lanes. Supports 1, 2 lanes.
g_BUFF_DEPTH	Depth of the buffer. Number of active pixels in active video line.

2.3.4 Inputs and Outputs

The following table lists the input and output ports of the SLVS-EC RX IP configuration parameters.

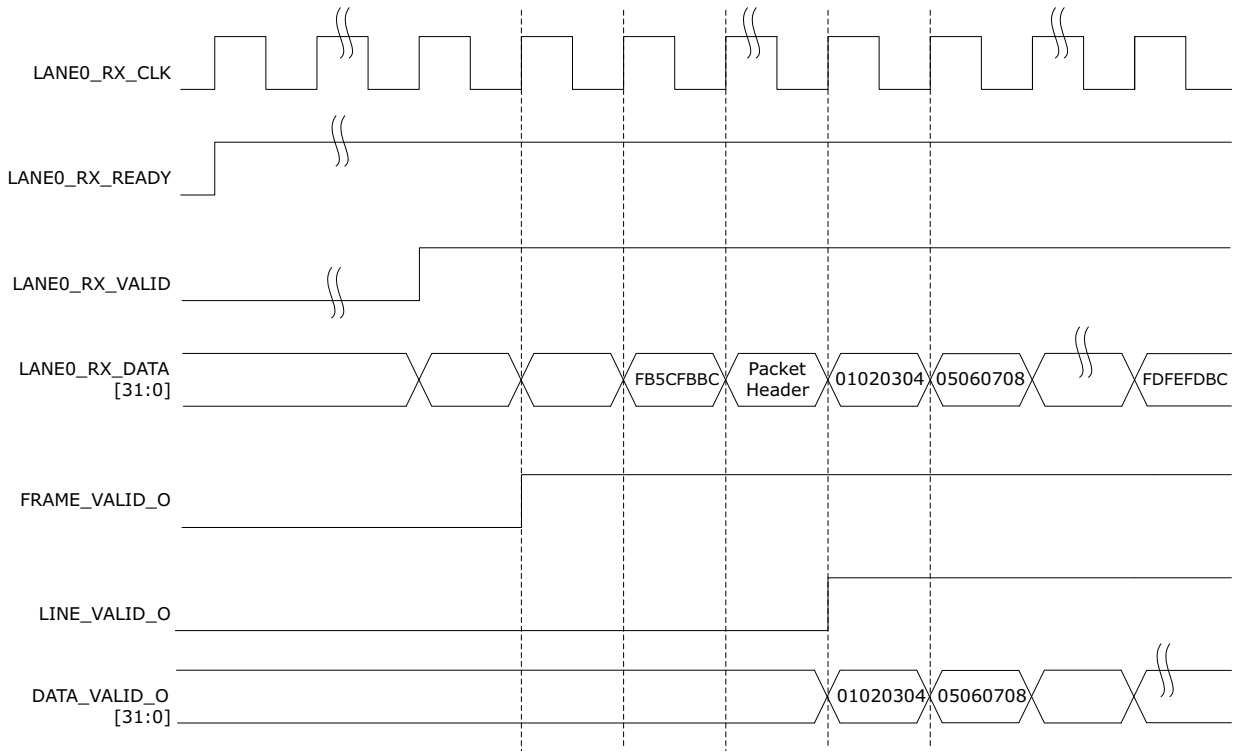
Table 4 • **Input and Output Ports**

Signal Name	Direction	Width	Description
LANE#_RX_CLK	Input	1	Recovered clock from the transceiver for that particular Lane
LANE#_RX_READY	Input	1	Data ready signal for Lane
LANE#_RX_VALID	Input	1	Data Valid signal for Lane
LANE#_RX_DATA	Input	32	Lane recovered data from transceiver
LINE_VALID_O	Output	1	Data valid signal for active pixels in a line
FRAME_VALID_O	Output	1	Valid signal for Active lines in a frame
DATA_OUT_O	Output	LANE_WIDTH*32	Pixel data output

2.4 Timing Diagram

The following figure shows the SLVS-EC IP timing diagram.

Figure 9 • **SLVS-EC IP Timing Diagram**



2.5 Resource Utilization

The following table shows the resource utilization of a sample SLVS-EC Receiver Core implemented in a PolarFire FPGA (MPF300TS-1FCG1152I package), for RAW8 and 2-lane configuration.

Table 5 • **Resource Utilization**

Element	Usage
DFFs	1645
4-input LUTs	1020
LSRAMs	13