UG0862

User Guide
HDMI TX

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document.

2 Introduction

Microsemi's High-Definition Multimedia Interface (HDMI) transmitter IP supports transmitting video data described in the HDMI standard specification.

HDMI TX IP features are:

- Supports HDMI 2.0 and HDMI 1.4
- Supports 1, 2, and 4 pixels per clock input
- Supports 8-bits color depth
- Supports up to 4K resolutions of 4096x2160 at 60 Hz
- Supports Encoding Scheme - TMDS

HDMI is a high-speed, serial, digital signaling system that is designed to transmit large amounts of digital data over a long cable length. To achieve these goals, HDMI utilizes Transition Minimized Differential Signaling (TMDS), which is optimized for robust digital data transmission.

A TMDS link consists of a single clock channel and three data channels. The video pixel clock is transmitted on the TMDS clock channel, which helps to keep the signals in synchronization. Video data is carried as 24-bit pixels on the three TMDS data channels, where each data channel is designated for red, green, and blue color component.

TMDS encoder allows transmitting serial data at a high speed, while minimizing potential for EMI (Electro-Magnetic Interference) over copper cables by minimizing the number of transitions (reducing interference between channels), achieves DC balance, on the wires, by keeping the number of ones and zeros, on the line nearly equal.

HDMI TX IP is designed to be used along with PolarFire device transceivers. The IP is compatible with HDMI 1.4 and HDMI 2.0 and supports up to 60 frames per second with a maximum bandwidth of 18 Gbps. The IP uses TMDS encoder that converts the 8 bits per channel into the 10-bit DC-balanced, transition minimized sequence, which is then transmitted serially at a rate of 10 bits per pixel per channel on the video data period. During the video blanking period, control tokens are transmitted that are generated based on hsync and vsync signals.

The control tokens can have one of the four predefined values:

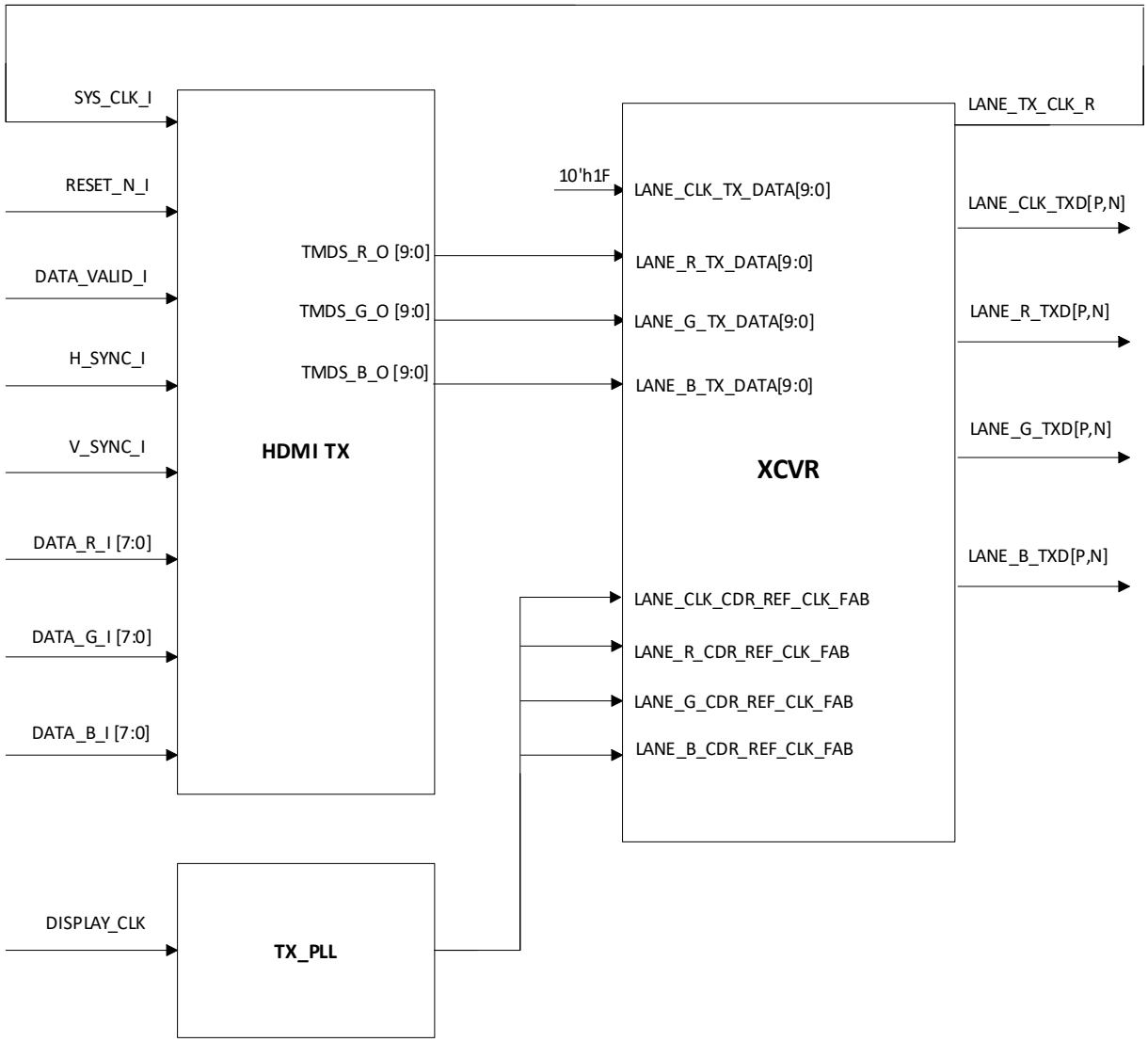
10'b1101010100, 10'b0010101011, 10'b0101010100, and 10'b1010101011. Control data characters are designed to have a large number (7) of transitions to help the receiver synchronize its clock with the transmitter clock.

The HDMI TX IP can process the data at 1, 2, or 4 pixels per clock. When the IP operates in 2 or 4 pixels per clock, it also produces the output in the form of two or four encoded pixels per clock.

3 Hardware Implementation

The following figure illustrates the HDMI TX IP in 1 pixel mode for PolarFire devices:

Figure 1 • **HDMI TX IP Block Diagram**



In the TMDS encoder, the first stage is an XOR/XNOR operation, which minimizes the number of transitions, and the second stage is an INV/NONINV, which minimizes the disparity (DC balance). The extra two bits are added at this stage of operation. Control data (hsync and vsync) is encoded to 10 bits in 4 possible combinations to help the receiver synchronize its clock with the transmitter clock. A Transceiver should be used along with the HDMI TX IP to serialize the 10 bits (1 pixel mode) or 40 bits (4 pixels mode).

4 Inputs and Outputs

4.1 Ports

The following table describes the input and output ports of HDMI TX IP.

Table 1 • **Inputs and Outputs**

Signal Name	Direction	Width	Description
SYS_CLK_I	Input	1 bit	System clock, usually the same clock as the display controller
RESET_N_I	Input	1 bit	Asynchronous active low reset signal.
DATA_VALID_I	Input	1 bit	Data valid input • 1 for video data • 0 for control data
H_SYNC_I	Input	1 bit	Horizontal sync pulse
V_SYNC_I	Input	1 bit	Vertical sync pulse
DATA_R_I	Input	[g_PIXELS_PER_CLK * 8 - 1: 0]	Input “R” data
DATA_G_I	Input	[g_PIXELS_PER_CLK * 8 - 1: 0]	Input “G” data
DATA_B_I	Input	[g_PIXELS_PER_CLK * 8 - 1: 0]	Input “B” data
TMDS_R_O	Output	[g_PIXELS_PER_CLK * 10 - 1: 0]	Encoded “R” data
TMDS_G_O	Output	[g_PIXELS_PER_CLK * 10 - 1: 0]	Encoded “G” data
TMDS_B_O	Output	[g_PIXELS_PER_CLK * 10 - 1: 0]	Encoded “B” data

4.2 Configuration Parameters

The following table describes the configuration parameters in the HDMI TX IP.

Table 2 • **Configuration Parameters**

Parameter Name	Description
g_PIXELS_PER_CLK	Number of pixels per clock input if g_PIXELS_PER_CLK = 1, input data width = 8, output data width = 10 if g_PIXELS_PER_CLK = 2, input data width = 16, output data width = 20 if g_PIXELS_PER_CLK = 4, input data width = 32, output data width = 40

4.3 Testbench Simulation

Testbench is provided to check the functionality of HDMI TX core. The following table describes the parameters, that are configured according to application.

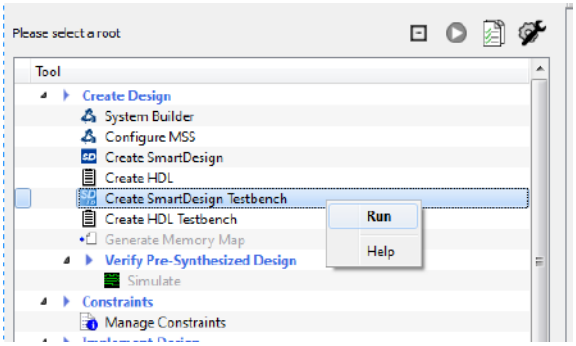
Table 3 • **Testbench Configuration Parameter**

Name	Description
g_PIXELS_PER_CLK	Number of pixels per clock input

The following steps describe how to simulate the core using the testbench:

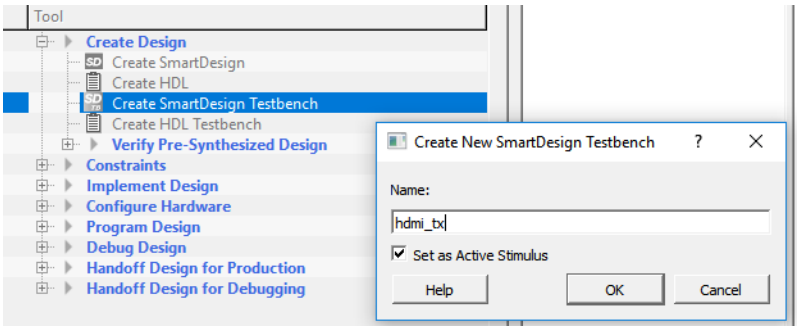
1. In the **Design Flow** window, expand **Create Design**.
2. Right-click **Create SmartDesign testbench** and click **Run.** See the following figure:

Figure 2 • **Creating SmartDesign Testbench**



3. Enter a name for the SmartDesign testbench, and click **OK**.

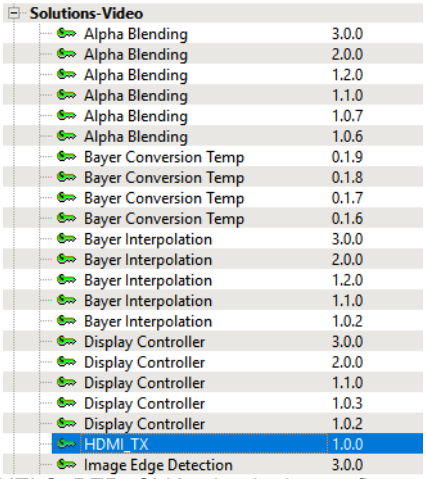
Figure 3 • **Naming SmartDesign Testbench**



SmartDesign testbench is created, and a canvas appears to the right of the Design Flow pane.

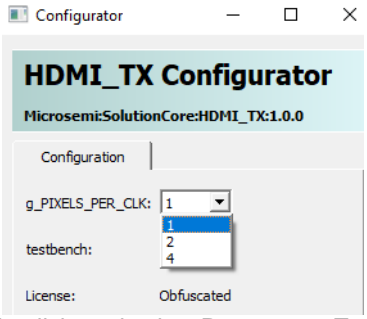
4. In the **Libero SoC Catalog** (**View > Windows > Catalog**), expand **Solutions-Video**, and drag the **HDMI TX IP** core onto the SmartDesign testbench canvas.

Figure 4 • **HDMI TX in Libero SoC Catalog**



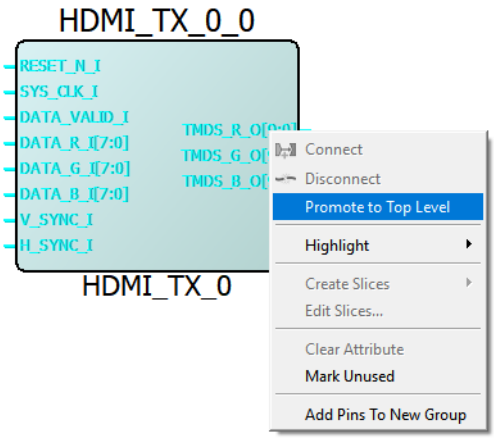
5. Select required g_PIXELS_PER_CLK value in the configurator window as shown below.

Figure 5 • **Parameter Configuration**



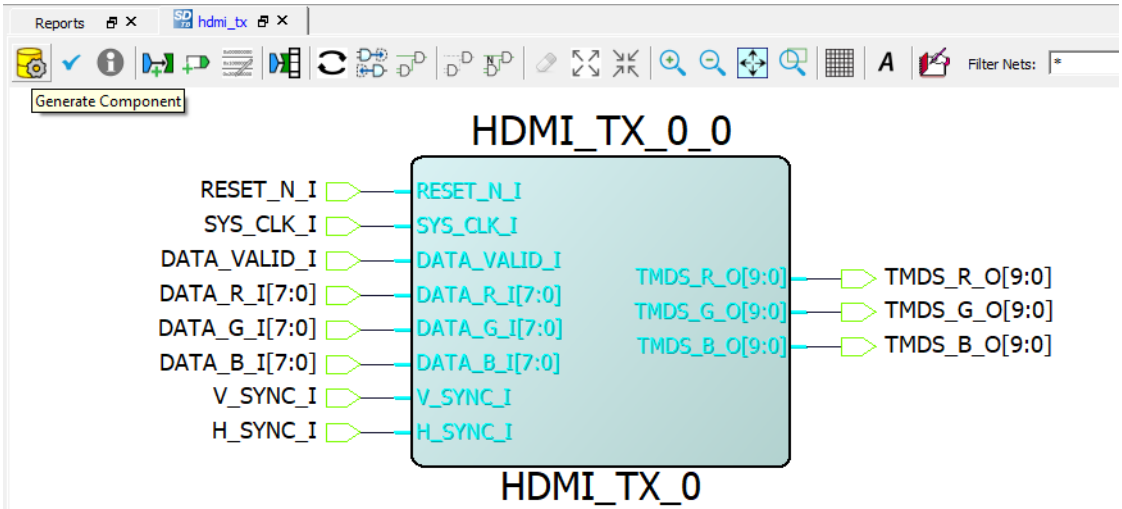
6. Select all the ports. Right-click, and select **Promote to Top Level**, as shown in the following figure.

Figure 6 • **Promote to Top Level**



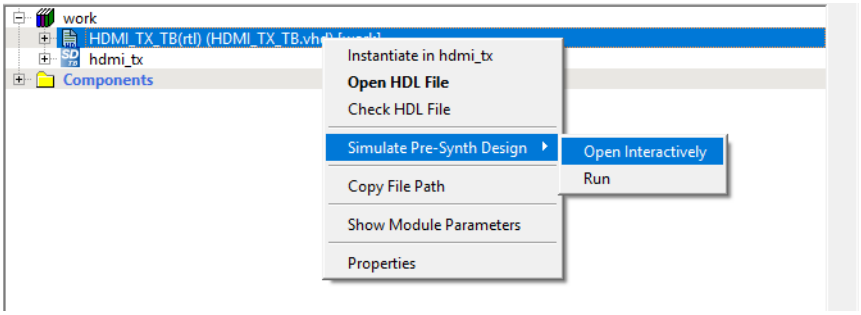
7. Click **Generate Component** from the SmartDesign toolbar, as shown in the following figure.

Figure 7 • **Generate Component**



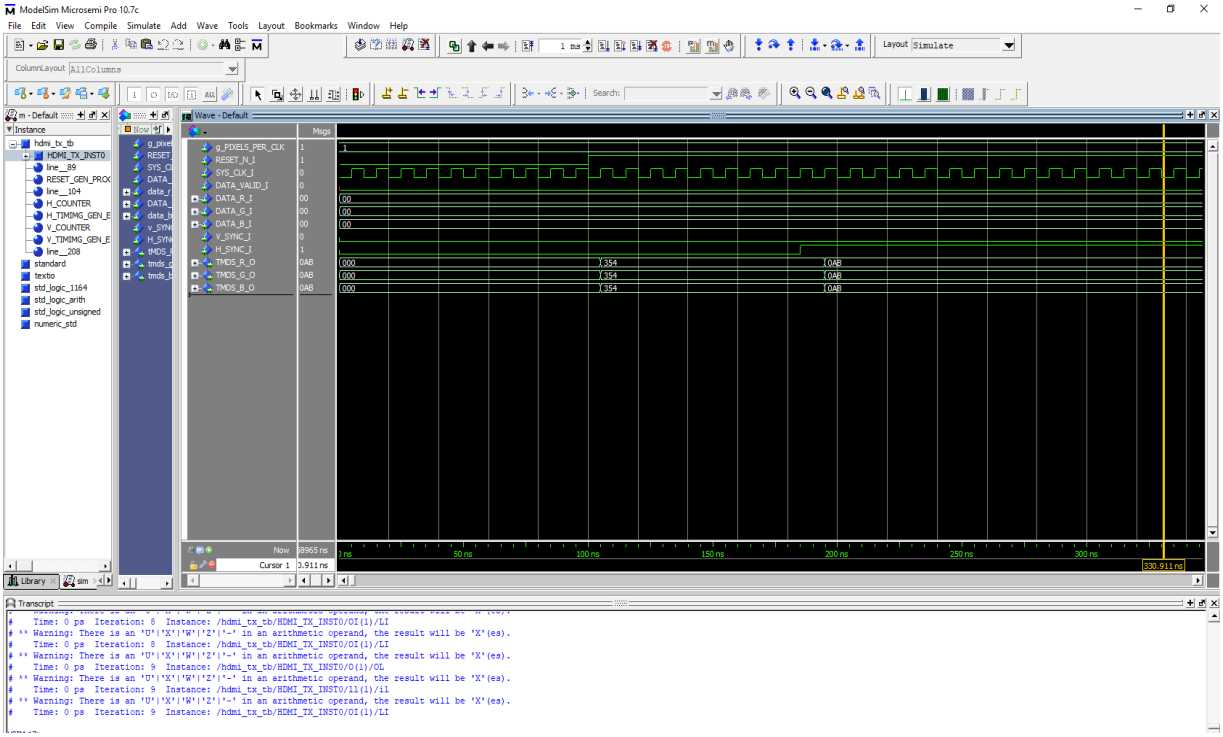
8. On the **Stimulus Hierarchy** tab, right-click HDMI_TX_TB testbench file, and click **Open Interactively** from Simulate Pre-Synth Design.

Figure 8 • **Simulating Testbench**



The ModelSim tool appears with the test bench file loaded on to it as shown in the following figure.

Figure 9 • **ModelSim Tool with HDMI TX Testbench File**

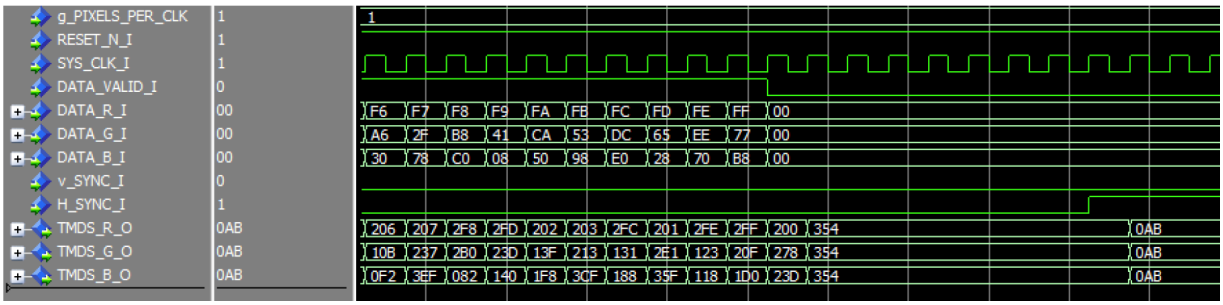


If the simulation is interrupted because of the runtime limit in the DO file, use the run -all command to complete the simulation.

4.4 Timing Diagrams

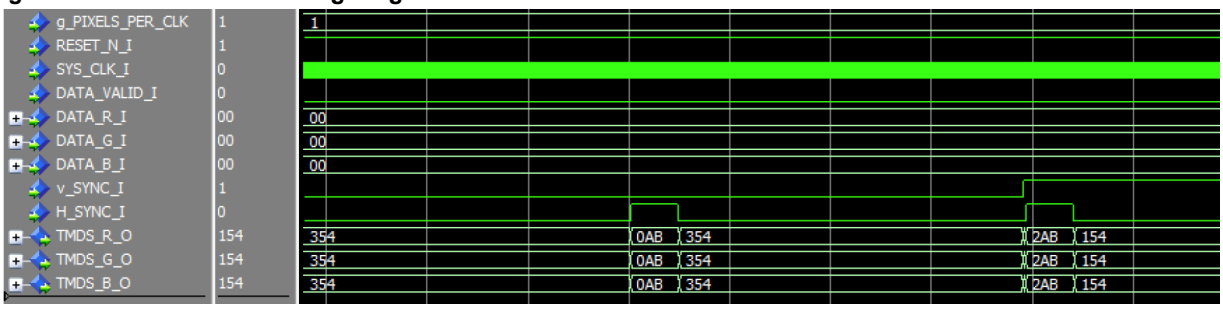
The following timing diagram for HDMI TX IP shows video data and control data periods for 1 pixel per clock.

Figure 10 • **HDMI TX IP Timing Diagram of Video Data for 1 Pixel Per Clock**



The following diagram shows the 4 combinations of control data.

Figure 11 • **HDMI TX IP Timing Diagram of Control Data for 1 Pixel Per Clock**



4.5 Resource Utilization

HDMI TX IP is implemented in PolarFire FPGA (MPF300T - 1FCG1152I Package). The following table describes the resources utilized by the FPGA, when pixels per clock = 1.

Table 4 • **Resource Utilization for 1 Pixel Per Clock**

Resource	Usage
DFFs	42
4LUTs	250

The following table describes the resources utilized by the FPGA, when pixels per clock = 4.

Table 5 • **Resource Utilization for 4 Pixels Per Clock**

Resource	Usage
DFFs	168
4LUTs	1100