UG0875 User Guide
CoaXPress IP

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of the document.

2 Introduction

2.1 Overview

CoaXPress is an interface to connect Devices (typically cameras) to Hosts (typically frame grabbers), it consists of one master connection and optional extension connections, which together forms a link. In CoaXPress v1.1 protocol, each connection supports up to 6.25 Gbps data rate.

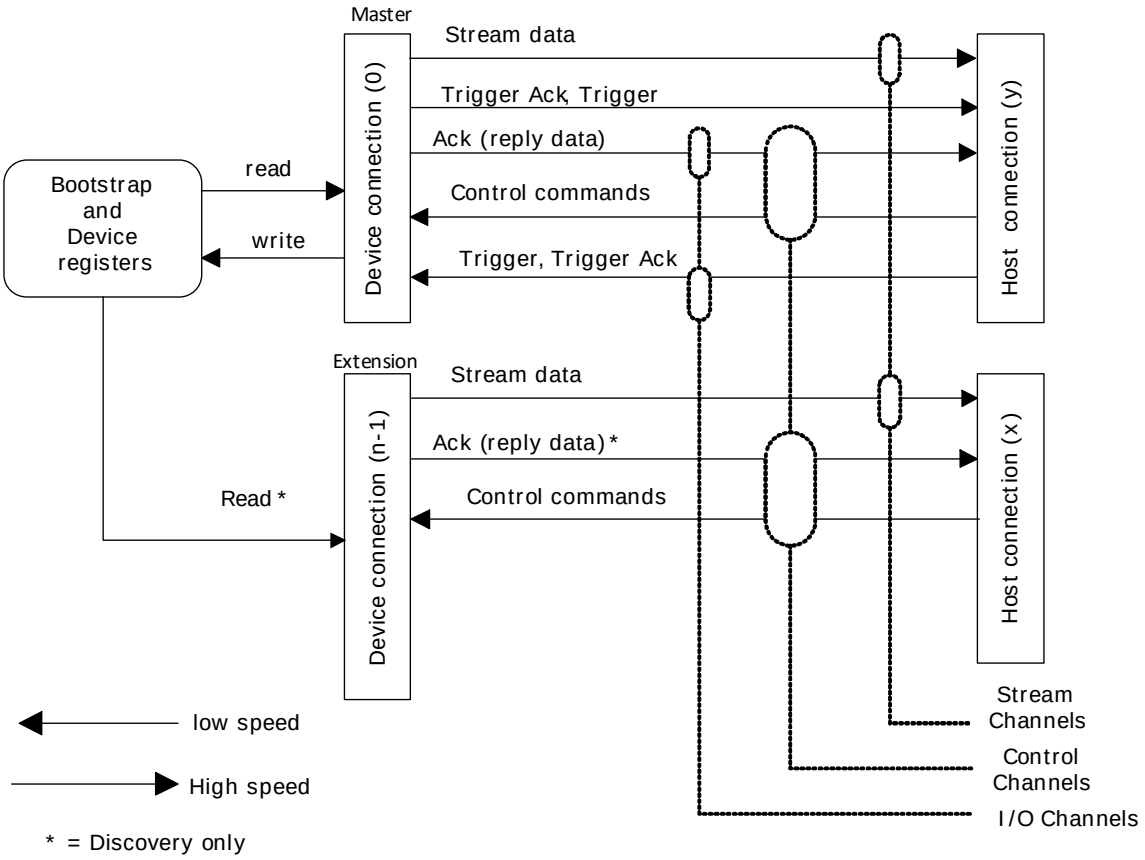
The link consists of downconnection and upconnection. The link direction from Device to Host is downconnection, and the link direction from Host to Device is upconnection. Upconnection could be low speed upconnection or high speed upconnection. Low speed upconnection rate is 20.83 Mbps, while high speed downconnection or high speed upconnection rate could be: 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, or 6.25 Gbps.

Within one connection pair, both the upconnection and downconnection are transmitted on the same coax cable. For each connection, CoaXPress defines a set of logical channels to carry specific data frame:

- Stream data on stream channel (for example, image data from Device to Host)
- Real time triggers on IO channel (A trigger event occurs when a triggers frame received)
- Device control on Control channel (frames from Host to read and write Device control registers)

The following figure shows the logical channel diagram when high speed up connection is not available.

Figure 1 • **Link Diagram without High Speed Upconnection**



In the preceding diagram, Stream data is transmitted on stream channel, which is high speed downconnection from Device to Host. Trigger frame includes bidirectional Trigger and bidirectional Trigger Ack. Host transmits,Trigger and Trigger Ack on low speed master upconnection while the Device

transmits, Trigger and Trigger Ack on high speed master downconnection. On Master connection, the Host transmits Control commands on low speed upconnection, which can read and write the device registers. The Device transmits registers, Control Command Acknowledgment from Device is transmitted on high speed downconnection. On extension connection, Control commands and Ack are the same as Master connection, except for Control commands are only able to read Device in Device Discovery process.

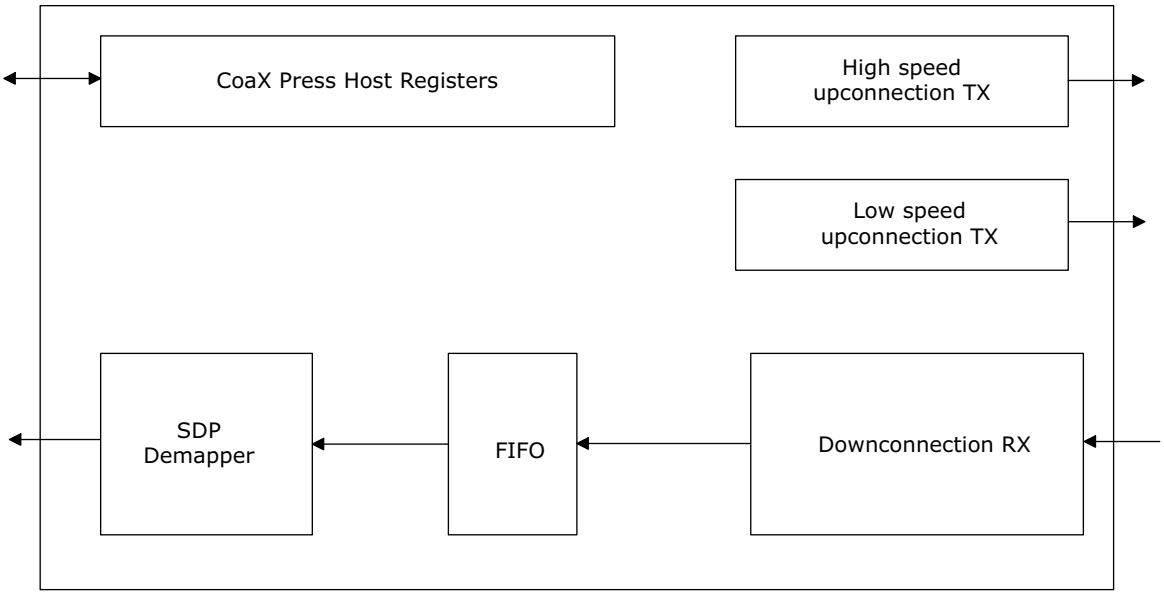
When high speed upconnection is available, the master link upstream function is moved to high speed upconnection.

CoaXPress IP implements the link layer defined in CoaXPress v1.1 standard. CoaXPress includes CoaXPress Host IP and CoaXPress Device IP.

2.2 CoaXPress Host IP Architecture

The following figure shows the diagram of CoaXPress Host IP implementation:

Figure 2 • **CoaXPress Host IP Implementation Diagram**



As show in the preceding diagram, CoaXPress Host IP includes downconnection RX module, SDP demapper, low speed upconnection TX module, and optional high speed upconnection TX module.

Downconnection RX module receives packets in downconnection channel. The stream data packet and markers are forwarded to SDP demapper, the Command Acknowledgment packets are buffered for the software reading.

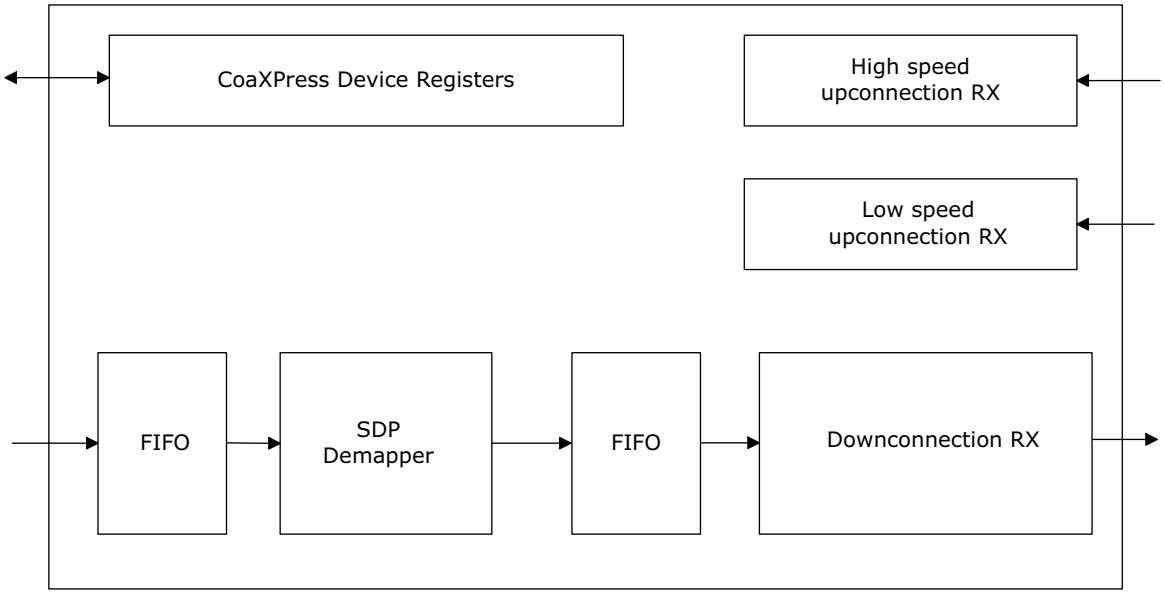
The upconnection TX modules transmit Control Command packet from the software configuration, and it also transmit Trigger and Trigger Ack.

The SDP demapper gets image line packets from stream data packets payload section, it sends the image line packets to downstream module. It also forwards the frame markers and line markers to downstream module.

2.3 CoaXPress Device IP Architecture

The following figure shows the diagram of CoaXPress Device IP implementation:

Figure 3 • **CoaXPress Device IP Implementation Diagram**



As shown in the preceding diagram, CoaXPress Device IP includes downconnection TX module, SDP mapper, low speed upconnection RX module, and optional high speed upconnection RX module.

The SDP mapper generates stream data packets with image line packets as payload, it also forwards the input frame marker and line marker to downconnection TX module.

The downconnection TX module is downconnection transmitter, it transmits stream data packets, markers, Command Acknowledgment packets, Trigger and Trigger Ack packets.

High speed upconnection RX and low speed upconnection RX module receives Trigger packets and Control Command packets from CoaXPress Host.

2.4 Key Features

CoaXPress IP features are:

- Only single lane mode.
- Supports high speed upconnection.
- Supports up to 6.25 Gbps on downconnection and high speed upconnection.
- Supports 20.83 Mbps low speed upconnection.
- Meets the requirements in CoaXPress V1.1
- Including CoaXPress Host IP and CoaXPress Device IP.

2.5 Resource Utilization

The following table describes the resource utilization in which CoaXPress IP is implemented in PolarFire device:

Table 1 • **CoaXPress IP Resource Utilization**

	LUT	DFF	uSRAM	LSRAM
CoaXPress Host IP	4040	3530	0	5
CoaXPress Device IP	4400	4420	0	7

3 Function Description

3.1 Image Packet Transmission

CoaXPress Device IP accepts image packets from camera. Each line packet is wrapped into a stream data packet. Also, the frame marker and line marker are required. The frame marker and line marker are transmitted transparently to CoaXPress Host.

The following table describes the stream data packet:.

Table 2 • **Stream Data Packet Format**

Word	Content	Description
	4x K27.7	Start of packet indication (see section 8.4).
	4x 0x01	Stream data packet indication.
0	4x Stream ID	Unique stream ID that this packet contains data for.
1	4x Packet Tag	8 bit tag. Incremented for each packet with this stream data words N per packet.
2	4x DsizeP (15:8)	16 bit value representing the number of stream data words N per packet.
3	4x DsizeP (7:0)	
4 to N+3	Stream data	N words of stream data.
N+4	CRC	32-bit CRC calculated over the stream data 4 to (N+3).
	4x K29.7	End of packet indication.

There is a register sdp_payload_max_len, which controls the maximal length of stream data packet payload. Reset or power up, sdp_payload_max_len is set to 0 (zero), by default, which means stream data packet transmission is disabled. To enable stream data packet transmission, user need to set a proper value after link initialization, and ensure that, a complete image line packet is mapped into one stream data packet.

To support a flexible frame marker and line marker solution, user need to generate the complete frame marker and line marker and send to CoaXPress Device IP. CoaXPress Device IP would not modify any marker bits or field and transmit it transparently.

There is a FIFO to buffer the input image line packet or marker, and it calculates the input packet length and drops the packet with wrong length or error condition. User need to set a right FIFO depth and ensure that it buffers at least 2 image line packets.

In stream data packet transmission process, CoaXPress Device IP counts, how many packets are transmitted, the software reads this counter value.

CoaXPress Host IP receives data stream from CoaXPress Device, it recognizes stream data packet and frame/line markers. To support a flexible frame/line marker solution, user can define the marker header and code by setting the register marker_header_word, the host IP recognizes the markers according to this setting.

For stream data packets, the CoaXPress Host IP determines if there is any error, the error case includes CRC error, TAG error, and length error. All these error cases can be read by the software. CoaXPress Host IP also counts how many stream data packets have been received. The stream data packets overhead including header and trailer are removed, and CoaXPress Host IP outputs the stream data packet payload to downstream module.

For frame markers and line markers, CoaXPress Host IP does not modify any field or bit and output the complete marker to downstream module.

3.2 Trigger and Trigger Ack

CoaXPress IP supports 2-way directions of trigger and trigger Ack, from host to device, and from device to host.

For CoaXPress Host IP upconnection transmitter and CoaXPress Device IP downconnection transmitter, both provide an input port to accept external trigger signal. The input trigger falling edge generates a Falling Trigger transmission, while the input trigger rising edge generates a Rising Trigger transmission.

After receiving a Trigger frame, a Trigger Ack frame should be send immediately. The Trigger receiver provides an output port to recovery the received Trigger event, a received Rising Trigger generates a rising edge on this port, while a received Falling Trigger generates a falling edge on this port. The Trigger receiver includes Host downconnection receiver, device low-speed upconnection receiver and device high-speed upconnection receiver.

For CoaXPress Device IP, high speed downconnection transmitter is responsible for Trigger and Trigger Ack transmission. For CoaXPress Host IP, low speed upconnection transmitter is responsible for Trigger and Trigger Ack transmission when high speed upconnection is not available, else, Trigger and Trigger Ack is transmitted on high speed upconnection.

The following table shows the high-speed Trigger frame format:

Table 3 • **High Speed Trigger Format**

Word	Content	Description
0	Either 4x K28.4	Trigger packet indication - rising edge
	or 4x K28.4	Trigger packet indication - falling edge
1	4x Delay	The delay value is three minus the number of whole characters between the trigger event and the start of this trigger packet. Usage is optional, when it is not set to 0.

The following table shows the low-speed Trigger frame format:

Table 4 • **Low Speed Trigger Format**

Char	Content	Description
0-2	Either K28.2 K28.4 K28.4	Trigger packet indication - rising edge
	or K28.2 K28.2 K28.2	Trigger packet indication - falling edge
3-5	3x Delay	The delay value is 239 minus the number of units of 1/24 the low speed connection bit interval (2.00 ns) between the trigger event and the start of the trigger packet. The host uses a coarser time unit by setting lower bits of this value fixed at 0 or giving it a bias. The Device uses a coarser time unit by using less bits of this value (discard non used lower bits of this value or use rounding) The chosen accuracy and usage of this timing correction value is left as a quality of implementation at both the Host and the Device.

The following table shows the Trigger Ack frame format:

Table 5 • **Trigger Ack Format**

Word	Content	Description
0	4x 28.6	I/O acknowledgment packet indication
1	4x Code	Acknowledgment code, repeated 4 times: 0x01 Trigger packet received OK

Trigger and Trigger Ack have the highest priority transmission order. On high speed connection, they can be insert at any word boundary. On low speed connection, they can be insert at any character boundary.

After the transmission of a Trigger, the transmitter is waiting for a Trigger Ack in a defined time, which is configured by user. If there is no Trigger Ack in defined time, then the transmitter might resend a previous Trigger, or send a new trigger when a new trigger event occurs. The maximal resending trigger times is configured by user.

CoaXPress Host and Device count how many Trigger and Trigger Ack have been transmitted or received, the software can read these counters for debugging purpose.

3.3 Control Channel

The control channel provides register access through specific control commands, transmitted from Host to Device, and the resulting acknowledgment messages, transmitted from the Device to the Host.

The software is responsible to generate control commands and control acknowledgment messages. In each high-speed or low-speed connection transmitter, the CoaXPress Host and Device IP provides a buffer to accept packets from the software configuration, and the packets are transmitted when the configuration is completed, and transmitter is not transmitting other packets.

When received a control command or control acknowledgment, CoaXPress IP writes the received packet into buffer and allows the software to know a received control packet is available for reading. The software must check, if there is available packet and reads it out.

In summary, every transmitter has a buffer to accept control packets generated in the software for transmission, and every receiver has a buffer to storage received control packets and give instruction to the software to read the received packet out.

The CoaXPress Host IP and Device IP only send and receive control packet, the software is responsible for the following items:

- Generate control commands in CoaXPress Host.
- Generate control acknowledgment in CoaXPress Device.
- Checking if the received control packet is error free.
- Determine if the acknowledgment is timeout and resend the control command if necessary.

Refer to section “Writing and Reading Control Packet” to get the details of reading and writing control packets.

3.4 Connection Test

The CoaXPress Host and Device IP provides connection test to test the quality of the connection. For each connection, the transmitter includes a test frame generator, and the receiver includes a test frame receiver.

The following table shows the test frame format:

Table 6 • **Test Frame Format**

	Content				
Word	**P0**	**P1**	**P2**	**P3**	**Description**
	K27.7	K27.7	K27.7	K27.7	Start of packet indication (see section 8.4).
	0x04	0x04	0x04	0x04	Connection test indication.
0	0x00	0x01	0x02	0x03	Test data
1	0x04	0x05	0x06	0x07	
...					
63	0xFC	0xFD	0xFE	0xFF	
64	0X00	0X01	0X02	0X03	
...					
1023	0XFC	0XFD	0XFE	0XFF	
	K29.7	K29.7	K29.7	K29.7	End of packet indication.

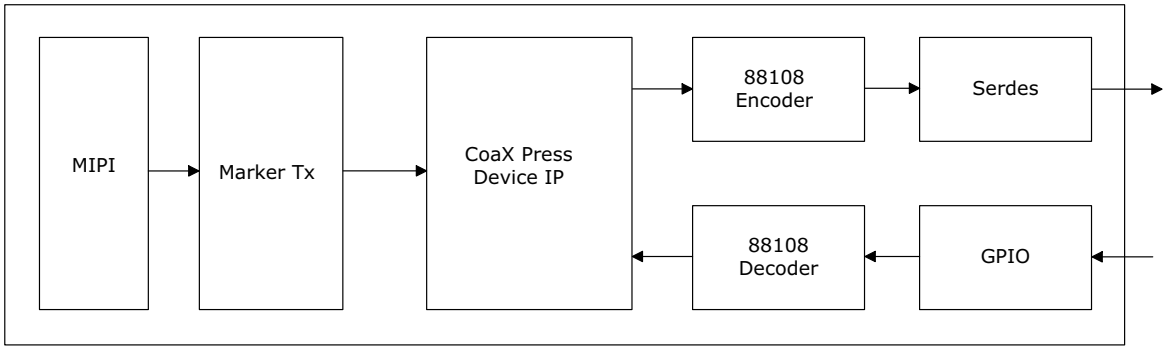
Prior to starting CoaXPress communication between Host and Device, user can start run connection test for each connection channel. There is a register control test frame transmission for each connection transmitter. Connection transmitter counts how many test frames are sent, and connection receiver counts how many test frames are received.

4 Typical Application

4.1 Device IP Application

The following diagram describes a typical CoaXPress Device IP application:

Figure 4 • **Typical Application for CoaXPress Device IP**



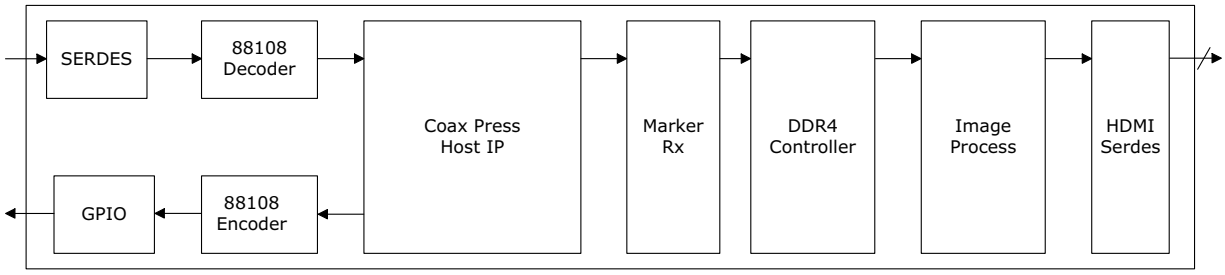
As described in the preceding diagram, MIPI interface gets image frames and lines from external camera, Marker Tx module generates frame marker at the starting of each frame and generates line marker at the starting of each line, it also forwards the line data to CoaXPress Device IP. CoaXPress Device IP transmit the line data packet in stream data packet with frame/line marker on downconnection. The downconnection data is encoded to 10B data and transmitted on Serdes. On upconnection, the data from 20.83 Mbps GPIO is decoded to 8B data in 8B10B decoder, CoaXPress Device IP gets 8B upconnection data and recognizes the packets on upconnection.

If quick trigger and control channel are required, the high-speed upconnection should be added. In this case, upconnection packets are transmitted on high-speed upconnection when it is established.

4.2 Host IP Application

The following diagram describes a typical CoaXPress Host IP application:

Figure 5 • **Typical Application for CoaXPress Host IP**



As described in the preceding diagram, this application gets data packets from CoaXPress cable, and it send data to HDMI interface.

Serdes gets downconnection data from CoaXPress device and decode it to 8B data. CoaXPress Host IP processes all the packets in downconnection data stream, the frame/line marker and image line data packets are extracted from stream data packet, the Marker Rx module forwards image line data packets to DDR4. DDR4 reading data is sending to HDMI interface after image signal processing.

On the Host upconnection direction, the CoaXPress Host IP generates Trigger, Trigger Ack, and Control Command packets, upconnection data stream is coded to 10B code in 8B10B encoder. The 10B data is transmitted on a GPIO port to CoaXPress Device.

If quick trigger and control channel is required, the high-speed upconnection should be added. In this case, upconnection packets are transmitted on high-speed upconnection when it is established.

5 CoaXPress Host IP Interface Singles

5.1 Interface

CoaXPress IP includes Host IP and Device IP. The following table shows the input and output ports for CoaXPress Host IP:

Table 7 • **CoaXPress Host IP Interface Signals**

Interface	Direction	Description
tx_rst_n_i	Input	Low active reset signal with tx_clk_i synchronization.
tx_clk_i	Input	Host transmitter clock.
rx_rst_n_i	Input	Low active reset signal with rx_clk_i synchronization.
rx_clk_i	Input	Host receiver clock.
clk_mod_i	Input	Indicates the tx_clk_i and rx_clk_i frequency. 0 means 125 Mhz 1 means 156.25 Mhz 2 means 250 Mhz 3 means 312.5 Mhz
addr_i	Input	Reading and writing internal registers interface: address.
cs_i	Input	Reading and writing internal registers interface: select enable, high active.
wen_i	Input	Reading and writing internal registers interface: write enable, high active.
ren_i	Input	Reading and writing internal registers interface: read enable, high active.
wdata_i	Input	Reading and writing internal registers interface: writing data.
rdata_o	Output	Reading and writing internal registers interface: reading data.
rdval_o	Output	Indicates if data on rdata_o port is active or available.
trigger_i	Input	Input trigger signal. Host generate Trigger packet if rising or falling edge event occurs on this port.
trigger_o	Output	Recovery trigger signal. Host generate a rising edge on this port, if a Rising Trigger packet received and generates a falling edge on this port, if a falling Trigger packet received.
lsuc0_tx_dval_o	Output	Indicates, if Low-Speed upconnection data is available.
lsuc0_tx_data_o	Output	Low-Speed upconnection data.
lsuc0_tx_k_o	Output	Low-Speed upconnection data K character indication.
hsuc_tx_k_o	Output	High-Speed upconnection data K character indication.
hsuc_tx_data_o	Output	High-Speed upconnection data.
hsdc0_rx_k_i	Input	Downconnection K character indication.
hsdc0_rx_data_i	Input	Downconnection data.
ipkt_data_val_o	Output	Indicates, if data on ipkt_data_o is available.
ipkt_data_sop_o	Output	Starting of image line packet or marker indication.
ipkt_data_eop_o	Output	End of image line packet or marker indication.
ipkt_data_len_o	Output	Image line packet or marker length.
ipkt_data_k_o	Output	Image line packet or marker data K character indication.

Table 7 • **CoaXPress Host IP Interface Signals**

Interface	Direction	Description
ipkt_data_o	Output	Image line packet or marker data.

5.2 Configuration Parameters

The following table describes the configuration parameters for CoaXPress Host IP:

Table 8 • **Configuration Parameters for CoaXPress Host IP**

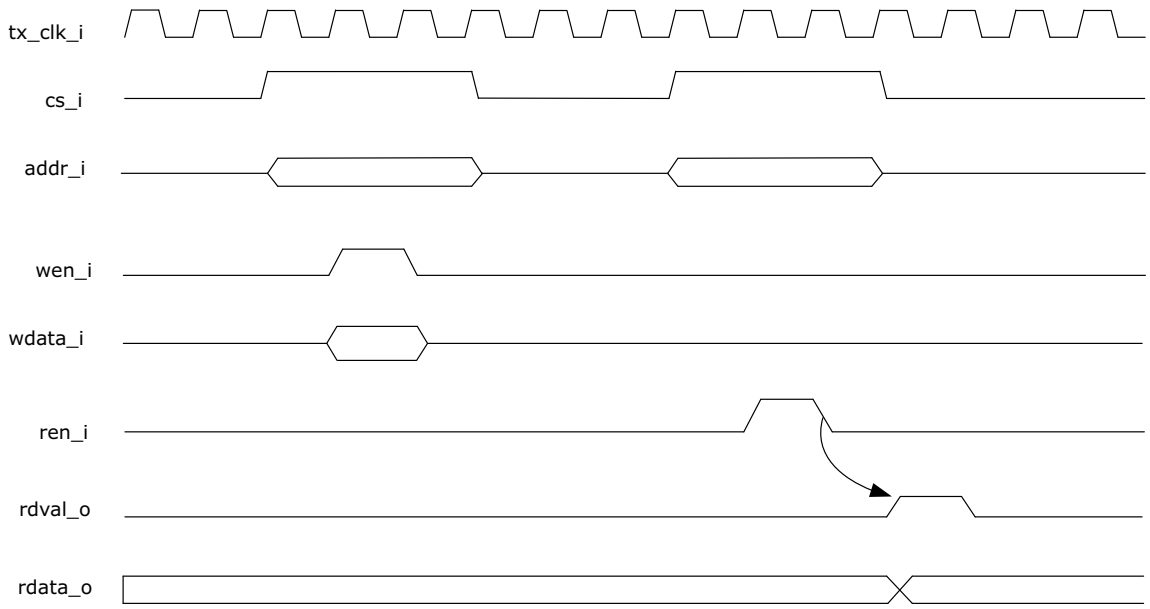
Name	Default	Description
g_TX_CMD_FIFO_DEPTH	128	Control Command transmitter FIFO depth, the FIFO data width is 32 bits. It should be able to buffer at least 1 maximal Control Commend packet from the software configuration.
g_TX_CMD_FIFO_ADDR_WID	7	Control Command transmitter FIFO address width.
g_RX_CMD_ACK_FIFO_DEPTH	128	Control Acknowledgment receiver FIFO depth, the FIFO data width is 32 bits. It should be able to buffer at least 1 maximal Control Acknowledgment packet from Device.
g_RX_CMD_ACK_FIFO_ADDR_WID	7	Control Acknowledgment receiver FIFO address width.
g_RX_CONN_FIFO_DEPTH	1024	Downconnection FIFO depth, data width is 32 bits, it should be able to buffer at least 2 maximal stream data packets.
g_RX_CONN_FIFO_ADDR_WID	10	Downconnection FIFO address width.
g_HSUC_EN	0	High Speed Upconnection enable or disable.

5.3 Key Interface Description

5.3.1 Reading and Writing Register Interface

The following figure shows the timing diagram of the Reading and Writing Internal Register Interface:

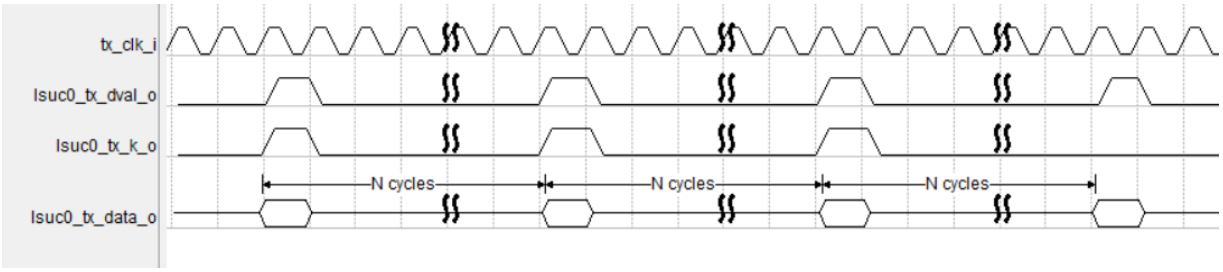
Figure 6 • **Timing diagram for Reading and Writing Host IP Registers Interface**



5.3.2 Low-Speed Upconnection Transmitter Interface

The following figure shows the timing diagram of Low Speed Upconnection Transmitter Interface:

Figure 7 • **Timing Diagram for Low Speed Upconnection Transmitter Interface**

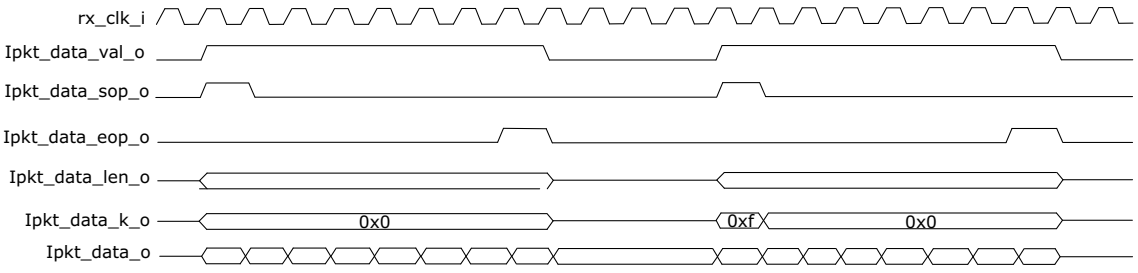


Low speed upconnection transmitter outputs 1 valid data every 480ns. If tx_clk_i frequency is 156.25 Mhz, then it means it outputs 1 valid data every 75 clock cycles.

5.3.3 Image packet output Interface

The following figure shows the timing diagram of image packet output interface:

Figure 8 • **Timing Diagram for Low Speed Upconnection Transmitter Interface**



This interface outputs, image line packet and markers packets including frame marker and line marker. User need to design a downstream module to receive marker packets.

6 CoaXPress Device IP Interface Singles

6.1 Interface

The following table shows the input and output ports for CoaXPress Device IP:.

Table 9 • **CoaXPress Device IP Interface Signals**

Interface	Direction	Description
tx_rst_n_i	Input	Low active reset signal with tx_clk_i synchronization.
tx_clk_i	Input	Device transmitter clock.
rx_rst_n_i	Input	Low active reset signal with rx_clk_i synchronization.
rx_clk_i	Input	Device receiver clock.
lsuc_rst_n_i	Input	Low active reset signal with tx_clk_i synchronization.
lsuc_clk_i	Input	Low-Speed upconnection receiver clock.
addr_i	Input	Reading and writing internal registers interface: address.
cs_i	Input	Reading and writing internal registers interface: select enable, high active.
wen_i	Input	Reading and writing internal registers interface: write enable, high active.
ren_i	Input	Reading and writing internal registers interface: read enable, high active.
wdata_i	Input	Reading and writing internal registers interface: writing data.
rdata_o	Output	Reading and writing internal registers interface: reading data.
rdval_o	Output	Indicates if data on rdata_o port is active or available.
trigger_i	Input	Input trigger signal. Host generate Trigger packet if rising or falling edge event occurs on this port.
lsuc_trigger_o	Output	Recovery trigger signal from Low-Speed upconnection.
hsuc_trigger_o	Output	Recovery trigger signal from High-Speed upconnection.
lsuc0_rx_dval_i	Input	Indicates if data on lsuc0_rx_data_i is available.
lsuc0_rx_k_i	Input	Low-Speed upconnection received data K character indication.
lsuc0_rx_data_i	Input	Low-Speed upconnection received data.
ipkt_val_i	Input	Indicates if data on ipkt_data_i is available or active.
ipkt_sop_i	Input	Indicates the starting of input image line packet or marker.
ipkt_eop_i	Input	Indicates the end of input image line packet or marker.
ipkt_marker_i	Input	Indicates if the packet is frame marker or line marker.
ipkt_k_i	Input	Indicates the ipkt_data_i K character.
ipkt_data_i	Input	Input image line data or marker data.
ipkt0_fifo_alfull_o	Output	Indicates the image line packet or marker FIFO is almost full, the previous module should pause sending data to avoid FIFO overflow.
hsdc0_tx_k_o	Output	Indicates K character on hsdc0_tx_data_o port.
hsdc0_tx_data_o	Output	Downconnection transmission data.

6.2 Configuration Parameters

The following table describes the configuration parameter for CoaXPress Device IP:

Table 10 • **Configuration Parameters for CoaXPress Device IP**

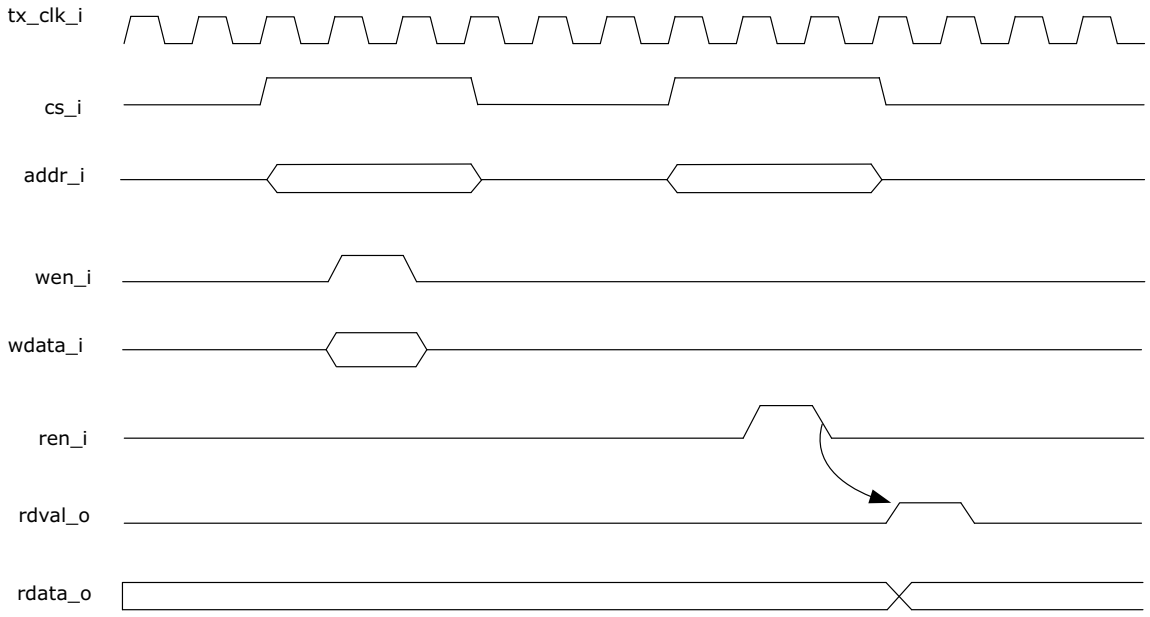
Name	Default	Description
g_TX_CMD_FIFO_DEPTH	128	Control Command transmitter FIFO depth, the FIFO data width is 32 bits. It should be able to buffer at least 1 maximal Control Commend packet from the software configuration.
g_TX_CMD_FIFO_ADDR_WID	7	Control Command transmitter FIFO address width.
g_RX_CMD_ACK_FIFO_DEPTH	128	Control Acknowledgment receiver FIFO depth, the FIFO data width is 32 bits. It should be able to buffer at least 1 maximal Control Acknowledgment packet from Device.
g_RX_CMD_ACK_FIFO_ADDR_WID	7	Control Acknowledgment receiver FIFO address width.
g_TX_CONN_FIFO_DEPTH	1024	Downconnection FIFO depth, data width is 32 bits, it should be able to buffer at least 2 maximal stream data packets.
g_TX_CONN_FIFO_ADDR_WID	10	Downconnection FIFO address width.
g_SDP_MAP_FIFO_DEPTH	1024	Stream data packet mapper input FIFO, data width is 32bits, it should be able to buffer at least maximal image line packets.
g_SDP_MAP_FIFO_ADDR_WID	10	Stream data packet mapper input FIFO address width.
g_HSUC_EN	0	High Speed Upconnection enable or disable.

6.3 Key Interface Description

6.3.1 Reading and Writing Register Interface

The following figure shows the timing diagram of Reading and Writing Internal Register Interface:

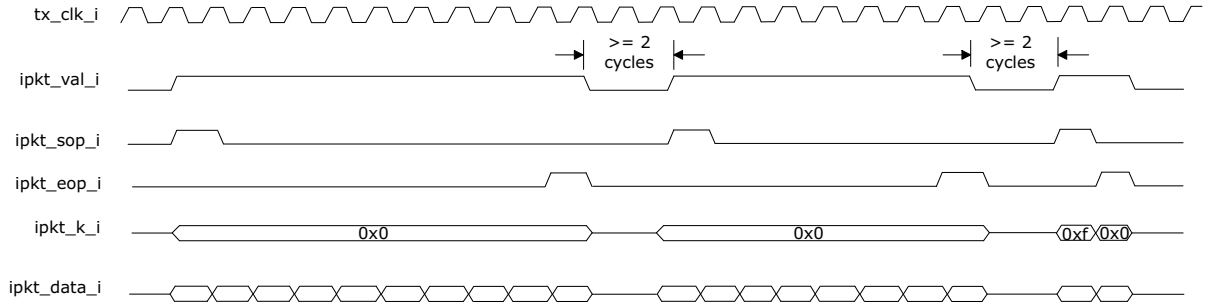
Figure 9 • **Timing Diagram for Reading and Writing Device IP Registers Interface**



6.3.2 Image packet and Marker Input Interface

The following figure shows the timing diagram of Image Packet Output Interface:

Figure 10 • **Timing Diagram for Image Packet or Marker Input Interface**



This image packer and marker input interface accepts image line packet and markers including frame marker and line marker. There should be at least two idle clock cycles between any two input packets.

User need to design a upstream module to generate complete marker packet and send markers to CoaXPress Device IP. The port ipkt_k_i should only be no-zero for marker packets, it should be constantly zero for image line packets.

7 CoaXPress Host IP Configuration Guide

7.1 Connection Test

To test high speed upconnection, software writes register 0x0009 bit [0] to 1, then read register 0x000D to know how many test frames have been transmitted. To stop high speed upconnection test function, software writes the register the address is 0x0009.

To test low speed upconnection, software writes register 0x0010 bit [0] to 1, then read register 0x0014 to know how many test frames have been transmitted. To stop low speed upconnection test function, software writes the register the address is 0x0009.

CoaXPress Host IP downconnection receiver always counts how many Test frames have been received, the software should read register 0x0097 to know it, and read register 0x0096 to know how many error test frames have been received.

7.2 Sending Control Command

In high speed upconnection transmitter and low speed upconnection transmitter, there is a Control Command FIFO to buffer Control Command packets from the software. When the packet configuration is completed, upconnection transmitter starts to Control Command Packet transmission.

The following table shows the Control Command packet format:

Table 11 • **Control Command Format**

Word	Content	Description
	4x K27.7	Start of packet indication (see section 8.4).
	4x 0x02	Control command indication.
0	Cmd	Control operation code (in character P0): Ox00 Memory read Ox01 Memory write OxFF Control channel reset Others values are reserved for future use.
	Size	24 bit value, stored in consisting of 3 characters P1, P2, and P3, that specifies the number of data bytes 8 to read or written. Eight does not include any dummy bytes for padding. This value will be 1 (at least 1 byte to read/write) except for a control channel reset when it will be 0 (zero).
1	Addr	32 bit address of the memory location to read from / write. When more than one byte must be read / write, the successive addresses are in increasing order starting from this address. Set to Ox00000000 for a control channel reset.
2 to (N-1)+2	Write Data	Data to be written. This field is omitted for a read operation (Cmd=0x00) or a control channel.
		reset (Cmd=OxFF).
		The size of this data section will be an integer number of words N, where N = Ceil(B / 4) * When 8 is not a multiple of 4, a number of dummy bytes (4 N — 8) will be padded after the last data byte. Padded dummy bytes will have the value 0 (zero).
N+2	CRC	32 bit CRC calculated over words 0 to (N+2)-1.
	4x K29.7	End of packet indication.

When generating and writing Control Command packet in the software, the 4xK27.7, 4x0x02, and 4xK29.7 words should not be writing into CoaXPress Host IP, the software must be responsible to generate all other fields from Word 0 to Word N+2.

The software must write the Control Command packet word by word, from Word 0 to Word N+2.

To write one word into high speed upconnection transmitter.Execute the following steps:

1. Set register 0x0202 bit [1] to 0.
2. Set register 0x0200 bit [1] to 1 if the writing data is Word 0, otherwise set it to 0.
3. Set register 0x0200 bit [0] to 1 if the writing data is Word N+2, otherwise set it to 0.
4. Set register 0x0201 bit [31:0] to writing data value.
5. Set register 0x0202 bit [1] to 1.

To write one word into low speed upconnection transmitter. Execute the following steps:

1. Set register 0x0202 bit [0] to 0.
2. Set register 0x0200 bit [1] to 1 if the writing data is Word 0, otherwise set it to 0.
3. Set register 0x0200 bit [0] to 1 if the writing data is Word N+2, otherwise set it to 0.
4. Set register 0x0201 bit [31:0] to writing data value.
5. Set register 0x0202 bit [0] to 1.

7.3 Reading Received Command Acknowledgment

In CoaXPress Host downconnection receiver, there is a Command Acknowledgment FIFO to buffer received Command Acknowledgment packets from CoaXPress Device. When received a complete packet, the software must read the Command Acknowledgment packet.

The following table shows the Command Acknowledgment format:

Table 12 • **Command Acknowledgment Format**

Word	Content	Description
	4x K27.7	Start of packet indication (see section 8.4).
	4x 0x03	Control acknowledge indication.
0	4x Code	Acknowledgment code (repeated 4 times): Success: Ox00 Final, command executed OK, reply data is appended. (that is acknowledgment of read command). Ox01 Final, command executed OK, No reply data is appended (that is acknowledgment of write command). 0x03 Final, control channel reset executed OK. 0x04 Waft. The time for the Host to wait will be sent as a 4 byte integer. In the reply data field, using the same packet structure as for a Ox00 acknowledgement. The value will be in milliseconds, with a range of 100ms to 10s. Logical Errors (final acknowledgments): 0x40 Invalid address. Ox41 Invalid data for the address. 0x42 Invalid control operation code. 0x43 Write attempted to a read-only address. Ox44 Read attempted from a write-only address. 0x45 Size field too large — command message (write) or acknowledgment message (read) would exceed packet size limit. 0)(46 Incorrect size received, message size is inconsistent with message size indication. 0x47 Malformed packet. Physical Errors (final acknowledgments): 0x80 Failed CRC test in last received command. Others values are reserved for future use. For all acknowledgment codes other than 0x00 or 0x04, the Length, Data, and CRC fields will be omitted and the end of packet indication will be transmitted following the acknowledgment code.
1	Size	Number of appended reply data bytes B, which will be the same as the size field in the corresponding Control Command packet. B does not include any dummy bytes for padding.
2 to (N-1)+2	Data	Reply data. The size of this data section will be an integer number of words N, where N = Ceil(B / 4)* When B is not a multiple of 4, a number of dummy bytes (4 N — B) will be padded after the last data byte. Padded dummy bytes will have the value 0 (zero).

Table 12 • **Command Acknowledgment Format**

Word	Content	Description
N+2	CRC	32 bit CRC calculated over data words 0 to (N+2)-1).
	4x K29.7	End of packet indication.

CoaXPress Host IP writes Word 0 to Word N+2 into downconnection Command Acknowledgment Receiver FIFO. Before Word 0, there is an addition word, which indicates the reading Acknowledgment packet length in unit of words.

The software must read register 0x009A bit [4] periodically to determine if there is Command Acknowledgment data to be read. The software must read the packet out word by word.

To read the packet, the software must execute the following steps:

1. Read register 0x009A bit [4], 1 means there is data to be read. 0 means no data to be read and finish the reading operation.
2. Set register 0x0099 bit [0] to 0.
3. Set register 0x0099 bit [0] to 1.
4. Read register 0x009C, the read data is reading word.
5. Read register 0x009B, if bit [3] is 0, the reading data should be discarded. If bit [2] is 1, the reading data means the reading packet length. If bit [1] is 1, the reading data is Word 0. If bit [0] is 1, the reading data is Word N+2.
6. Return to step 1.

7.4 Register Definition

The following table shows the internal registers defined in CoaXPress Host IP:

Table 13 • **CoaXPress Host IP Registers**

Addr	Bits	Name	Type	Default	Description
0x0000	[31:0]	version	RO	0x00000001	CoaXPress Host IP version.
0x0002	[0]	hsuc_enable	RW	0x0	Enable high speed upconnection transmitter, 1 means enable.
0x0003	[15:8]	lsuc_io_ack_timeout_time	RW	0x1	Low speed upconnection waiting Trigger Ack max time, 1 means 1-character time on low speed upconnection, which is 480ns.
	[7:0]	lsuc_max_resend_trigger	RW	0x3	Maximal re-send Trigger times if the Trigger Ack is not found in low speed upconnection transmitter.
0x0004	[31:0]	marker_header_word	RW	0x7c7c7c7c	Marker frame header word 8B code.
0x0010	[16]	lsuc_enable	RW	0x1	Enable low speed upconnection transmitter, 1 means enable.
	[0]	lsuc_tx_test_frame_enable	RW	0x0	Enable sending test frame on low speed upconnection.
0x0011	[15:0]	lsuc_tx_io_ack_num	RC	0x0000	How many Trigger Ack have been transmitted on low speed upconnection transmitter.

Table 13 • **CoaXPress Host IP Registers**

Addr	Bits	Name	Type	Default	Description
0x0012	[15:0]	lsuc_tx_r_trigger_num	RC	0x0000	How many Rising Trigger have been transmitted on low speed upconnection transmitter.
0x0013	[15:0]	lsuc_tx_f_trigger_num	RC	0x0000	How many Falling Trigger have been transmitted on low speed upconnection transmitter.
0x0014	[31:0]	lsuc_tx_test_frame_num	RC	0x0000	How many test frames have been transmitted on low speed upconnection transmitter.
0x0015	[15:0]	lsuc_tx_cmd_num	RC	0x0000	How many control command packets have been transmitted on low speed upconnection transmitter.
0x0016	[2]	lsuc_wait_ioack_timeout	RC	0X0	Indicates low speed upconnection had the event of waiting Trigger Ack timeout.
	[1]	lsuc_tx_cmd_fifo_overflow	RC	0X0	Indicates low speed upconnection control command Tx FIFO had overflow error.
	[0]	lsuc_tx_cmd_fifo_error	RC	0X0	Indicates low speed upconnection control command Tx FIFO had error, the error might be writing packet from the software format error, and the error packet has been discarded and not transmitted.
0x0008	[15:8]	hsuc_io_ack_timeout_time	RW	0x80	High speed upconnection waiting Trigger Ack max time, 0x80 means the max waiting time is 0x80 clock cycles.
	[7:0]	hsuc_max_resend_trigger	RW	0x03	Maximal re-send Trigger times if the Trigger Ack is not found in high speed upconnection transmitter.
0x0009	[0]	hsuc_tx_test_frame_enable	RW	0x0	Enable high speed upconnection transmitter to send test frame.
0x000A	[15:0]	hsuc_tx_ioack_num	RC	0x0000	How many Trigger Ack have been transmitted in high speed upconnection transmitter.
0x000B	[15:0]	hsuc_tx_r_trigger_num	RC	0x0000	How many Rising Trigger have been transmitted in high speed upconnection transmitter.
0x000C	[15:0]	hsuc_tx_f_trigger_num	RC	0x0000	How many Falling Trigger have been transmitted in high speed upconnection transmitter.
0x000D	[31:0]	hsuc_tx_test_frame_num	RC	0x00000000	How many test frames have been transmitted in high speed upconnection transmitter.

Table 13 • **CoaXPress Host IP Registers**

Addr	Bits	Name	Type	Default	Description
0x000E	[15:0]	hsuc_tx_cmd_num	RC	0x0000	How many control commands have been transmitted in high speed upconnection transmitter.
0x000F	[2]	hsuc_wait_ioack_timeout	RC	0x0	High speed upconnection transmitter had waiting Trigger Ack timeout.
	[1]	hsuc_tx_cmd_fifo_overflow	RC	0x0	High speed upconnection control command transmitter FIFO had overflow error.
	[0]	hsuc_tx_cmd_fifo_error	RC	0x0	High speed upconnection control command transmitter FIFO had error, it might be caused by wrong writing packet format from the software.
0X0090	[3:0]	hsdc_rx_conntion_id	RW	0x0	Connection ID for high speed downconnection channel.
0X0091	[1]	hsdc_rx_data_error	RC	0x0	Indicates if high speed downconnection receiver had RX data error.
	[0]	hsdc_rx_frame_type_error	RC	0x0	Indicates if high speed downconnection receiver had RX frame type filed error.
0X0092	[15:0]	hsdc_rx_r_trigger_num	RC	0x0000	How many Rising Trigger have been received in high speed downconnection receiver.
0X0093	[15:0]	hsdc_rx_f_trigger_num	RC	0x0000	How many Falling Trigger have been received in high speed downconnection receiver.
0X0094	[15:0]	hsdc_rx_io_ack_num	RC	0x0000	How many Trigger Ack have been received in high speed downconnection receiver.
0X0095	[15:0]	hsdc_rx_cmd_ack_num	RC	0x0000	How many Control Acknowledge have been received in high speed downconnection receiver.
0X0096	[31:0]	hsdc_rx_err_test_num	RC	0x00000000	How many error test frames have been received in high speed downconnection receiver.
0X0097	[31:0]	hsdc_rx_test_num	RC	0x00000000	How many test frames have been received in high speed downconnection receiver.
0X0098	[31:0]	hsdc_rx_sdp_num	RC	0x00000000	How many stream data packets have been received in high speed downconnection receiver.
0X0099	[0]	hsdc_cmd_ack_read_en	RW	0x0	Set to 1 to read 1 word from downconnection RX command acknowledge FIFO.

Table 13 • **CoaXPress Host IP Registers**

Addr	Bits	Name	Type	Default	Description
0X009A	[4]	hsdc_cmd_ack_available	RC	0x0	Indicates if there is available RX command acknowledge packet to be read in downconnection receiver.
	[0]	hsdc_cmd_ack_fifo_empty	RC	0x0	Indicates if there is available data to be read in downconnection RX command acknowledge FIFO.
0X009B	[3]	hsdc_cmd_ack_rdval	RO	0x0	Indicates if hsdc_cmd_ack_rd_data value is available.
	[2]	hsdc_cmd_ack_rd_len_ind	RO	0x0	Indicates if hsdc_cmd_ack_rd_data value is packet length field.
	[1]	hsdc_cmd_ack_rd_sop_ind	RO	0x0	Indicates if hsdc_cmd_ack_rd_data is the starting word of packet.
	[0]	hsdc_cmd_ack_rd_eop_ind	RO	0x0	Indicates if hsdc_cmd_ack_rd_data is the end word of packet.
0X009C	[31:0]	hsdc_cmd_ack_rd_data	RO	0x00000000	Reading data of RX command acknowledge packet.
0X009D	[0]	hsdc_cmd_ack_fifo_full	RC	0x0	Indicates if RX command acknowledge FIFO in downconnection receiver had full event.
0X0140	[3]	sdp_demap_fifo_error	RC	0x0	Indicates if stream data packet demap FIFO in downconnection receiver had error event, it means the RX packet had format error, the RX packet might be discarded.
	[2]	sdp_demap_fifo_overflow	RC	0x0	Indicates if stream data packet demap FIFO in downconnection receiver had overflow event.
	[1]	conn_fifo_error	RC	0x0	Indicates if connection FIFO in downconnection receiver had error event, it means the RX packet had format error, the RX packet might be discarded.
	[0]	conn_fifo_overflow	RC	0x0	Indicates if connection FIFO in downconnection receiver had overflow event.
0X0150	[7:0]	sdp_demap_sid	RW	0x00	Stream data packet demapper stream ID.

Table 13 • **CoaXPress Host IP Registers**

Addr	Bits	Name	Type	Default	Description
0X0151	[3]	sdp_demap_sop_error	RC	0x0	Indicates stream data packet demapper had RX SOP error.
	[2]	sdp_demap_eop_error	RC	0x0	Indicates stream data packet demapper had RX EOP error.
	[1]	sdp_demap_crc_error	RC	0x0	Indicates stream data packet demapper had RX CRC error.
	[0]	sdp_demap_tag_error	RC	0x0	Indicates stream data packet demapper had RX TAG error.
0x0200	[1]	tx_cmd_wr_sop	RW	0x0	Tx control command writing data SOP indication.
	[0]	tx_cmd_wr_eop	RW	0x0	Tx control command writing data EOP indication.
0X0201	[31:0]	tx_cmd_wr_data	RW	0x00000000	Tx control command writing data SOP.
0X0202	[1]	hsuc_tx_cmd_wr_en	RW	0X0	Tx control command data writing enable for high speed upconnection.
	[0]	lsuc_tx_cmd_wr_en	RW	0X0	Tx control command data writing enable for low speed upconnection.

8 CoaXPress Device IP Configuration Guide

8.1 Connection Test

To test downconnection, the software must set register 0x00CA bit [0] to 1, then read register 0x00C8 to know how many test frames have been transmitted. To stop downconnection test function, the software must set register 0x00CA bit [0] to 0.

CoaXPress Device IP upconnection receiver always counts how many Test frames have been received. For high speed upconnection, the software must read register 0x0070 to know it, and read register 0x0071 to know how many error test frames have been received. For low speed upconnection, the software must read register 0x0080 to know it, and read register 0x0081 to know how many error test frames have been received.

8.2 Stream Data Packet Transmission

To enable stream data packet transmission, the software must configure a proper value to register 0x0014 bit [15:0], this register field means maximal stream data packet payload length in unit of words, it should be equal or greater than the maximal image line packet.

To disable stream data packet transmission, register 0x0014 bit [15:0] should be set to 0x0000.

8.3 Sending Command Acknowledgment

In downconnection transmitter, there is a Command Acknowledgment FIFO to buffer Command Acknowledgment packets from the software. When the packet configuration is completed, CoaXPress Device IP starts to transmit the packet.

Refer to CoaXPress Host IP Configuration Guide section to get Command Acknowledgment format.

When generating and writing Command Acknowledgment packet in the software, the 4xK27.7, 4x0x03, and 4xK29.7 words should not be writing into CoaXPress Device IP, the software must be responsible to generate all other fields from Word 0 to Word N+2.

The software must write the Control Command packet word by word, from Word 0 to Word N+2.

To write one word into downconnection transmitter. Execute the following steps:

1. Set register 0x00C0 bit [8] to 0.
2. Set register 0x00C0 bit [1] to 1 if the writing data is Word 0, otherwise set it to 0.
3. Set register 0x00C0 bit [0] to 1 if the writing data is Word N+2, otherwise set it to 0
4. Set register 0x00C2 bit [31:0] to writing data value.
5. Set register 0x00C0 bit [1] to 1.

8.4 Reading Received Control Command

In high speed upconnection receiver and low speed upconnection receiver, there is a Control Command FIFO to buffer received Control Command packets from CoaXPress Host.

Refer to CoaXPress Host IP Configuration Guide section to get Control Command format. Control Command packet word 0 to word N+2 are written into FIFO, and an addition length word is also written into FIFO before word 0.

For high speed upconnection, the software must read register 0x007A bit [4] to determine if there is data available to read out. If there is new received packet. Execute the following steps:

1. Read register 0x007A bit [4], 1 means there is data to be read. 0 means no data to be read and finish the reading operation.
2. Set register 0x0079 bit [0] to 0.
3. Set register 0x0079 bit [0] to 1.
4. Read register 0x007C, the read data is reading word.

5. Read register 0x007B, if bit [3] is 0, the reading data should be discarded. If bit [2] is 1, the reading data means the reading packet length. If bit [1] is 1, the reading data is Word 0. If bit [0] is 1, the reading data is Word N+2.
6. Return to step 1.

For low speed upconnection, the software must read register 0x008A bit [4] to determine if there is available data to be read out. If there is new received packet, the software must execute the following steps to read it word by word.

1. Read register 0x008A bit [4], 1 means there is data to be read. 0 means no data to be read and finish the reading operation.
2. Set register 0x0089 bit [0] to 0.
3. Set register 0x0089 bit [0] to 1.
4. Read register 0x008C, the read data is reading word.
5. Read register 0x008B, if bit [3] is 0, the reading data should be discarded. If bit [2] is 1, the reading data means the reading packet length. If bit [1] is 1, the reading data is Word 0. If bit [0] is 1, the reading data is Word N+2.
6. Return to step 1.

8.5 Register Definition

The following table shows the internal registers defined in CoaXPress Device IP:

Table 14 • **CoaXPress Device IP Registers**

Addr	Bits	Name	Type	Default	Description
0x0000	[31:0]	version	RO	0x00000001	CoaXPress Device IP version.
0x0001	[31:16]	max_ipkt_len	RW	0x03ff	Input image line packet or marker maximal length.
	[15:0]	min_ipkt_len	RW	0x0002	Input image line packet or marker minimal length.
0x0002	[28]	hsuc_enable	RW	0x0	Enable high speed upconnection receiver.
	[18:16]	hsuc_rx_trigger_bias	RW	0x6	High speed upconnection receiver recovery trigger bias clock cycles.
	[7:0]	lsuc_rx_trigger_bias	RW	0x100	Low speed upconnection receiver recovery trigger bias clock cycles.
0x0008	[31:16]	dc_io_ack_timeout_time	RW	0x1000	Downconnection transmitter waiting Trigger Ack maximum time in unit of clock cycle. After sending a trigger, if no Trigger Ack is received within this time, it is timeout.
	[7:0]	dc_max_resend_trigger	RW	0x3	Defines the maximal resending Trigger times after waiting Trigger Ack timeout.
0x0009	[15:0]	dc_max_no_idle_words	RW	0x03e8	The maximal words between 2 IDLE word in downconnection.
0x0010	[31:0]	dc_tx_sdp_num	RC	0x00000000	How many stream data packets have been transmitted in downconnection transmitter.

Table 14 • **CoaXPress Device IP Registers**

Addr	Bits	Name	Type	Default	Description
0x0012	[2]	sdp_mapper_error	RC	0x0	Indicates if there is error in stream data packet mapper.
	[1]	sdp_mapper_fifo_error	RC	0x0	Indicates if there is error in stream data packet mapper FIFO.
	[0]	sdp_mapper_fifo_overflow	RC	0x0	Indicates if there is overflow in stream data packet mapper FIFO.
0x0013	[31:0]	sdp_mapper_tx_pkt_num	RC	0x00000000	How many stream data packets have been transmitted in stream data packet mapper.
0x0014	[23:16]	sdp_mapper_SID	RW	0x00	Stream data packet mapper Stream ID.
	[15:0]	sdp_mapper_pkt_max_len	RW	0x0000	Stream data packet payload maximal length in unit of words.
0x0050	[1:0]	conn_ID	RW	0x0	Downconnection transmitter ID.
0x0051	[1]	conn_fifo_error	RC	0x0	Indicates if there is error in Downconnection transmitter FIFO.
	[0]	conn_fifo_overflow	RC	0x0	Indicates if there is overflow in Downconnection transmitter FIFO.
0x0070	[31:0]	hsuc_rx_test_frame_num	RC	0x00000000	How many test frames have been received in high speed upconnection receiver.
0x0071	[31:0]	hsuc_rx_err_test_num	RC	0x00000000	How many error test frames have been received in high speed upconnection receiver.
0x0072	[15:0]	hsuc_rx_r_trigger_num	RC	0x0000	How many rising Trigger have been received in high speed upconnection receiver.
0x0073	[15:0]	hsuc_rx_f_trigger_num	RC	0x0000	How many falling Trigger have been received in high speed upconnection receiver.
0x0074	[15:0]	hsuc_rx_trigger_ack_num	RC	0x0000	How many Trigger Ack have been received in high speed upconnection receiver.

Table 14 • **CoaXPress Device IP Registers**

Addr	Bits	Name	Type	Default	Description
0x0075	[6]	hsuc_rx_cmd_fifo_full	RC	0x0	Indicates if the Control Command RX FIFO in high speed upconnection receiver is full.
	[5]	hsuc_rx_idle_error	RC	0x0	Indicates if there is IDLE error in high speed upconnection receiver.
	[4]	hsuc_rx_r_trigger_error	RC	0x0	Indicates if there is Rising Trigger error in high speed upconnection receiver.
	[3]	hsuc_rx_f_trigger_error	RC	0x0	Indicates if there is Falling Trigger error in high speed upconnection receiver.
	[2]	hsuc_rx_trigger_pair_error	RC	0x0	Indicates if there is mismatching Trigger pair error in high speed upconnection receiver.
	[1]	hsuc_rx_ioack_error	RC	0x0	Indicates if there is Trigger Ack error in high speed upconnection receiver.
	[0]	hsuc_rx_cmd_error	RC	0x0	Indicates if there is Control Command packet error in high speed upconnection receiver.
0x0076	[0]	hsuc_rx_cmd	RC	0x0	Indicates if there is new received Control Command packet in high speed upconnection.
0x0079	[0]	hsuc_cmd_rd_enable	RW	0x0	The rising edge of this signal read 1 RX control Command packet word.
0x007A	[4]	hsuc_cmd_available	RO	0x0	Indicates if there is received Control Command packet data to be read.
	[0]	hsuc_cmd_fifo_empty	RO	0x0	Indicates if the RX Control Command FIFO is full in high speed upconnection receiver.
0x007B	[3]	hsuc_cmd_rdata_val	RO	0x0	Indicates if hsuc_cmd_rdata is available.
	[2]	hsuc_cmd_rdata_len_ind	RO	0x0	Indicates if the hsuc_cmd_rdata is RX Control Command packet length.
	[1]	hsuc_cmd_rdata_sop_ind	RO	0x0	Indicates if the hsuc_cmd_rdata is the starting word of the RX Control Command packet.
	[0]	hsuc_cmd_rdata_eop_ind	RO	0x0	Indicates if the hsuc_cmd_rdata is the end word of the RX Control Command Packet.
0x007C	[31:0]	hsuc_cmd_rdata	RO	0x00000000	Reading data of RX Control Command packet.

Table 14 • **CoaXPress Device IP Registers**

Addr	Bits	Name	Type	Default	Description
0x007D	[1]	hsuc_cmd_fifo_error	RC	0x0	Indicates there is error in high speed upconnection RX Control Command FIFO.
	[0]	hsuc_cmd_fifo_full	RC	0x0	Indicates there is full event in high speed upconnection RX Control Command FIFO.
0X0080	[31:0]	lsuc_rx_test_frame_num	RC	0x00000000	How many test frames have been received in low speed upconnection receiver.
0X0081	[31:0]	lsuc_rx_err_test_num	RC	0x00000000	How many error test frames have been received in low speed upconnection receiver.
0X0082	[15:0]	lsuc_rx_r_trigger_num	RC	0x0000	How many rising Trigger have been received in low speed upconnection receiver.
0X0083	[15:0]	lsuc_rx_f_trigger_num	RC	0x0000	How many falling Trigger have been received in low speed upconnection receiver.
0X0084	[15:0]	lsuc_rx_trigger_ack_num	RC	0x0000	How many Trigger Ack have been received in low speed upconnection receiver.
0X0085	[6]	lsuc_rx_cmd_fifo_full	RC	0x0	Indicates if the Control Command RX FIFO in low speed upconnection receiver is full.
	[5]	lsuc_rx_idle_error	RC	0x0	Indicates if there is IDLE error in low speed upconnection receiver.
	[4]	lsuc_rx_r_trigger_error	RC	0x0	Indicates if there is Rising Trigger error in low speed upconnection receiver.
	[3]	lsuc_rx_f_trigger_error	RC	0x0	Indicates if there is Falling Trigger error in low speed upconnection receiver.
	[2]	lsuc_rx_trigger_pair_error	RC	0x0	Indicates if there is mismatching Trigger pair error in low speed upconnection receiver.
	[1]	lsuc_rx_ioack_error	RC	0x0	Indicates if there is Trigger Ack error in low speed upconnection receiver.
	[0]	lsuc_rx_cmd_error	RC	0x0	Indicates if there is Control Command packet error in low speed upconnection receiver.
0X0086	[0]	lsuc_rx_cmd	RC	0x0	Indicates if there is new received Control Command packet in low speed upconnection.
0X0089	[0]	lsuc_cmd_rd_enable	RW	0x0	The rising edge of this signal read 1 RX control Command packet word.

Table 14 • **CoaXPress Device IP Registers**

Addr	Bits	Name	Type	Default	Description
0X008A	[4]	lsuc_cmd_available	RO	0x0	Indicates if there is received Control Command packet data to be read.
	[0]	lsuc_cmd_fifo_empty	RO	0x0	Indicates if the RX Control Command FIFO is full in low speed upconnection receiver.
0X008B	[3]	lsuc_cmd_rdata_val	RO	0x0	Indicates if lsuc_cmd_rdata is available.
	[2]	lsuc_cmd_rdata_len_ind	RO	0x0	Indicates if the lsuc_cmd_rdata is RX Control Command packet length.
	[1]	lsuc_cmd_rdata_sop_ind	RO	0x0	Indicates if the lsuc_cmd_rdata is the starting word of the RX Control Command packet.
	[0]	lsuc_cmd_rdata_eop_ind	RO	0x0	Indicates if the lsuc_cmd_rdata is the end word of the RX Control Command Packet.
0X008C	[31:0]	lsuc_cmd_rdata	RO	0x00000000	Reading data of RX Control Command packet.
0X008D	[1]	lsuc_cmd_fifo_error	RC	0x0	Indicates there is error in low speed upconnection RX Control Command FIFO.
	[0]	lsuc_cmd_fifo_full	RC	0x0	Indicates there is full event in low speed upconnection RX Control Command FIFO.
0X00C0	[8]	dc_tx_cmd_ack_cfg_en	RW	0x0	The rising edge of this signal writes 1 dc_tx_cmd_ack_cfg_data into TX Command Acknowledgment FIFO in downconnection.
	[1]	dc_tx_cmd_ack_cfg_sop	RW	0x0	Indicates if dc_tx_cmd_ack_cfg_data is the starting word of writing Command Acknowledgment packet.
	[0]	dc_tx_cmd_ack_cfg_eop	RW	0x0	Indicates if dc_tx_cmd_ack_cfg_data is the end word of writing Command Acknowledgment packet.
0X00C2	[31:0]	dc_tx_cmd_ack_cfg_data	RW	0x00000000	Writing data of Command Acknowledgment packet.
0X00C3	[31:0]	dc_tx_sdp_num	RC	0x00000000	How many stream data packets have been transmitted in downconnection transmitter.
0X00C4	[31:0]	dc_tx_cmd_ack_num	RC	0x00000000	How many Command Acknowledgment packets have been transmitted in downconnection transmitter.

Table 14 • **CoaXPress Device IP Registers**

Addr	Bits	Name	Type	Default	Description
0X00C5	[15:0]	dc_tx_r_trigger_num	RC	0x0000	How many Rising Trigger packets have been transmitted in downconnection transmitter.
0X00C6	[15:0]	dc_tx_f_trigger_num	RC	0x0000	How many Falling Trigger packets have been transmitted in downconnection transmitter.
0X00C7	[15:0]	dc_tx_ioack_num	RC	0x0000	How many Trigger Ack packets have been transmitted in downconnection transmitter.
0X00C8	[31:0]	dc_tx_test_frame_num	RC	0x00000000	How many test frames have been transmitted in downconnection transmitter.
0X00C9	[4]	dc_wait_ioack_timeout	RC	0x0	Indicates if there is waiting Trigger Ack timeout event in downconnection transmitter.
	[3]	dc_tx_sdp_error	RC	0x0	Indicates if there is TX SDP error in downconnection transmitter.
	[2]	dc_tx_cmd_ack_error	RC	0x0	Indicates if there is TX CMD error in downconnection transmitter.
	[1]	dc_tx_cmd_ack_fifo_error	RC	0x0	Indicates if there is error in downconnection TX Command Acknowledge FIFO.
	[0]	dc_tx_cmd_ack_fifo_full	RC	0x0	Indicates if there is overflow in downconnection TX Command Acknowledge FIFO.
0X00CA	[0]	dc_tx_test_frame_enable	RW	0x0	Enable test frame transmission in downconnection.