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Microsemi | a Microchip company

FPGA & SoC TechBytes

Happy 2019!

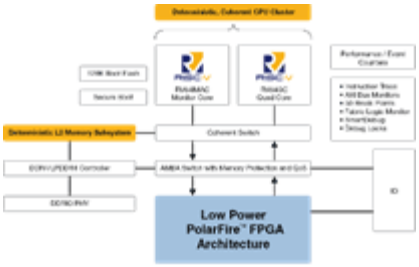
Welcome to the first FPGA & SoC TechBytes issue of 2019. We start the new year on the heels of last month's unveiling of the PolarFire SoC architecture at the RISC-V Summit in Santa Clara, CA, the availability of PolarFire production devices, and this month's launch of Libero SoC version 12.0, the most significant release of our FPGA design suite yet. We'll are also introducing a new Aviation & Defense Newsletter scheduled to launch next month.

YES, I want to continue receiving this newsletter

Libero SoC v12.0 Released, Download Today

Libero SoC version 12.0 is the most significant release of the FPGA design suite yet as marked by the delivery of gains in runtime and quality of results, production timing for the low-power PolarFire FPGA family, and one common design flow for all the company's latest generation FPGA families. Libero SoC v12.0's enhanced design flow runtimes enable designers to accelerate compilation time, while raising quality of results with fewer design iterations. By upgrading to Libero SoC v12.0, designers will see runtime reduction of 60 percent for timing, 25 percent for place and route and 18 percent for power results. They will also see an average increase of 4 percent in quality of results for larger designs and a 10 percent improvement for the PolarFire MPF300/TS-1 device. Libero SoC v12.0 will include production timing and power for PolarFire MPF300T-1. Learn more and download the new version here.

World's First RISC-V SoC FPGA Architecture Brings Real-Time to Linux



Microchip has unveiled the architecture for a new class of SoC FPGAs that combines the industry's lowest power mid-range PolarFire™ FPGA family with a complete microprocessor subsystem based on the open, royalty-free RISC-V instruction set architecture (ISA). Microchip's new PolarFire SoC architecture brings real-time deterministic asymmetric multiprocessing (AMP) capability to Linux platforms in a multi-core coherent central processing unit (CPU) cluster. The PolarFire SoC architecture, developed in collaboration with SiFive, features a flexible 2 MB L2 memory subsystem that can be configured as a cache, scratchpad or a direct access memory. This allows designers to implement deterministic real-time embedded applications simultaneously with a rich operating system for a variety of thermal and space constrained applications in collaborative, networked IoT systems. Read more here.

PolarFire Family Achieves Key Production Milestone

Marking another significant milestone, Libero SoC v12.0 is being released simultaneously with the production release of the PolarFire MPF100T, PolarFire MPF200T and PolarFire MPF300T devices, with order entry open for all family members, including the 500T. Learn more about the PolarFire FPGA family.

Low-Power Devices for Aerospace and Defense Introduced

With the release of Libero SoC v12.0, we are introducing two new industry-leading devices for the aerospace and defense market segments—the low-power, radiation-tolerant RT4G150L, which offers 25 percent power savings for standard speed grade; and military-grade support for the SmartFusion2 M2S150T/S FCV484 device.

Game-Changing 10G PON BMR Solution

The new PolarFire BMR solution enables customers to build 10G passive optical network (PON) optical line terminals (OLTs) in unprecedented small form factor modules while drawing the lowest power in extreme thermal environments. Completely customizable with the industry's fastest (10.8 nanosecond) lock times in mid-range FPGAs for PONs, the PolarFire BMR solution is the only offering of its kind enabling 10G PON solutions in such small form factor pluggable (SFP) and 10 Gb SFP (XFP) footprints. Download the user guide.

FPGA-in-the-Loop Workflow Supports MathWorks Integration with RTG4, PolarFire and SmartFusion2 Development Boards

The new integrated Field Programmable Gate Array (FPGA)-in-the-loop (FIL) workflow with MathWorks' HDL Coder and HDL Verifier enables customers to automatically generate test benches for hardware description language (HDL) verification, including VHSIC Hardware Description Language (VHDL) and Verilog, providing rapid prototyping and verification of designs. The new Workflow, available in MATLAB's R2018b release, enables customers to integrate MathWorks' MATLAB, a multi-paradigm numerical computing environment, and its Simulink, a graphical programming environment, with Microsemi's RTG4, PolarFire® FPGA and SmartFusion™2 system-on-chip (SoC) FPGA development boards, which allows the stimulation of designs through FIL verification workflow using Microsemi's development boards. FIL verification workflow enables customers to analyze the results back in MATLAB and Simulink. Click here for more details.

- Archived Webinars and Training -

- Mi-V Embedded Ecosystem
- SoftConsole and Renode from Antmicro
- LiberoDesign Suite Overview
- Enhanced Constraints Flow Overview 2018
- Embedded Design Flow using SoftConsole and Mi-V
- SmartDebug Live Probe
- SmartDebug Active Probe

- Events and Workshops -

- Embedded World – Nuremberg, Germany, Feb 26-28
- MATLAB EXPO India – Bangalore, India, April 25
- MATLAB EXPO India – Pune, India, April 23
- MATLAB EXPO India – Hyderabad, India, April 30
- FPGA Kongress – Munich, Germany, May 21-23

- News and Articles -

The Solar System's Fastest FPGAs Journey to the Sun Carrying a Microprocessor Relic on Board - **EE Journal**

Create Small Form Factor 10G Passive Optical Network Applications with Microchip's PolarFire FPGA Burst Mode Receiver - **Microchip**

World's first RISC-V-based FPGA SoC runs Linux - **LinuxGizmos.com**

Microchip unveils new class of SoC FPGA - **New Electronics**

Microsemi adds to RISC-V based FPGAs - **ElectronicsWeekly**

RISC-V: More Than A Core – **SemiEngineering**