Microsemi Corporation

June 21, 2019

Customer Notification No: CN19011

Subject
RTG4 LSRAM Circuit for Pipelined ECC and I/O Driven High at the End of Programming

Summary
This document describes two customer advisory notifications (CANs) for all RTG4 devices. The following table summarizes each CAN and the action required by the customer.

Notification	Description	Action Required
CAN 19011.1	LSRAM BLK Select De-assertion Circuit for Pipelined ECC	Regenerate the RAM with Libero SoC v11.9 SP3 (and later 11.x releases) or v12.1 (and later 12.x releases)
CAN 19011.2	I/O Driven High at the End of Programming	Regenerate the bitstream with Libero SoC v11.9 SP4 (and later 11.x releases) or v12.1 (and later 12.x releases)

CAN 19011.1 LSRAM BLK Select De-assertion Circuit for Pipelined ECC

Description of Change
An internal hold time issue can be observed on the LSRAM when the BLK select input is de-asserted after issuing a read command in pipelined-ECC mode. When the BLK select input de-asserts, it is supposed to clear the LSRAM data output latch, and eventually result in all-zero data sent to the LSRAM DOUT ports, depending on the number of pipeline stages enabled in the LSRAM. However, due to an internal hold time issue, the BLK select de-assertion clears the LSRAM data output latch so quickly that it violates the ECC pipeline register's hold time before it can capture the valid read data corresponding to the previously issued RAM read.

The RTG4 two-port and dual-port LSRAM configurators in Libero SoC v11.9 SP3 (and later 11.x releases) or v12.1 (and later 12.x releases) have been updated to generate an additional fabric-based circuit for pipelined-ECC mode. The additional circuit avoids the hold time issue by delaying BLK select de-assertion to the active LSRAM block. The mitigation circuit will be described in a future update to the RTG4 Fabric User's Guide (UG0574).

Note that along with this LSRAM configurator update, single-depth dual-port LSRAM components using pipelined-ECC mode that expose the BLK select input will no longer hold the most recent read data after de-asserting REN. The fabric-based mitigation circuit gates-off the read data output by the pipelined BLK select input, and thus the LSRAM read data output port will transition from the previous read data to all-zero on subsequent clock cycles, based on the number of pipeline stages enabled.

Application Impact
This issue only impacts RTG4 two-port and dual-port LSRAM in pipelined-ECC mode. This issue does not impact the following LSRAM configurations:

- Synplify-inferred LSRAM (Synplify does not infer pipelined-ECC mode.)
- Any configuration where the BLK select inputs are tied high
- Non-pipelined-ECC mode (with or without DOUT pipeline)
- Non-ECC mode (with or without DOUT pipeline)
- Two-port LSRAM configurator component without depth-cascading
- Dual-port LSRAM configurator component without depth cascading, and without exposing BLK select input on any port used for reading

- LSRAM port used exclusively for writes (There is no issue if BLK select input is de-asserted on that port after a write command is issued.)

This issue does not impact RTG4 uSRAM.

Action Required

To insert the mitigation circuit, existing designs must update to Libero SoC v11.9 SP3 (and later 11.x releases) or v12.1 (and later 12.x releases) and regenerate all LSRAM components using pipelined-ECC mode.

The software configurator update only applies to pipelined-ECC LSRAM components generated from the Libero IP catalog. Manually instantiated LSRAM instances can be replaced with LSRAM configurator components in the Libero SoC versions specified above to automatically insert the mitigation logic.

- Existing designs opened in the Libero SoC versions specified above will be invalidated if they contain any pipelined-ECC LSRAM component, and the user will be asked to regenerate the affected LSRAMs.
- Compile will generate an error if pipelined-ECC LSRAM catalog components still require regeneration.
- Static Timing Analysis (STA) must be rerun to check whether the updated LSRAM component with the additional circuit still meets timing requirements.

CAN 19011.2 I/O Driven High at the End of Programming

Description of Change

At the end of the RTG4 device programming cycle, outputs could be driven high momentarily before driving out the logic value specified by the design. Designs that have set the “output state during programming” in the boundary scan register (BSR) to ‘0’ and expect the output to remain low before, during, and after programming will see a brief high glitch at the end of programming. The glitch occurs after the JTAG test reset is issued at the end of programming when the output state control is handed-off from BSR control to fabric control and the fabric design starts operating. The glitch duration is design dependent because it depends on the propagation delay from the input pin to the output pin through the user fabric design. The worst case amplitude of the glitch is VDDI level of the I/O.

Libero SoC v11.9 SP4 (and later 11.x releases) or v12.1 (and later 12.x releases) contains a fix to the bitstream generation tool that prevents this glitch by adding a JTAG instruction before issuing the JTAG reset at the end of programming. This JTAG instruction releases the input state from BSR control to fabric control before the outputs are released from BSR control. This provides additional time for the input PAD logic levels to propagate into the fabric design and set the initial output values before the output state control is handed over to the fabric logic.

Application Impact

Evaluate if you have critical outputs that must remain low before, during, and after programming to maintain desired system functionality. If so, then the design bitstream must be regenerated to eliminate this output glitch at the end of programming. There is no reliability impact to the device because the I/O is driven high for a short time.

Action Required

If you are concerned about this glitch, regenerate the bitstream using Libero SoC v11.9 SP4 (and later 11.x releases) or v12.1 (and later 12.x releases).

Contact Information

If you have further questions about this subject, contact Microsemi Technical Support department by using the support portal at https://soc.microsemi.com/Portal/Default.aspx

Regards,

Microsemi Corporation

Affected Part Numbers

Microsemi Part Number	DLA SMD Number
RT4G150-CB1657PROTO	
RT4G150-CG1657B	5962-1620801QXF
RT4G150-CG1657E	5962-1620805QXF
RT4G150-CG1657EV	
RT4G150-CG1657V	5962-1620809VXF
RT4G150-CG1657PROTO	
RT4G150-CQ352B	
RT4G150-CQ352E	
RT4G150-CQ352EV	
RT4G150-CQ352PROTO	
RT4G150-LG1657B	5962-1620803QZC
RT4G150-LG1657E	5962-1620807QZC
RT4G150-LG1657EV	
RT4G150-LG1657V	5962-1620811VZC
RT4G150-LG1657PROTO	
RT4G150-1CB1657PROTO	
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-1CG1657EV	
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-1CG1657PROTO	
RT4G150-1CQ352B	
RT4G150-1CQ352E	
RT4G150-1CQ352EV	
RT4G150-1CQ352PROTO	
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-1LG1657EV	
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-1LG1657PROTO	
RT4G150L-CG1657EV	
RT4G150L-LG1657EV	
RT4G150L-CQ352EV	
RT4G150L-CG1657E	
RT4G150L-LG1657E	
RT4G150L-CQ352E	

Microsemi Part Number	DLA SMD Number
RT4G150L-CG1657B	
RT4G150L-LG1657B	
RT4G150L-CQ352B	
RT4G150L-CG1657PROTO	
RT4G150L-CB1657PROTO	
RT4G150L-LG1657PROTO	
RT4G150L-CQ352PROTO	

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