

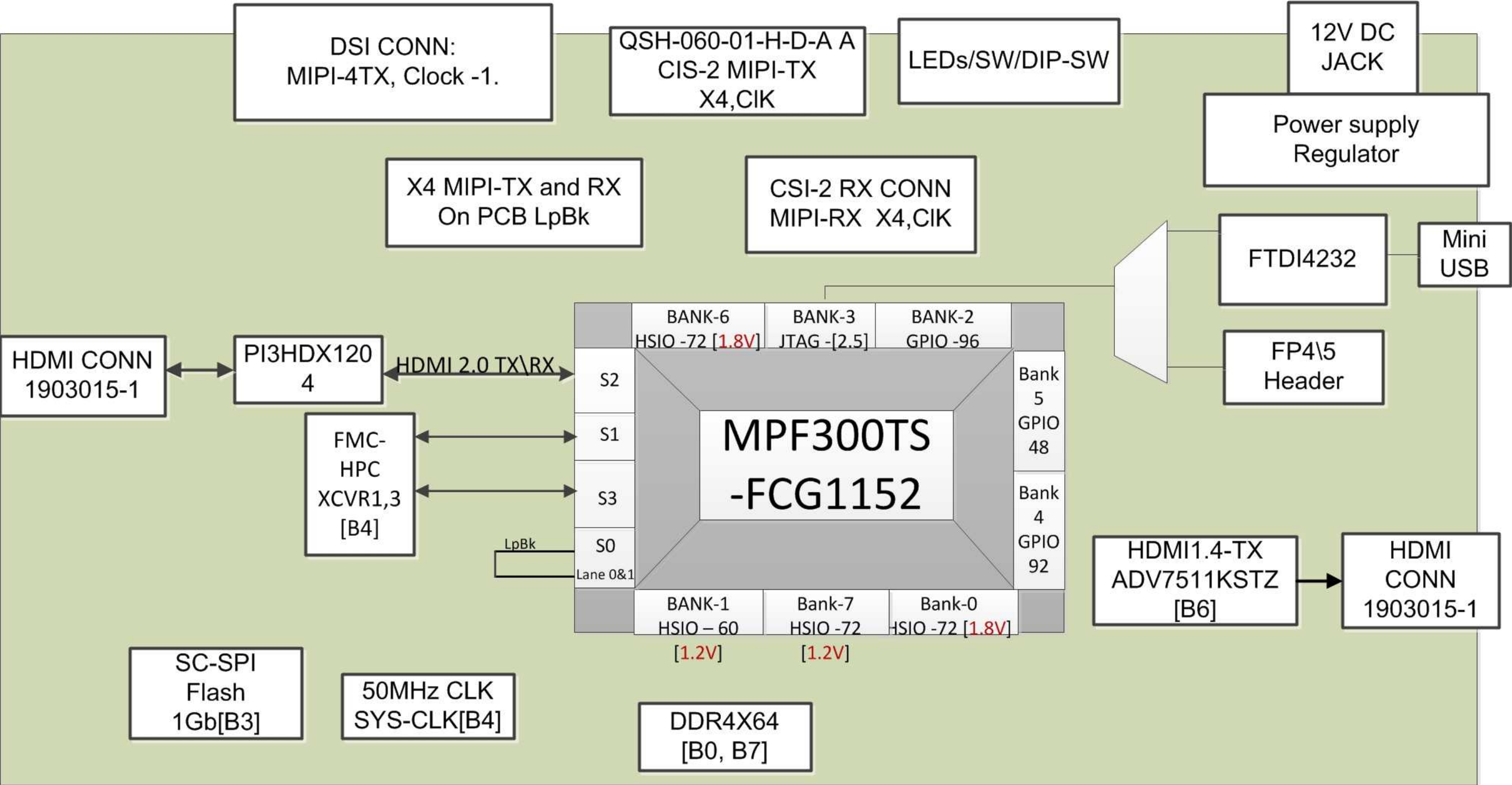
POLARFIRE VIDEO KIT

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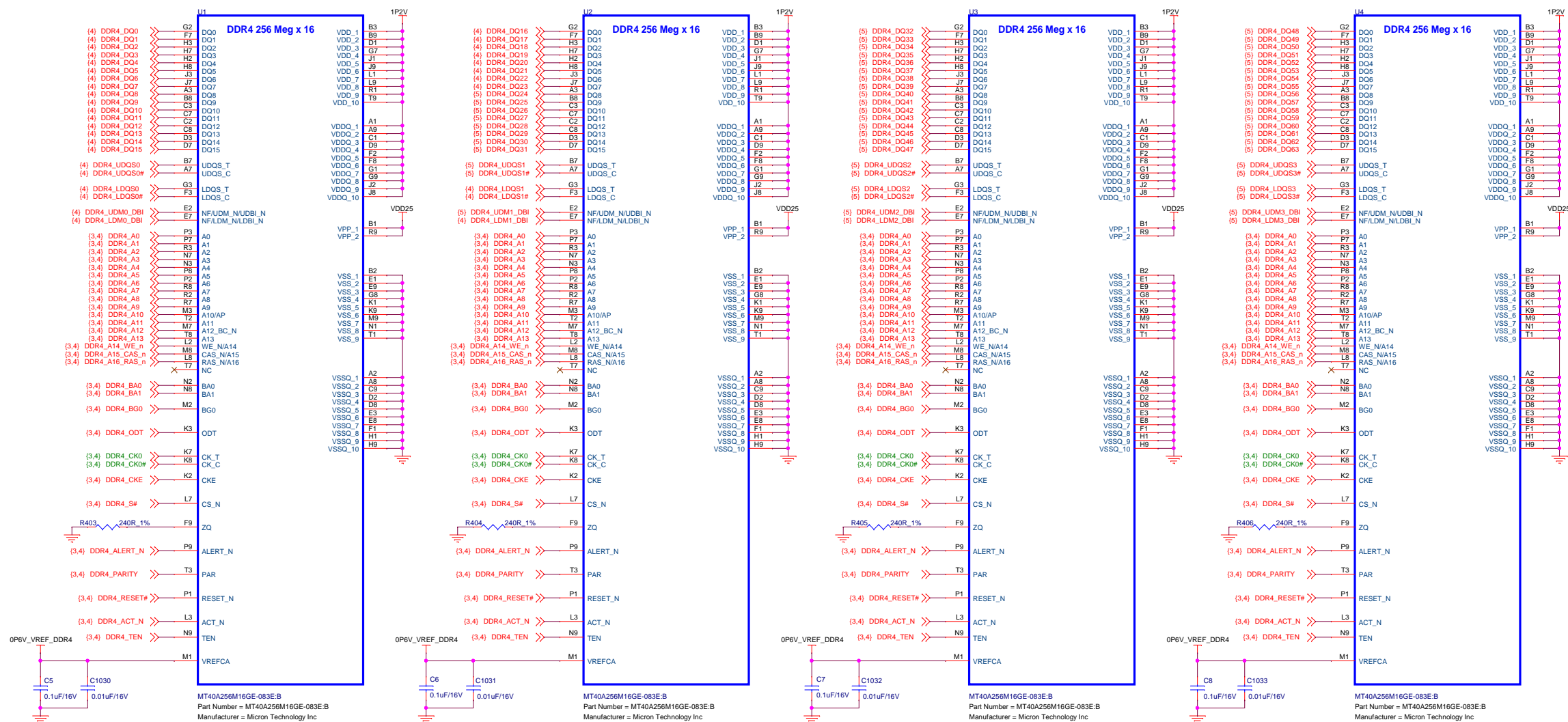
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POLARFIRE_VIDEO_KIT			
Rev	Part Number:		
1	MICROSEMI	DVP-100-000512-001	PACTRON:
Originator:			
GHURU KUMARAVELU			
Size	Date:		
Custom	Friday, February 22, 2019		
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BLOCK DIAGRAM

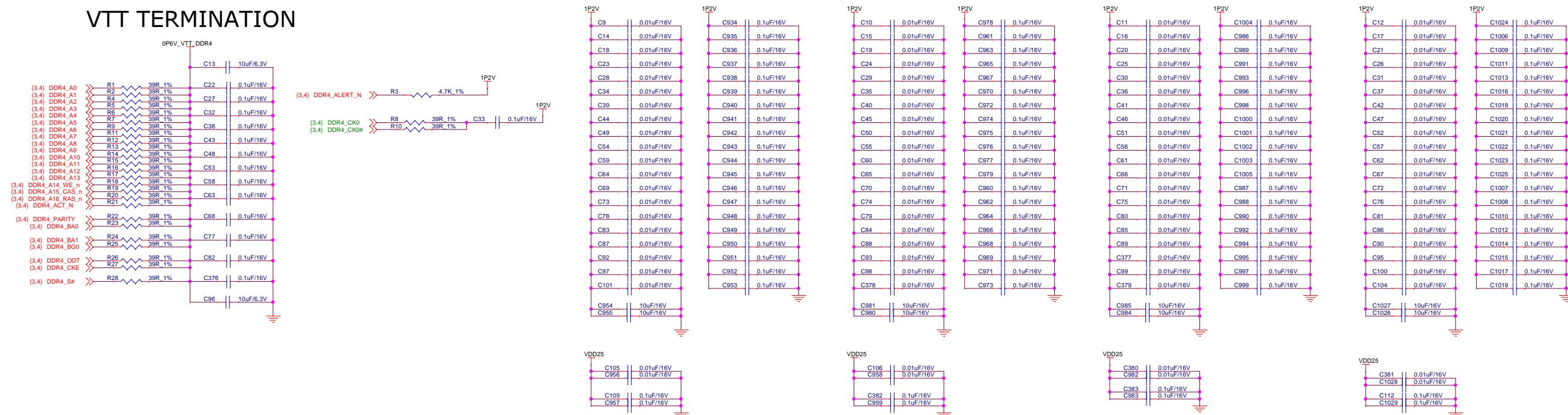


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SIZE Custom	DOCUMENT NO. DVP-100-000512-001	REV 1
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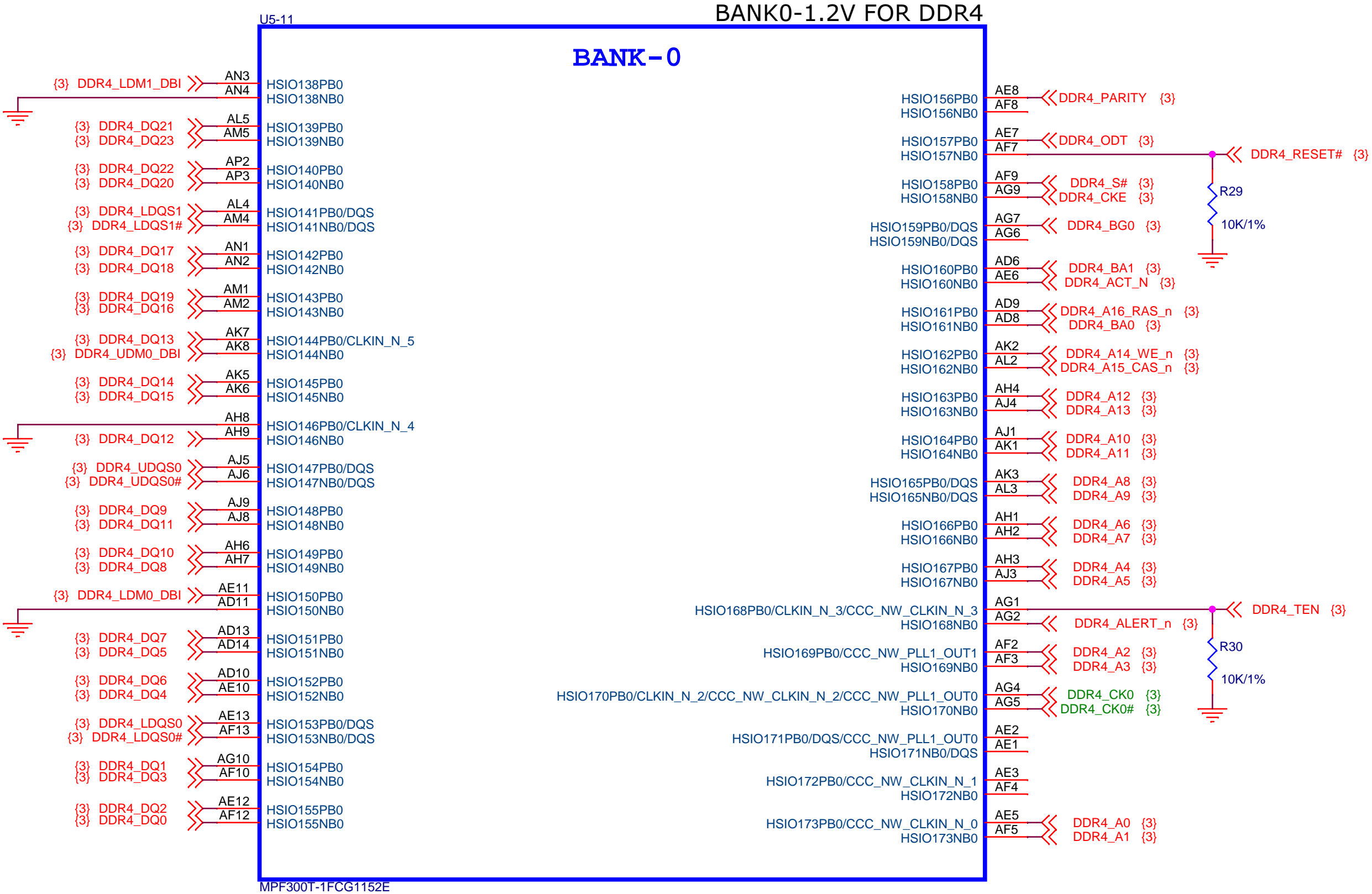
DDR4 MEMORY-BANK0&7



VTT TERMINATION



BANK0 Connection



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BANK7 Connection

D

C

B

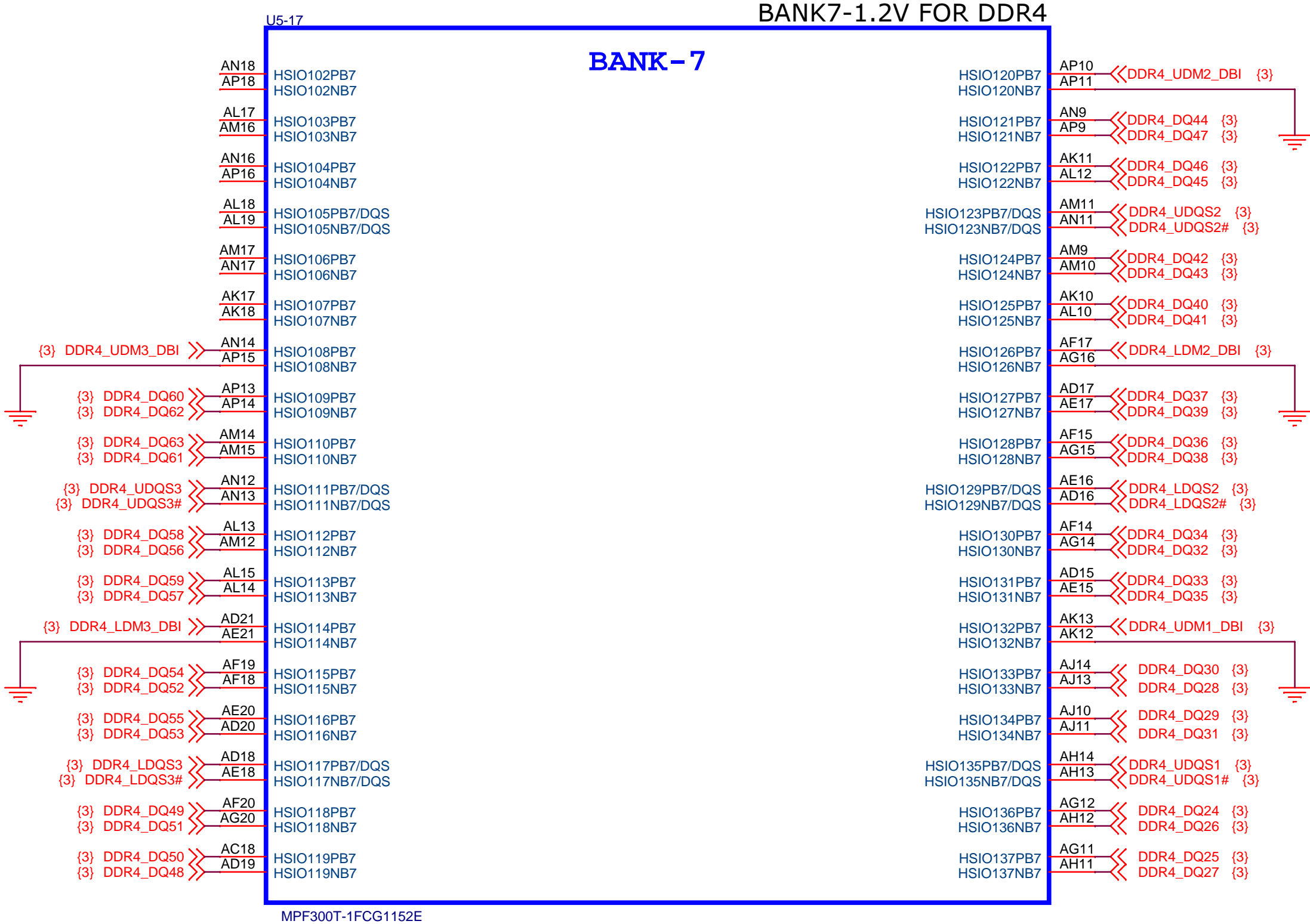
A

D

C

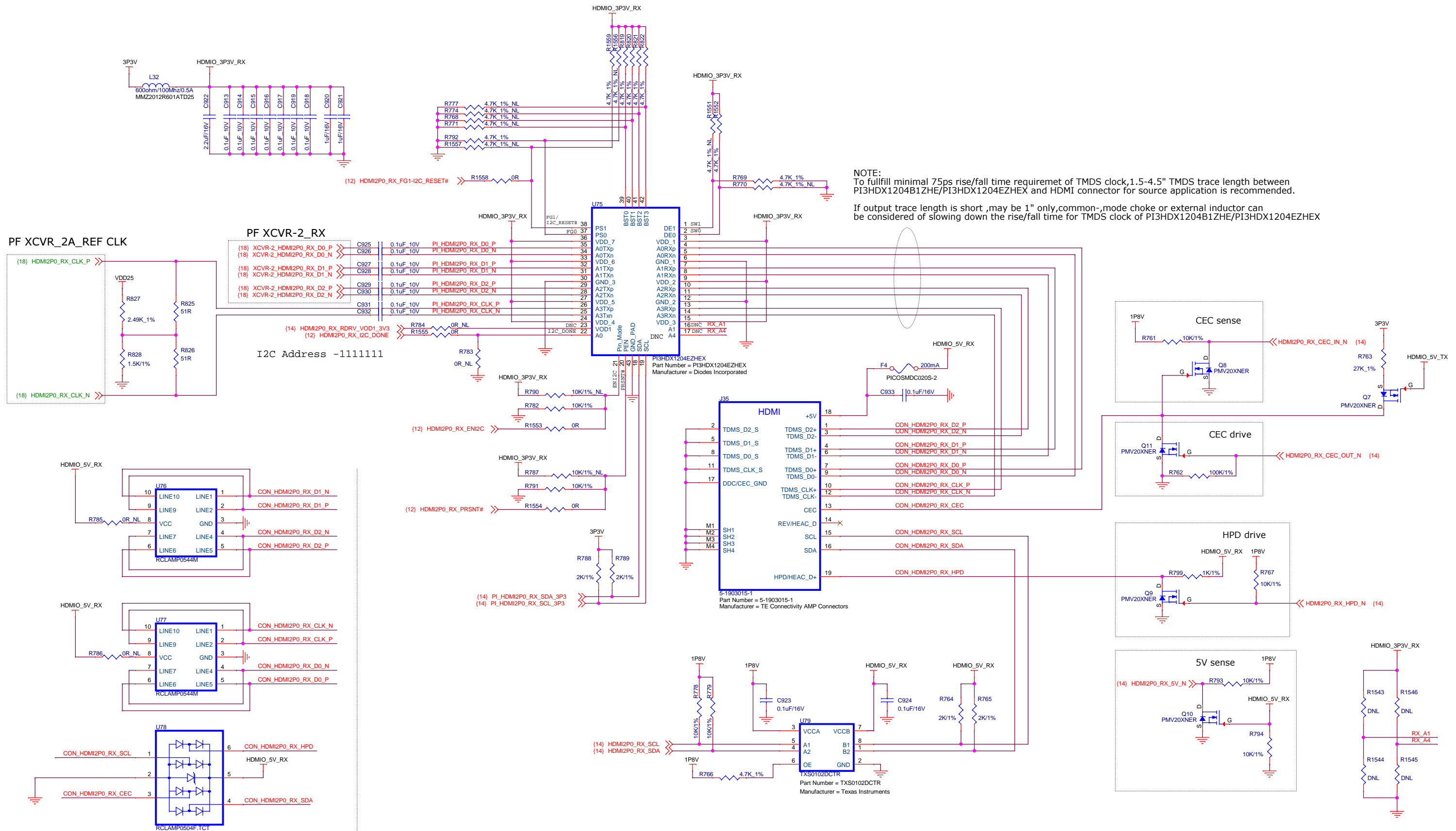
B

A

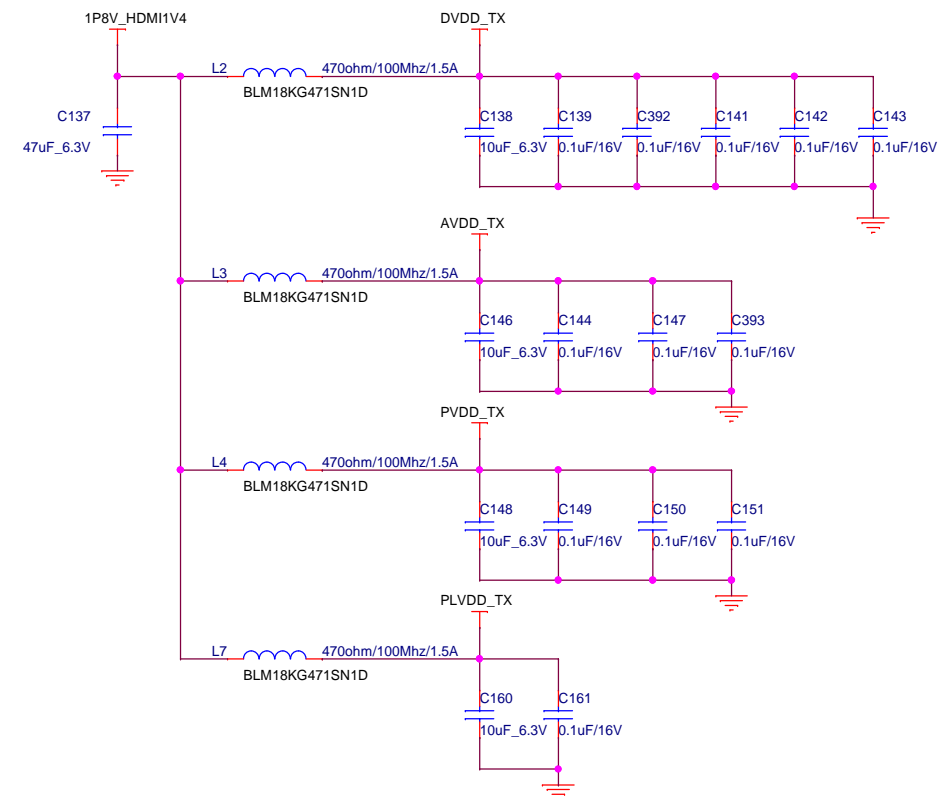
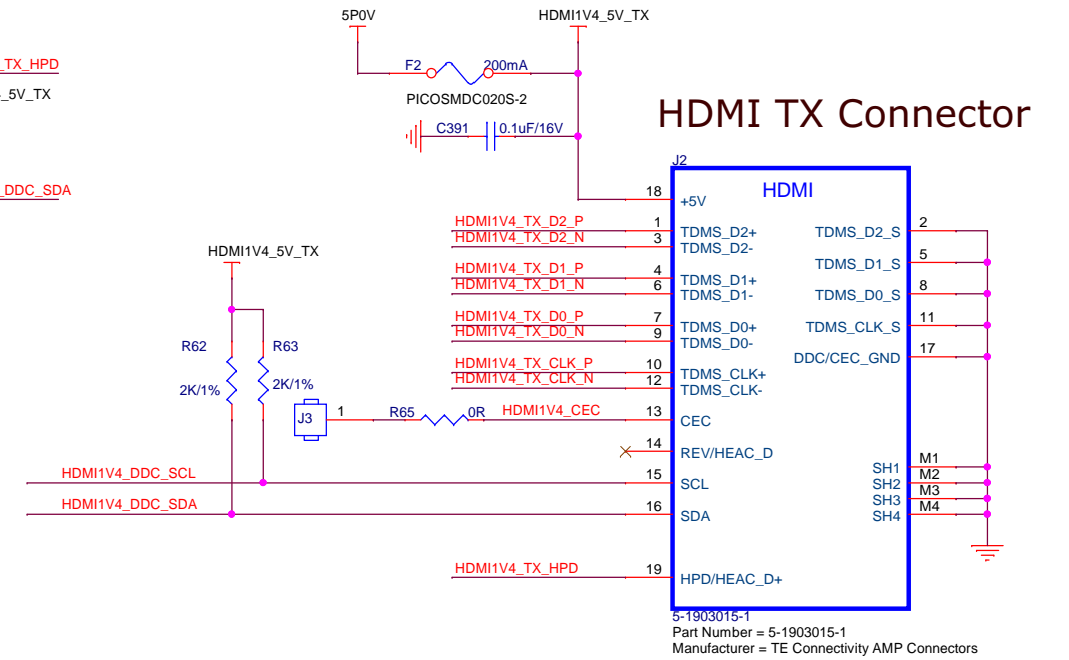
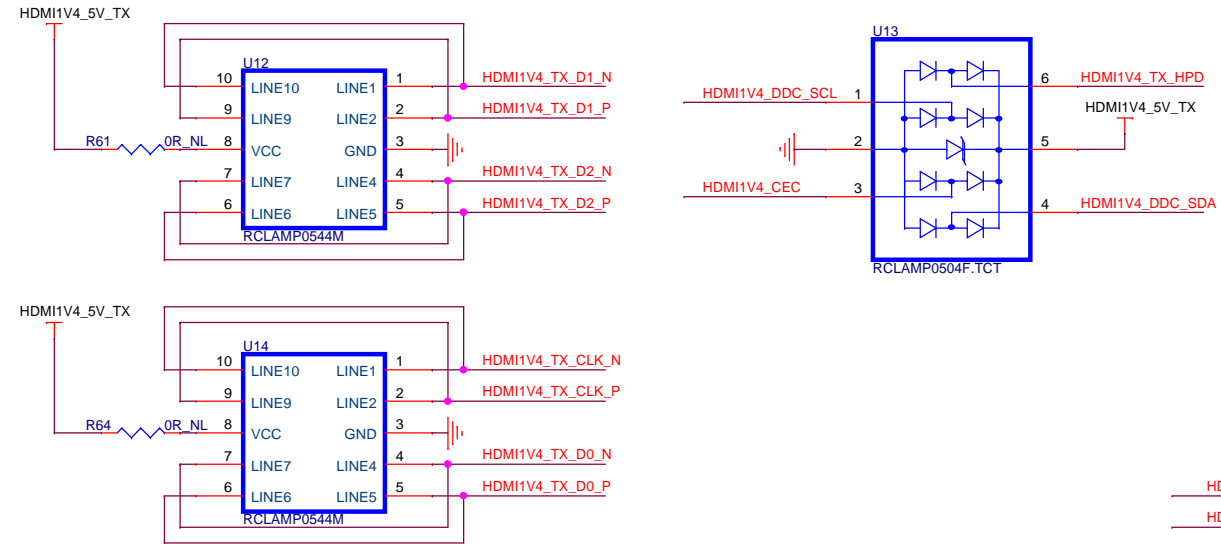
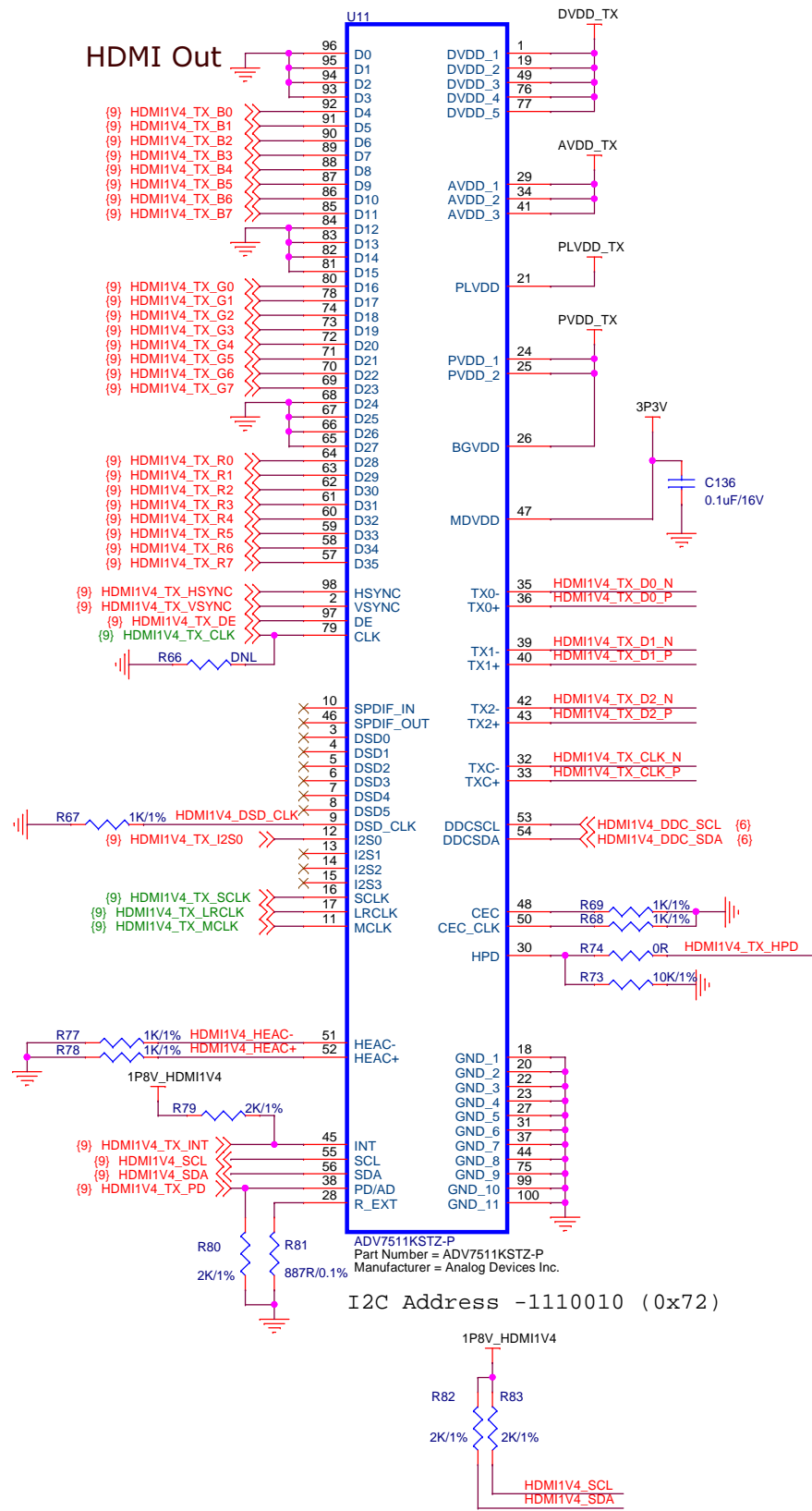


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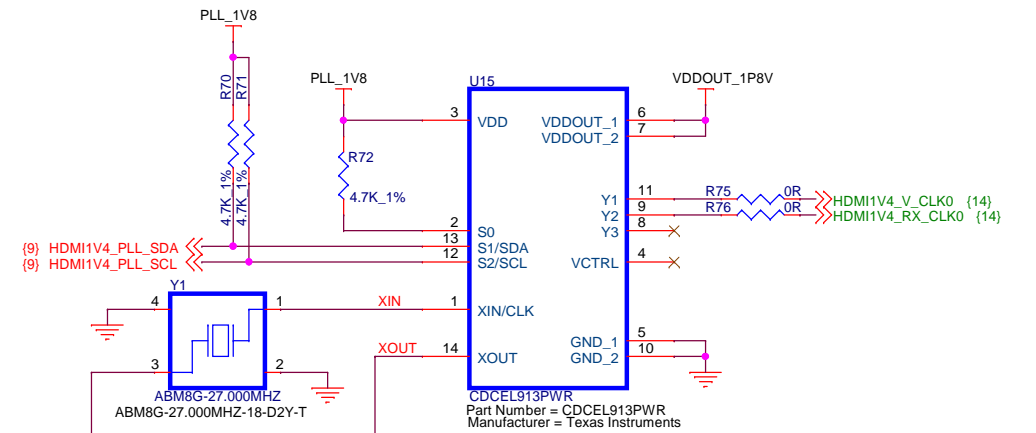
HDMI2P0 Redriver Interface (RX)



HDMI1V4 Transmitter Interface



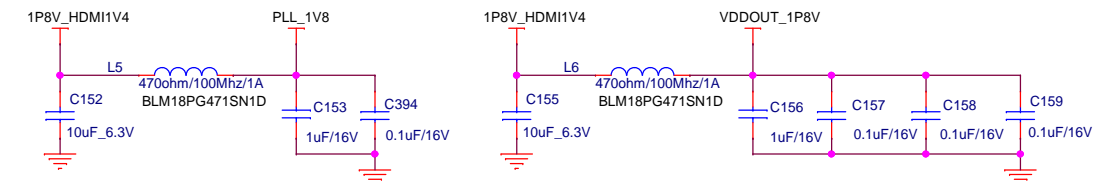
Clock Synthesizer



I2C Address -1100101

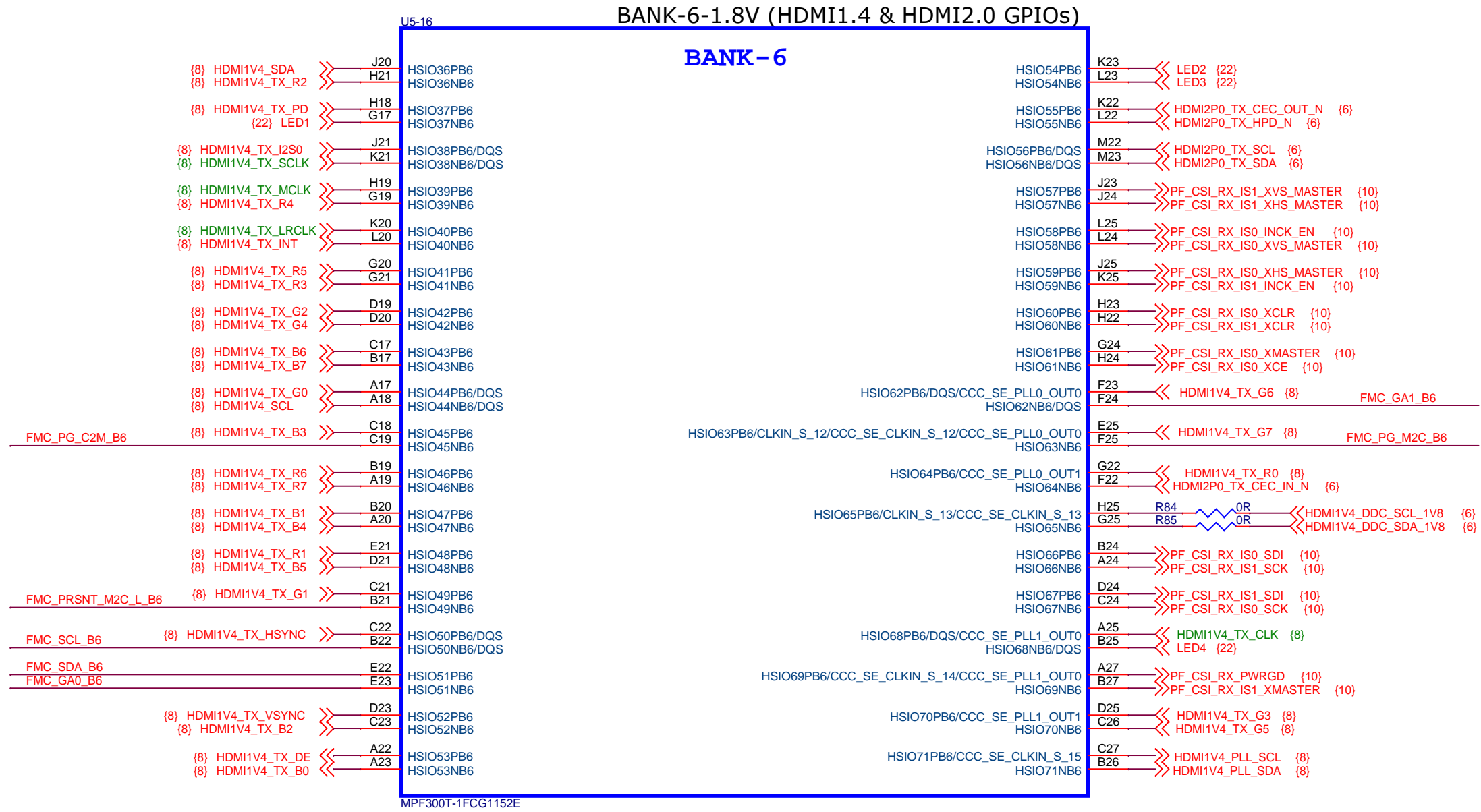
NOTE

HDMI1V4_V_CLK0 & HDMI1V4_RX_CLK0 SHOULD BE ASSIGN TO CCC OF PF

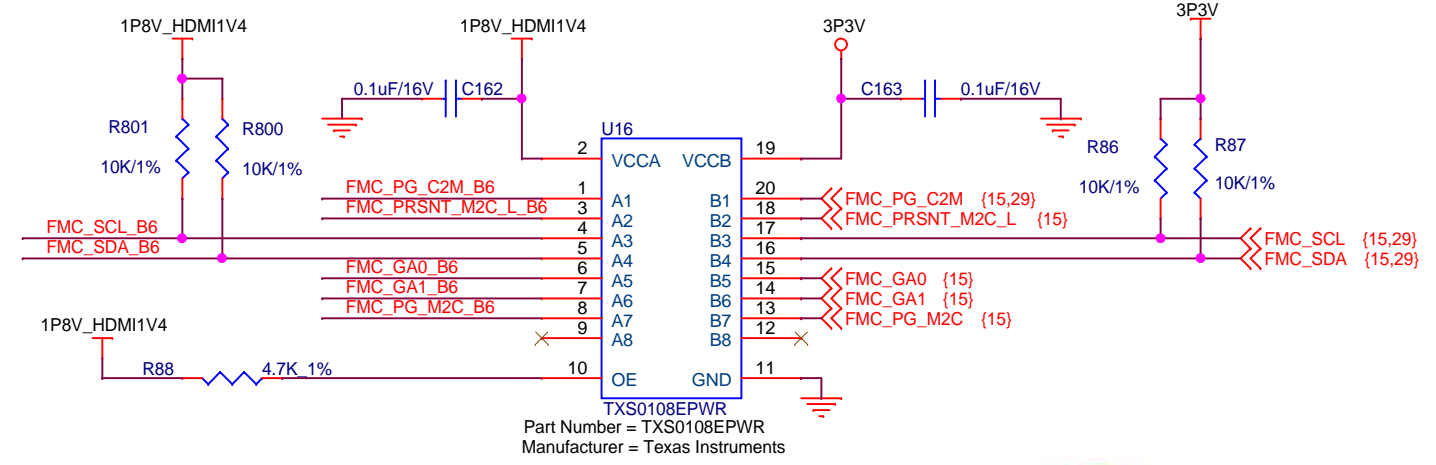


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Custom			1
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BANK6 Connection

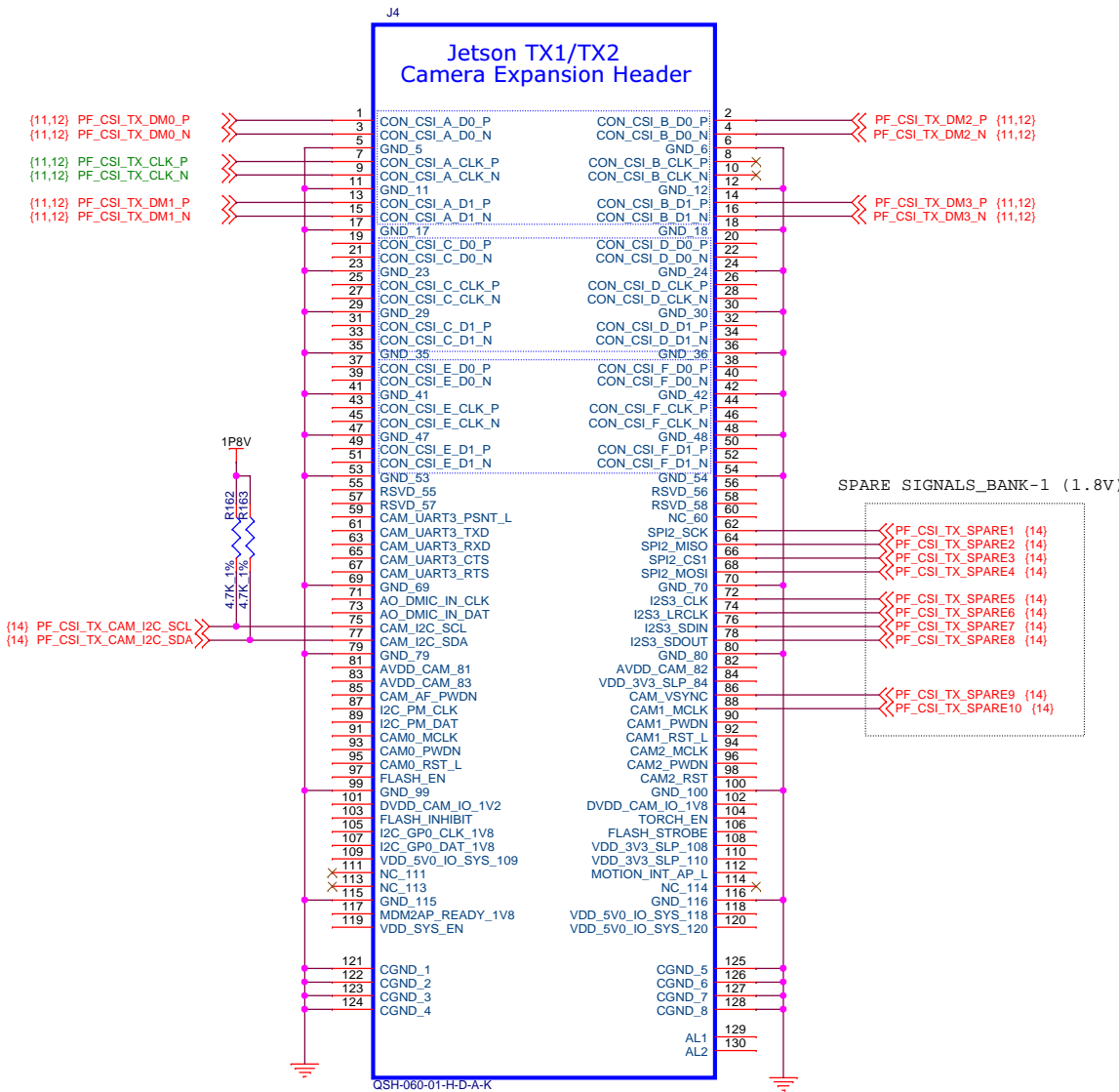


Level Translator - FMC Signals

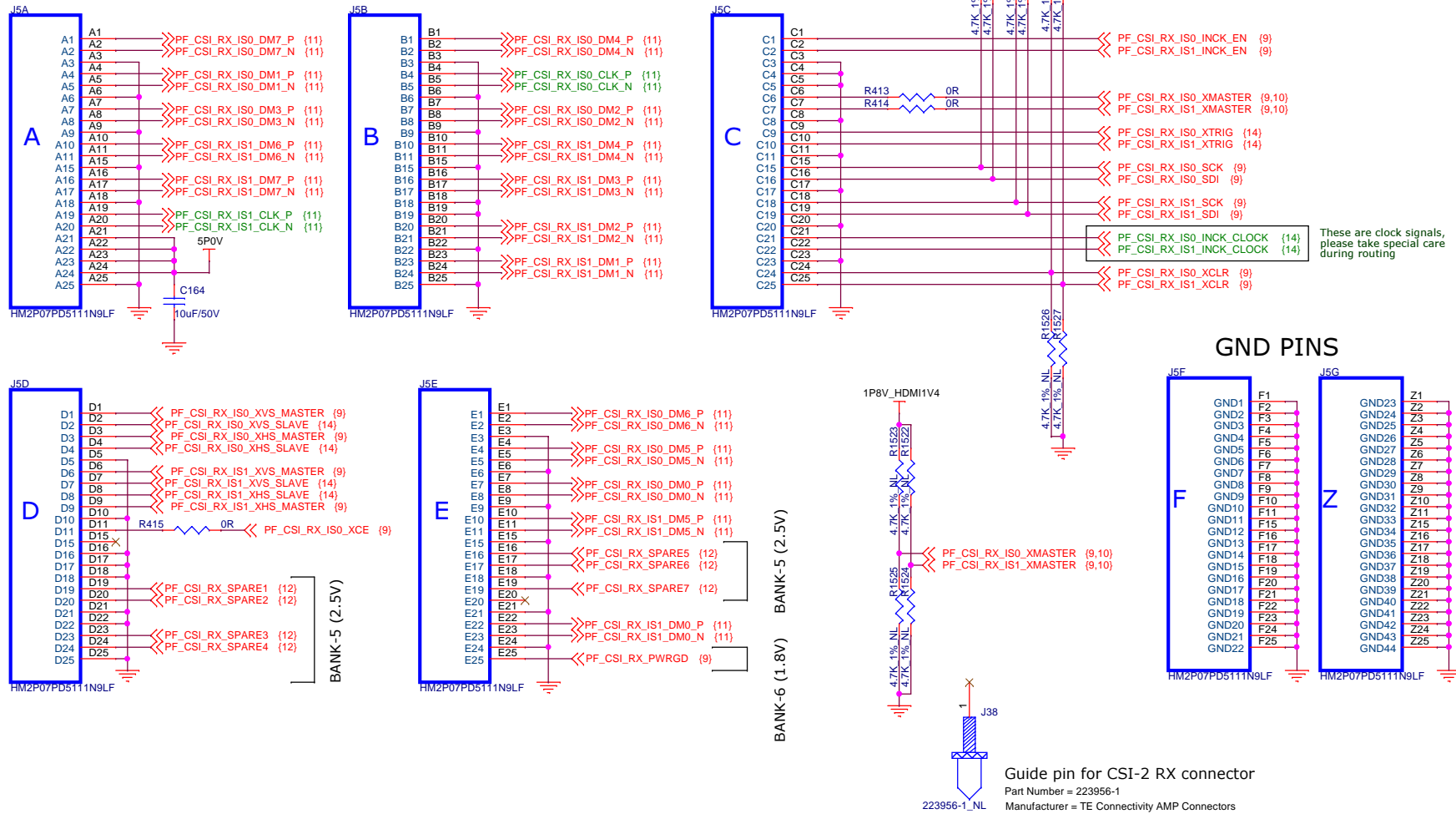


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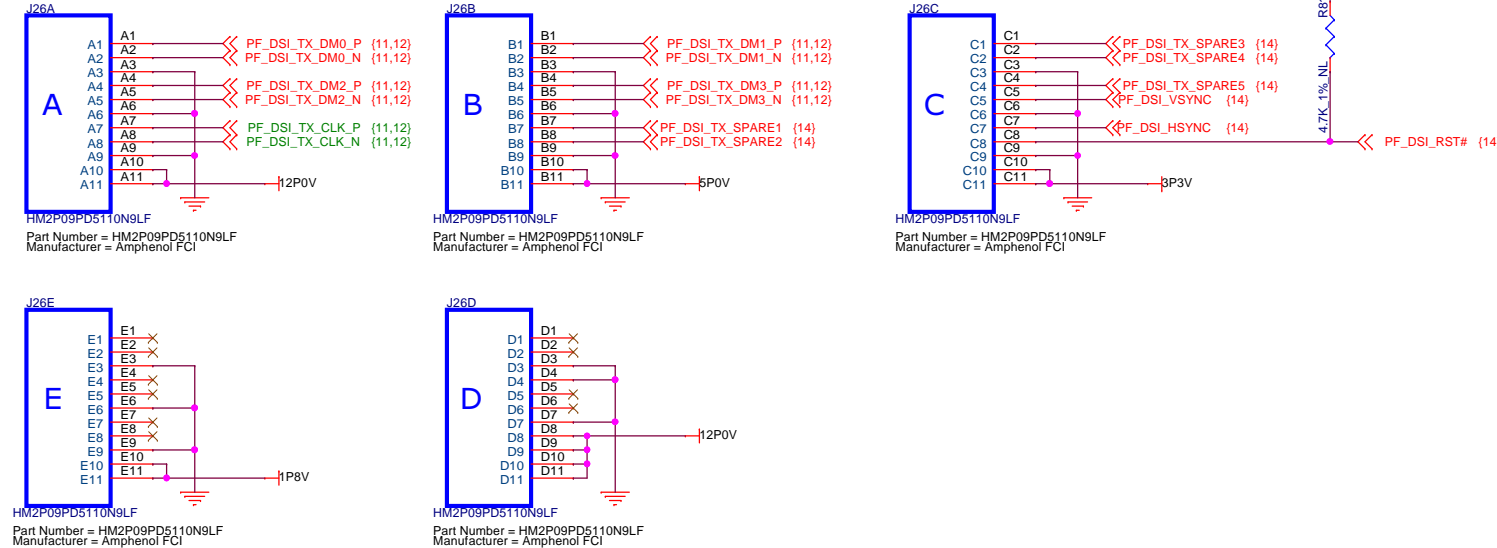
CSI-2 TX To Jetson TX1/TX2 Camera Expander



CSI-2 RX Image Sensor Interface



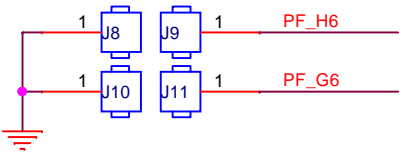
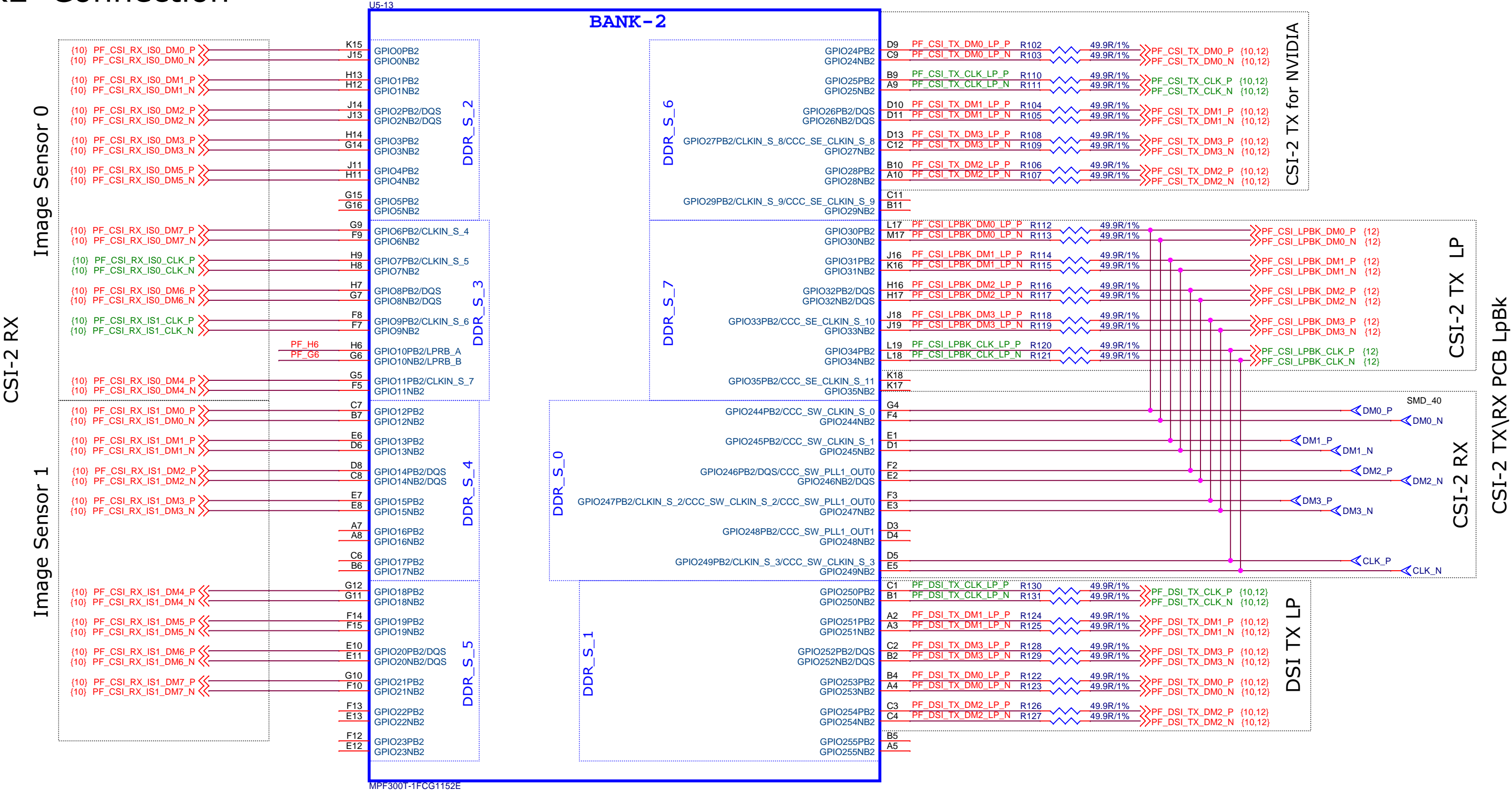
DSI TX Display Interface



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BANK2 Connection

BANK-2-1P2V (LVCMOS12 FOR MIPI), VDDAUX2=2.5/3.3V

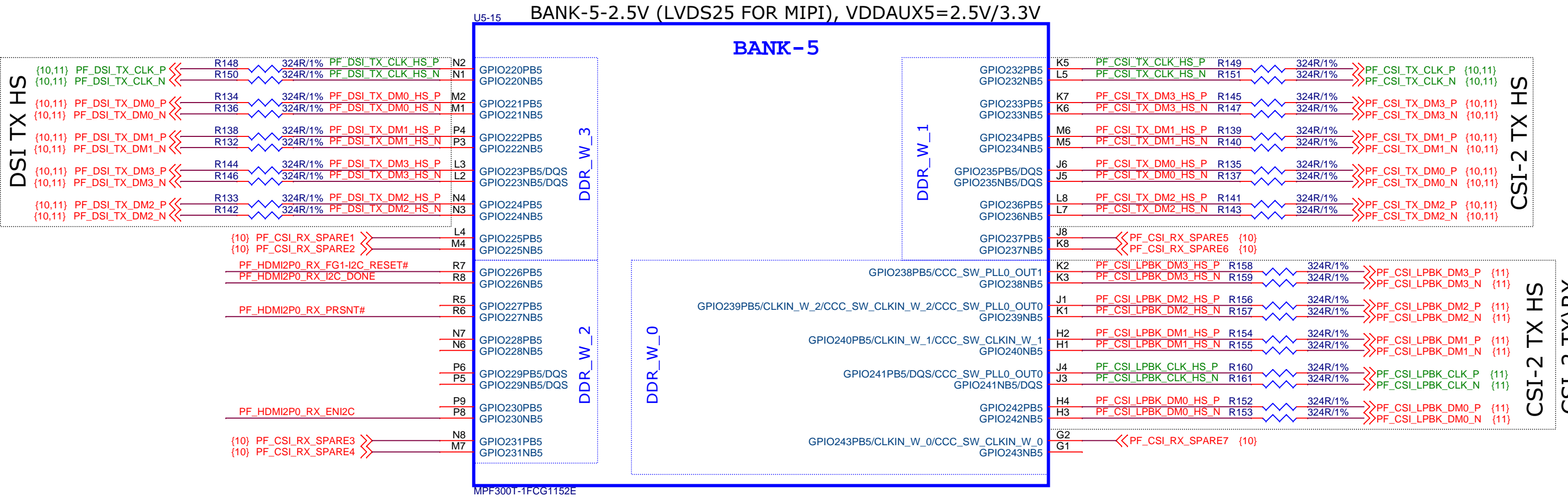


NOTE:
Nets PF_H6 & PF_G6 should be
routed differentially.
J9 & J11 should be
placed next to each other.

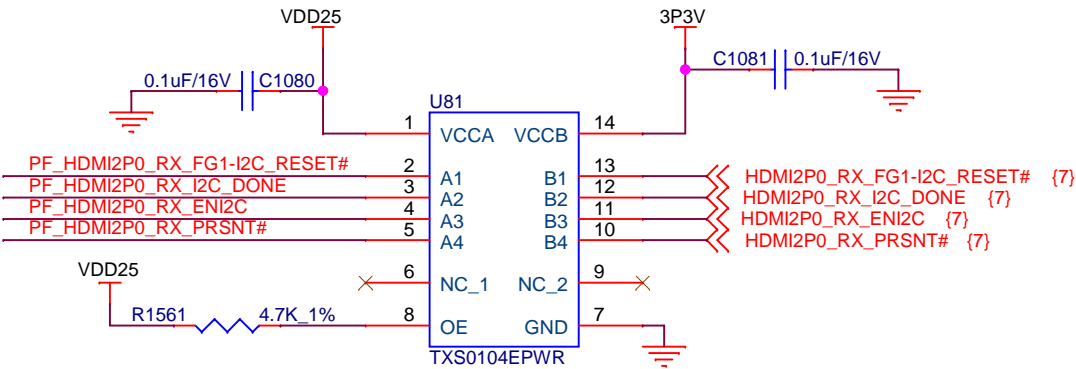


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BANK5 Connection

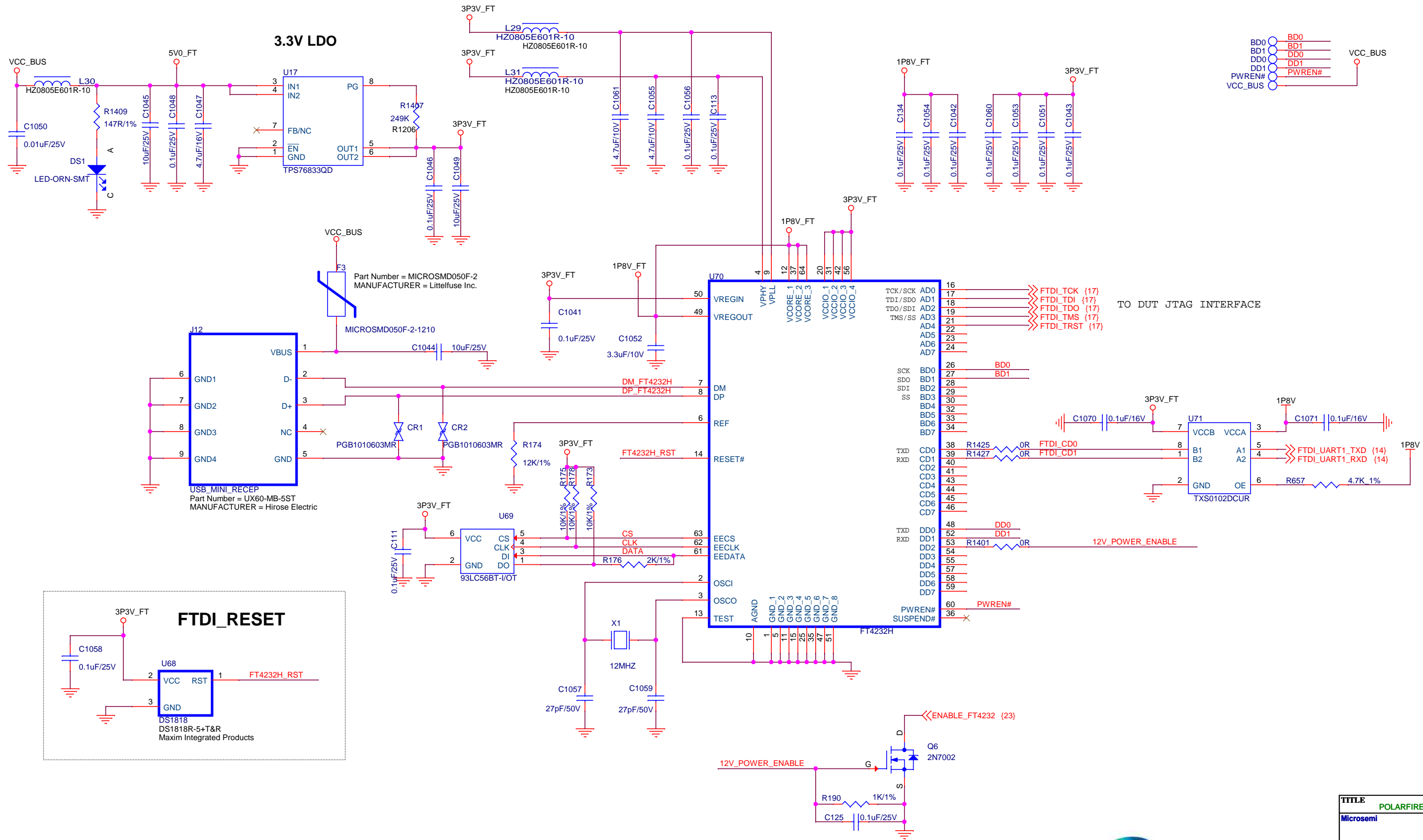


Level Translator - 3.3V Signals



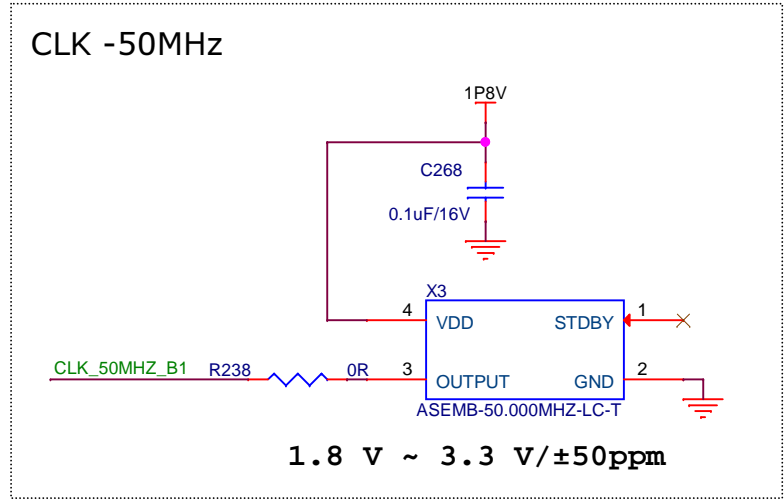
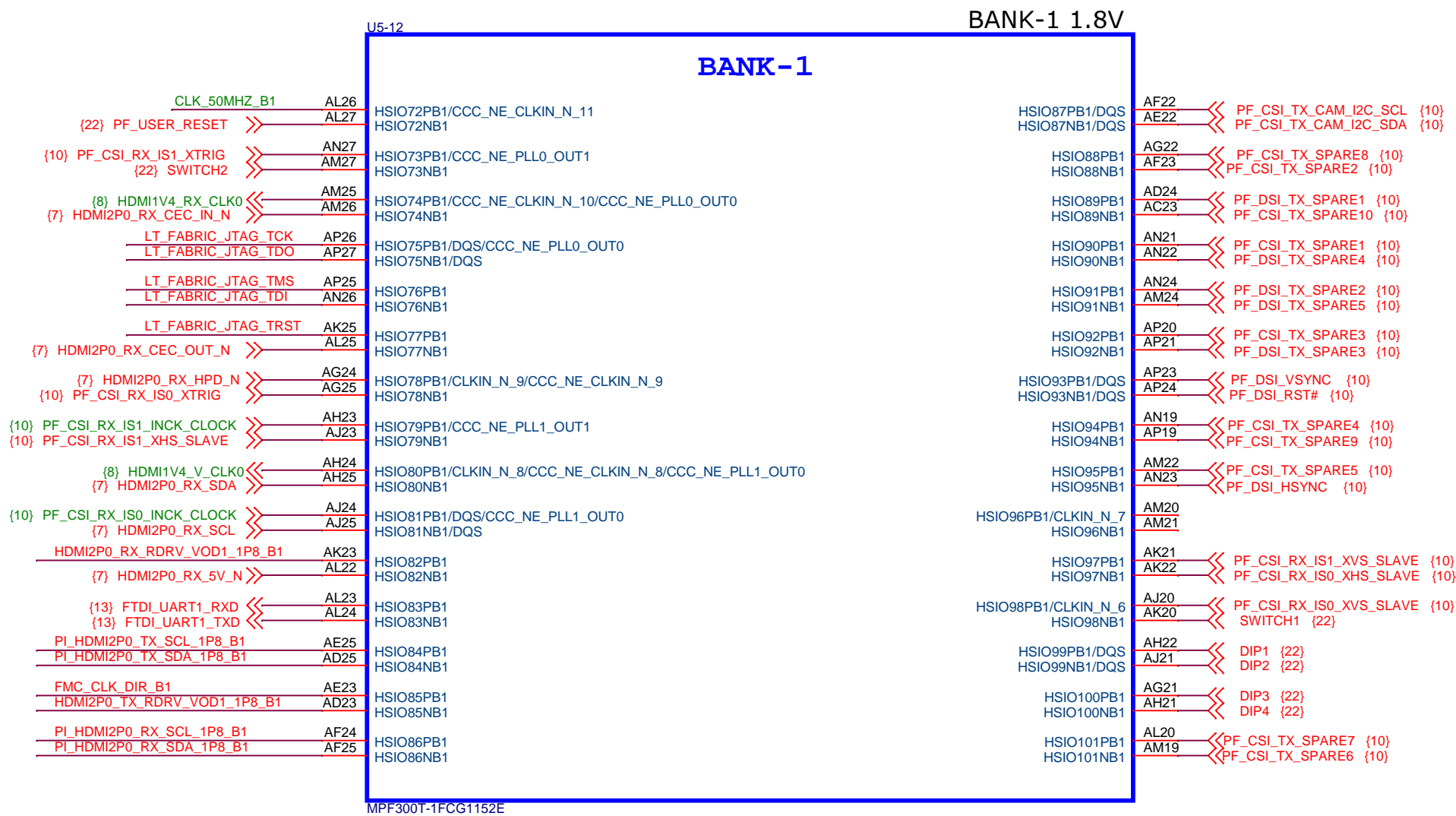
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FT4232H CIRCUITRY

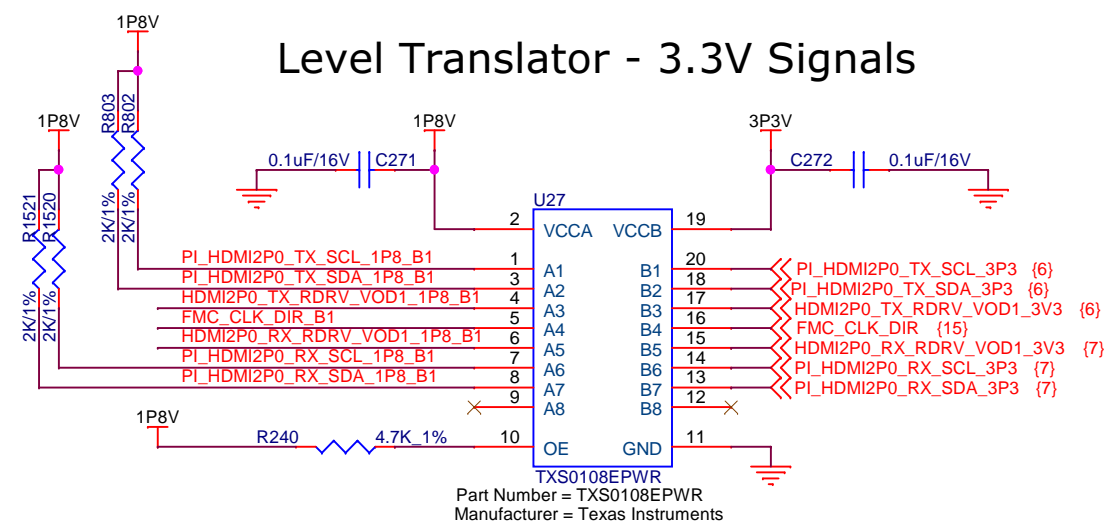


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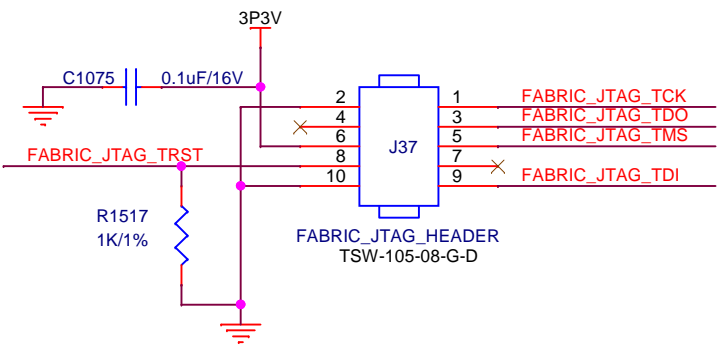
BANK1 Connection



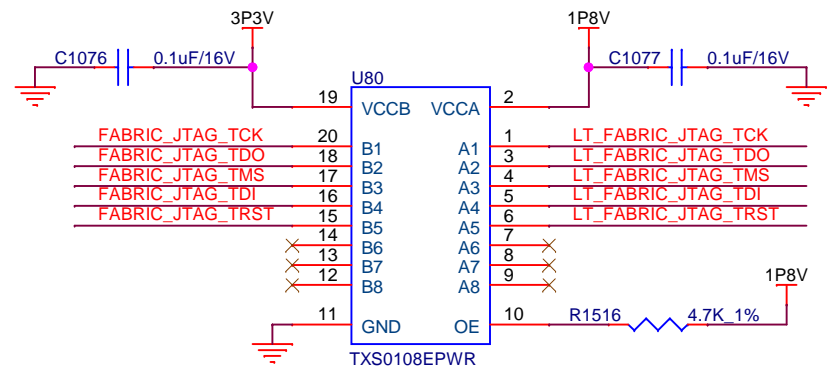
Level Translator - 3.3V Signals



FABRIC_JTAG_HEADER

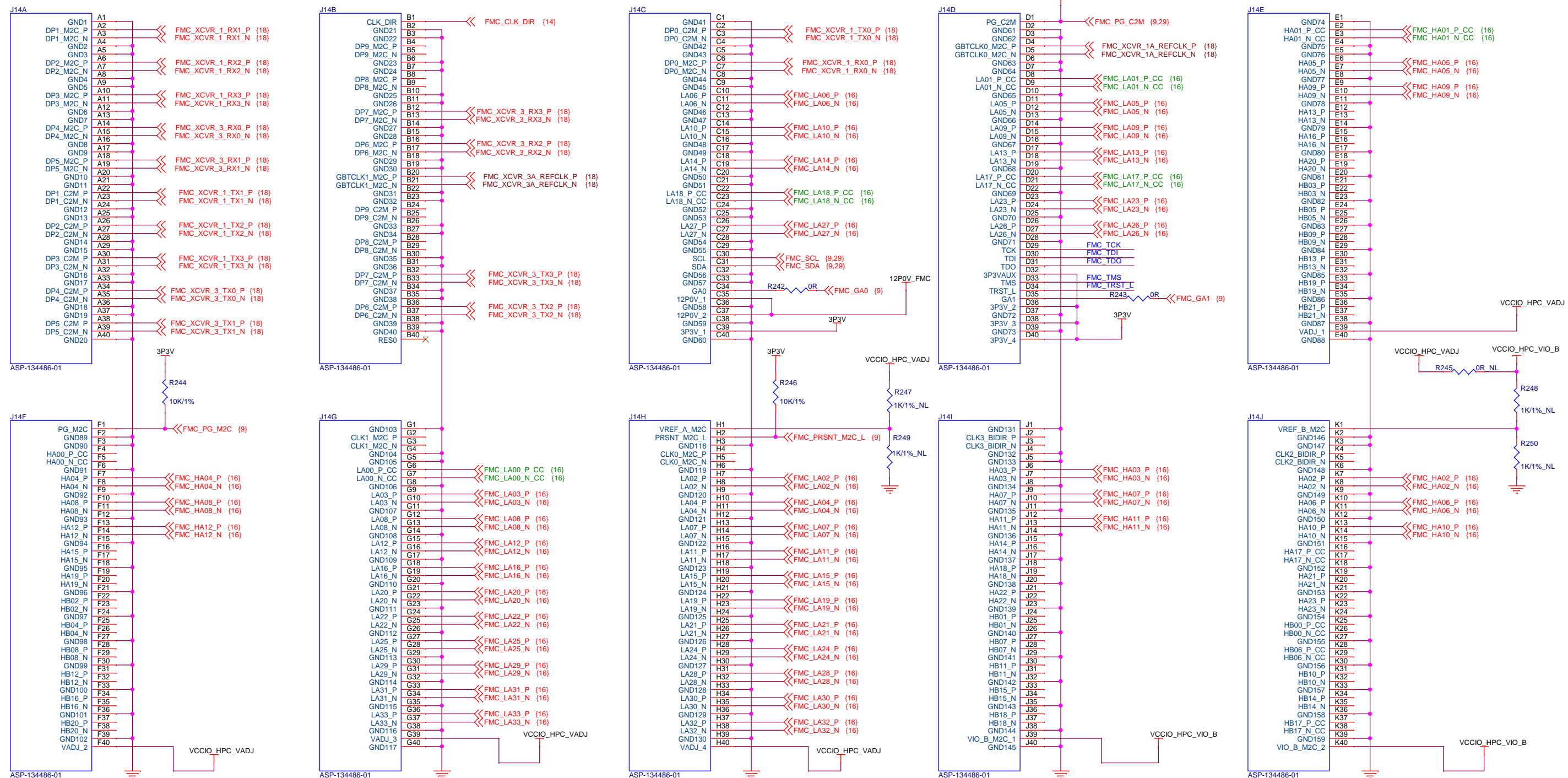


FABRIC_JTAG_HEADER-LEVEL TRANSLATOR

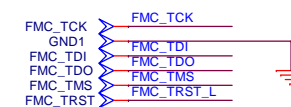
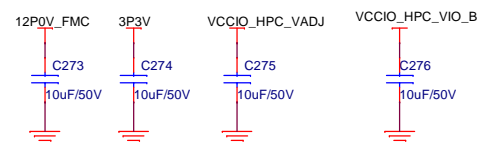


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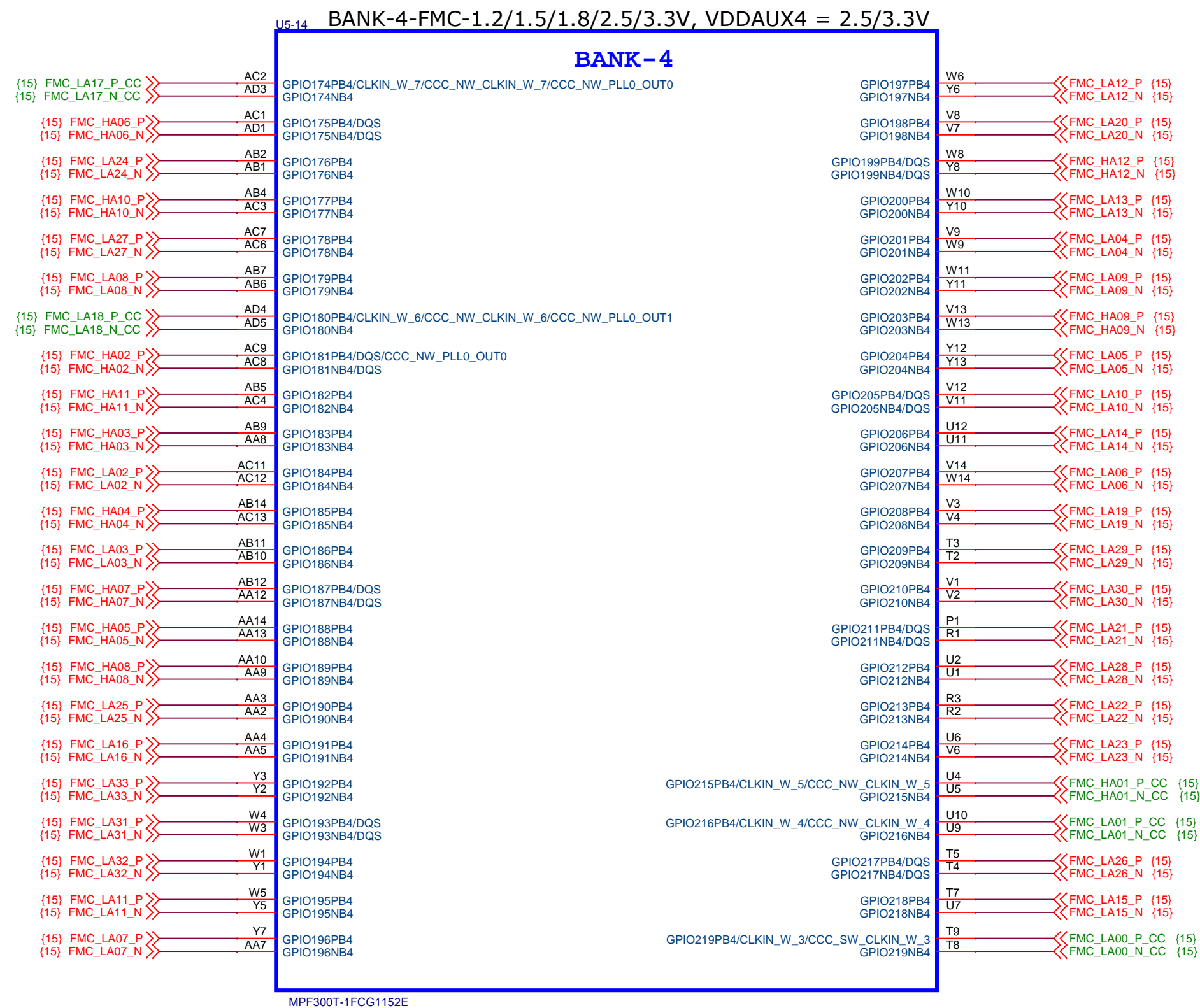
FMC Connection (HPC)



Decoupling Capacitor

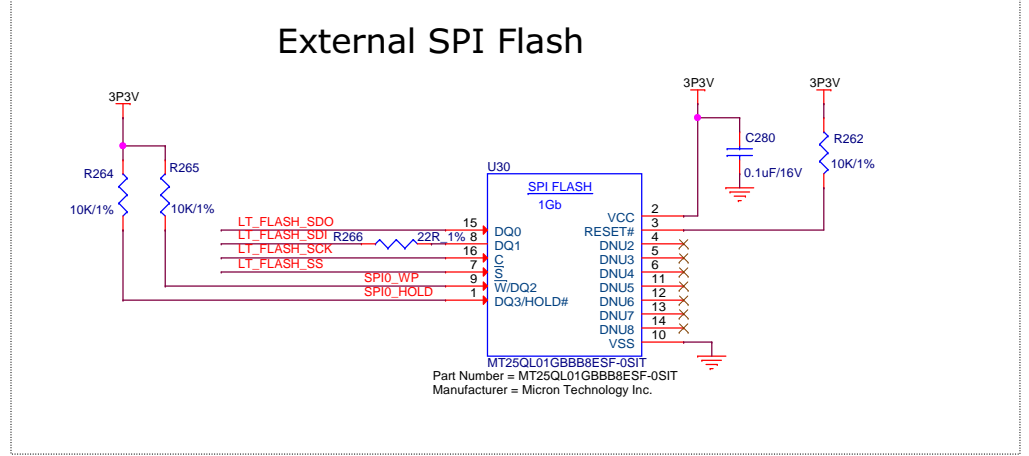
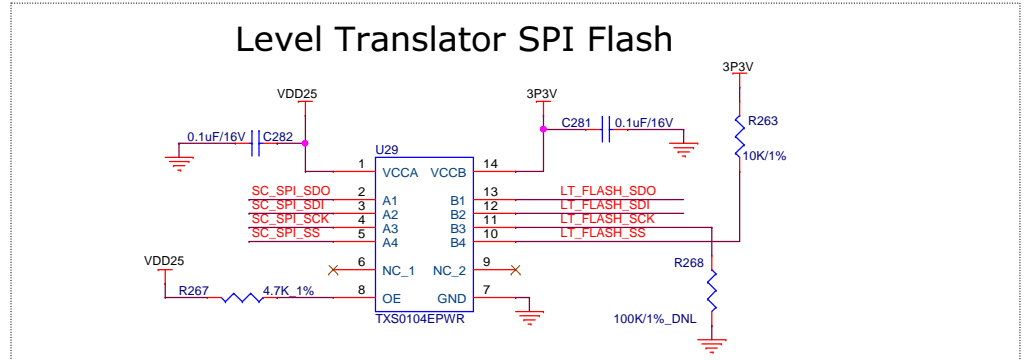
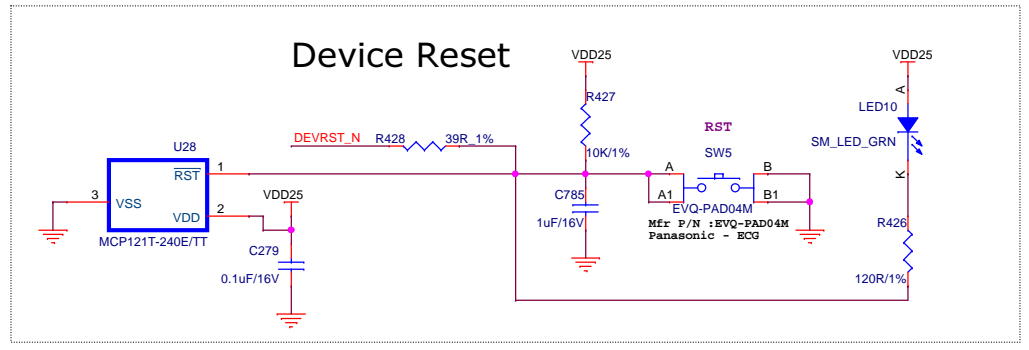
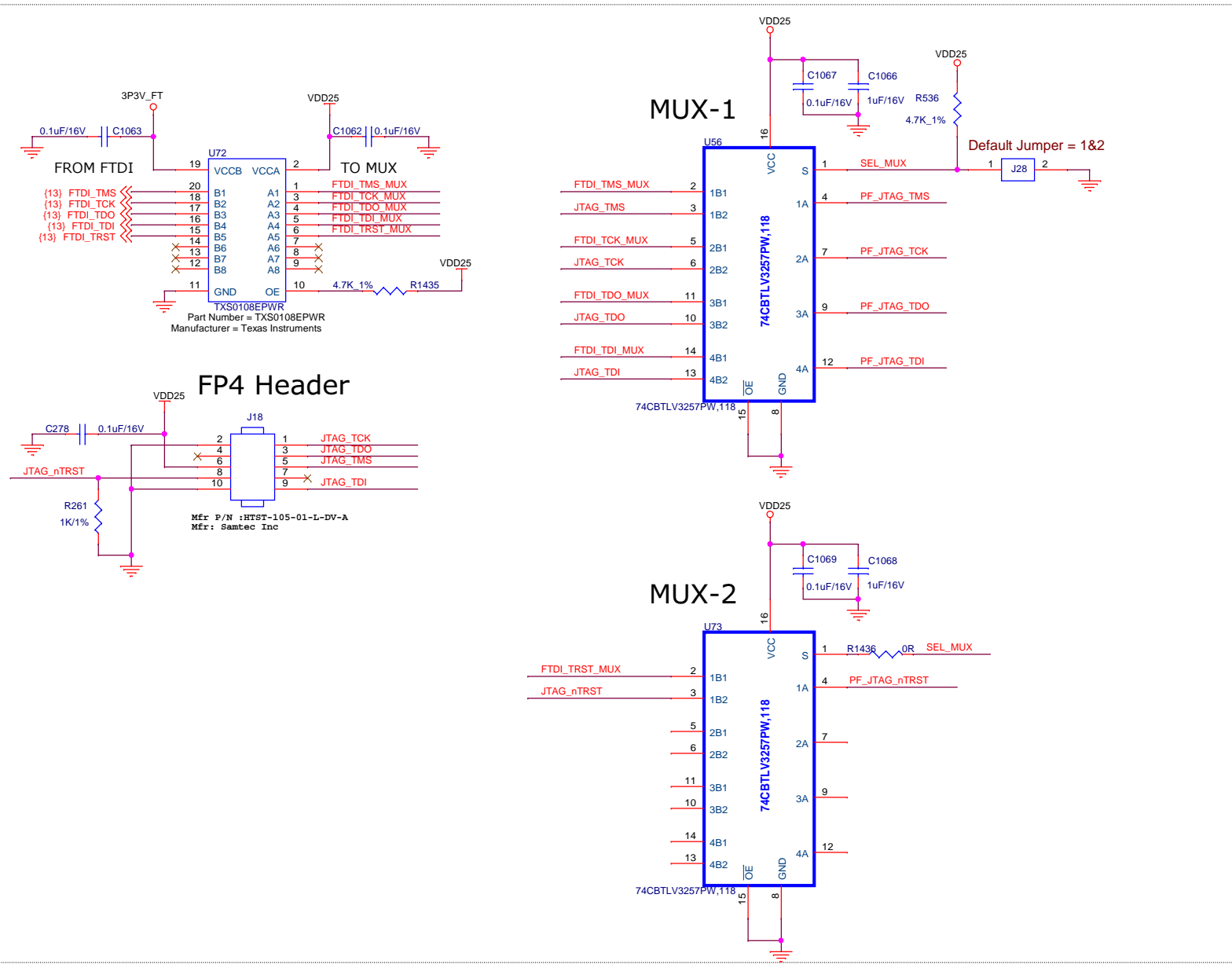
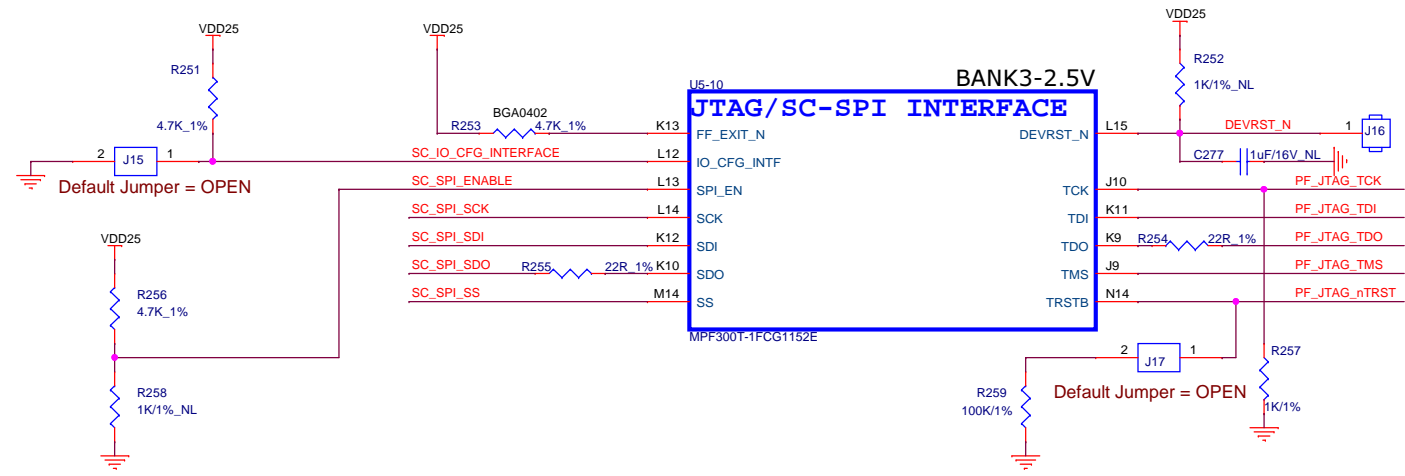


BANK4 Connection



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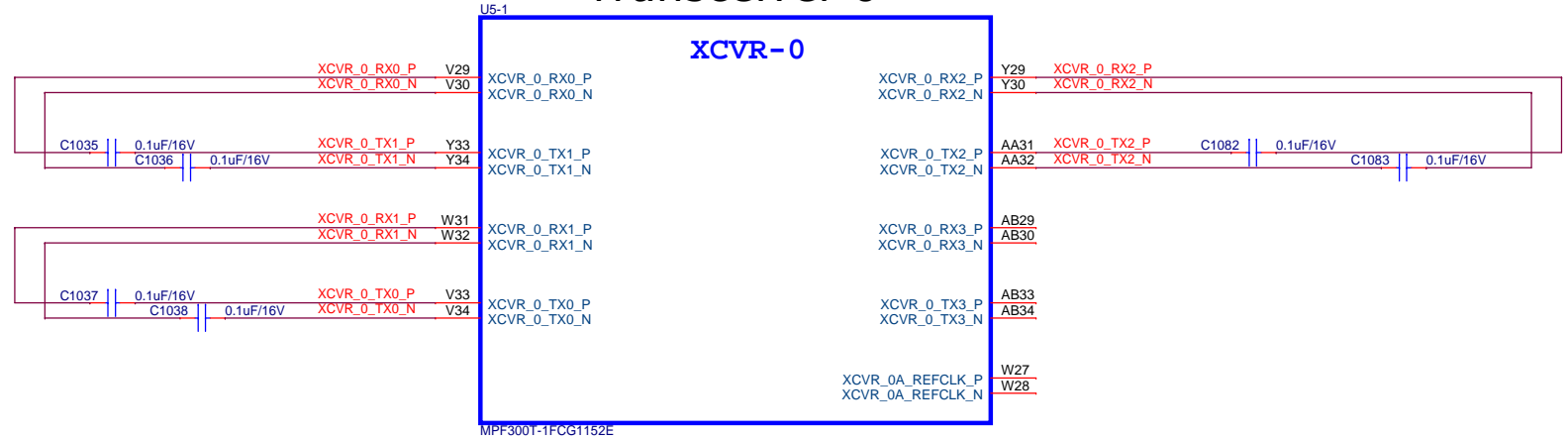
Programming Section



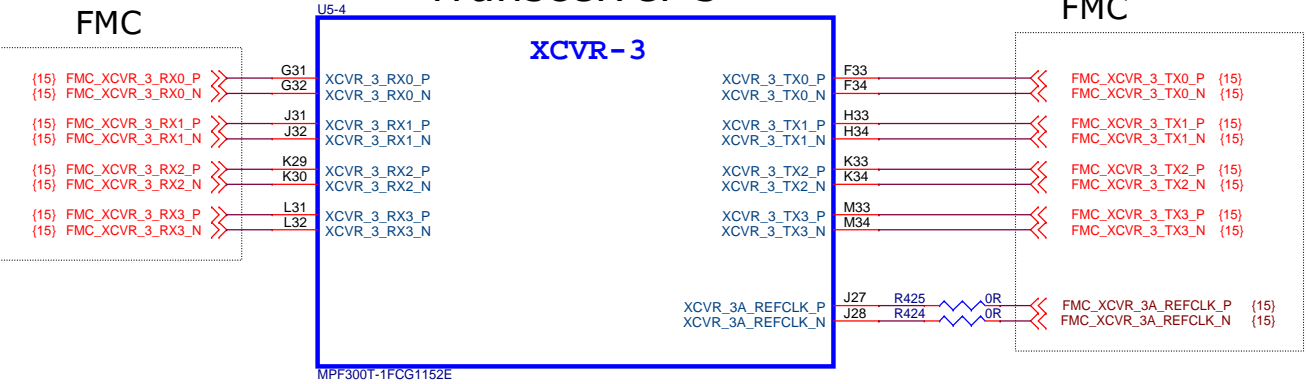
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Transceiver & External Reference Clocks

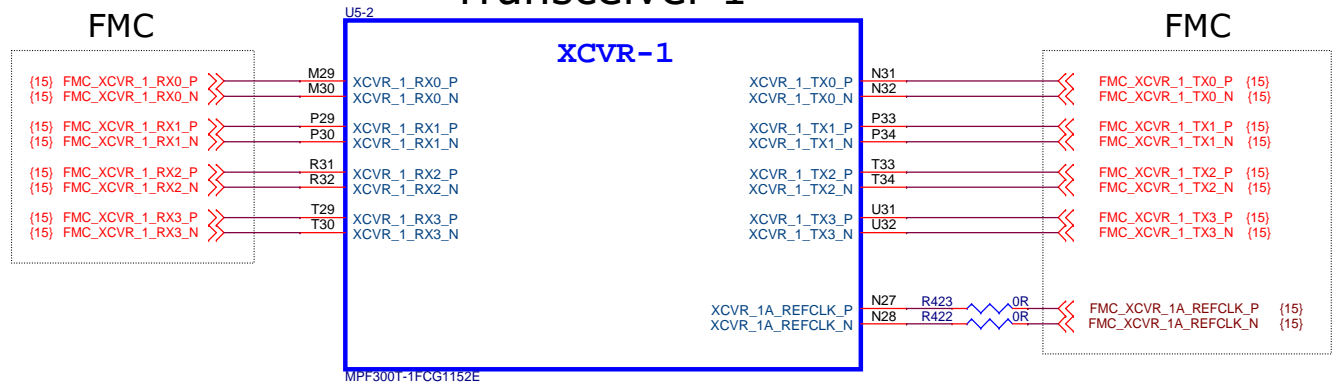
Transceiver 0



Transceiver 3

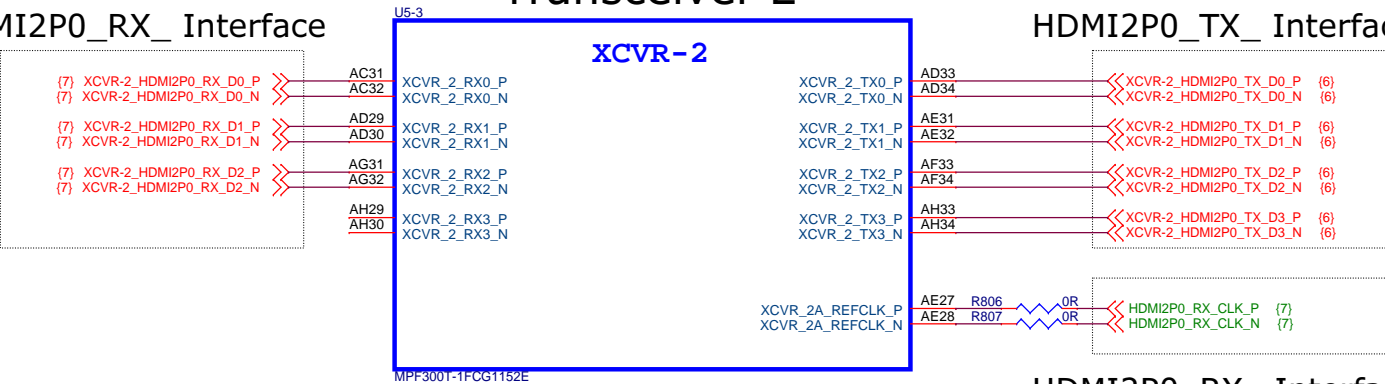


Transceiver 1



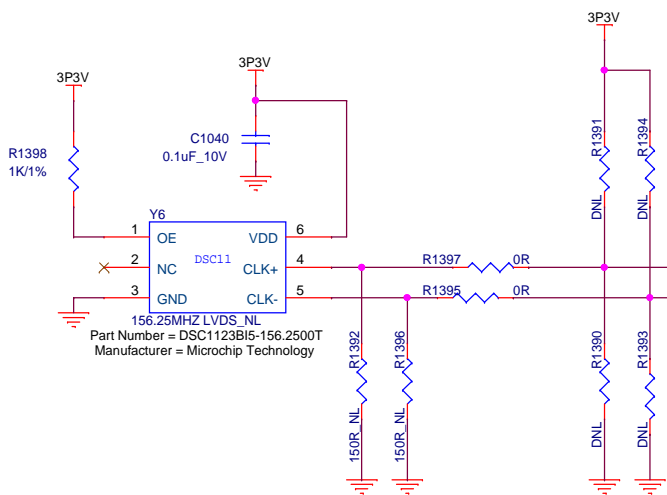
HDMI2P0_RX_ Interface

Transceiver 2

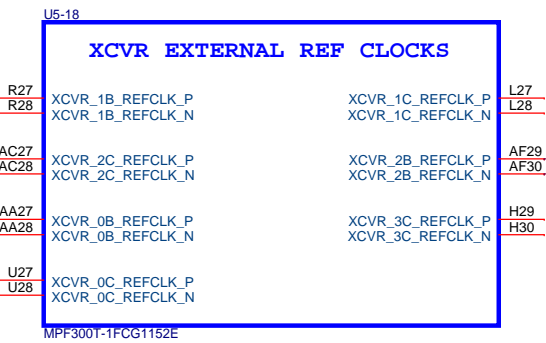


HDMI2P0_RX_ Interface

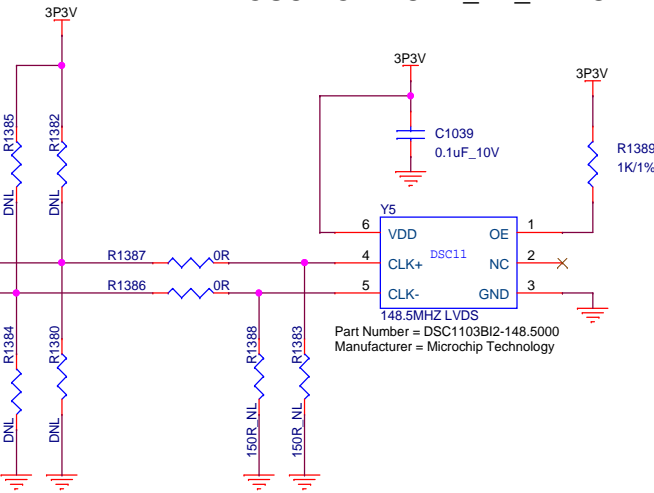
OSC FOR XCVR_0B_REFCLK



Transceiver External Reference Clocks

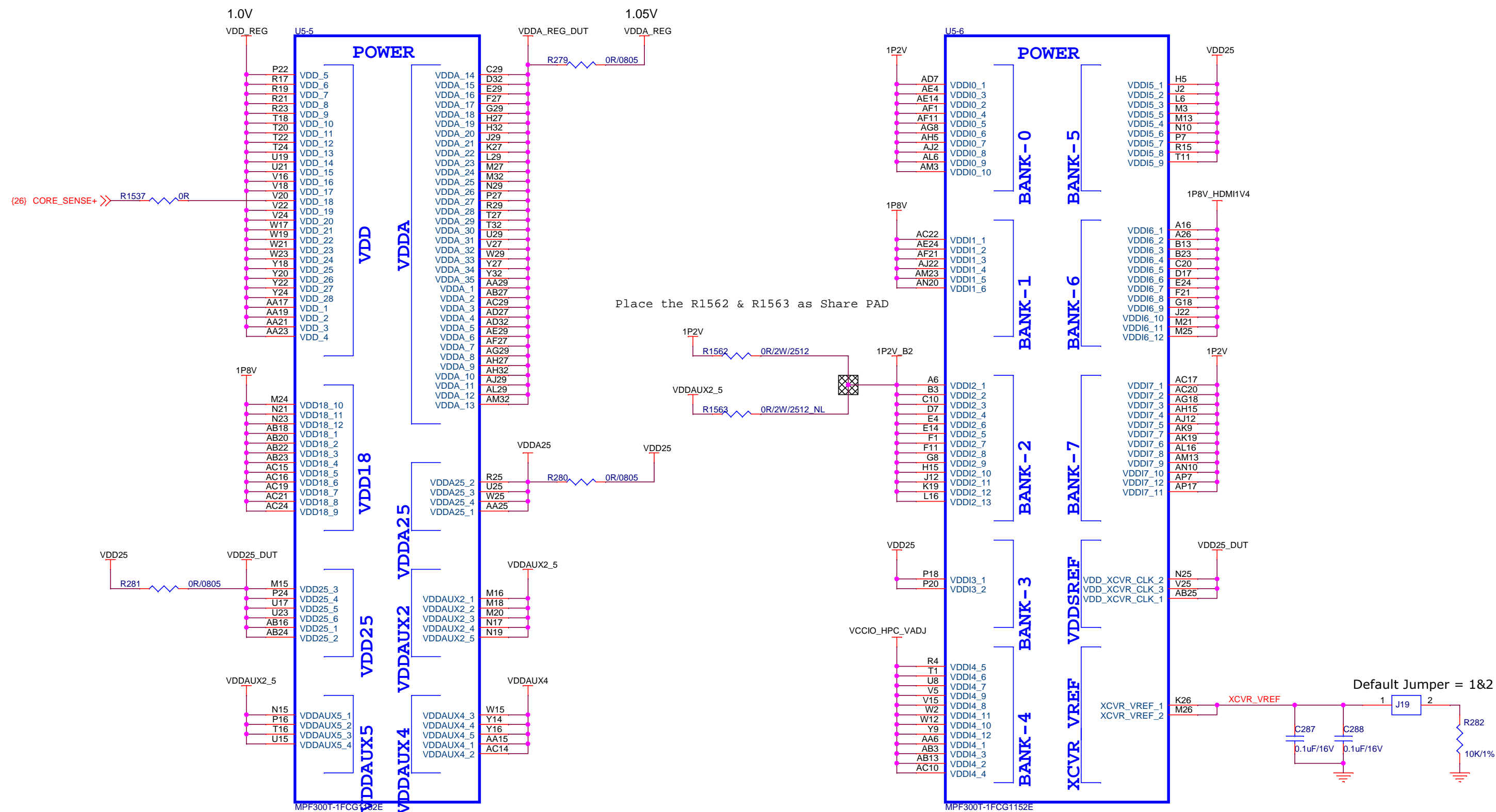


OSC FOR XCVR_2B_REFCLK



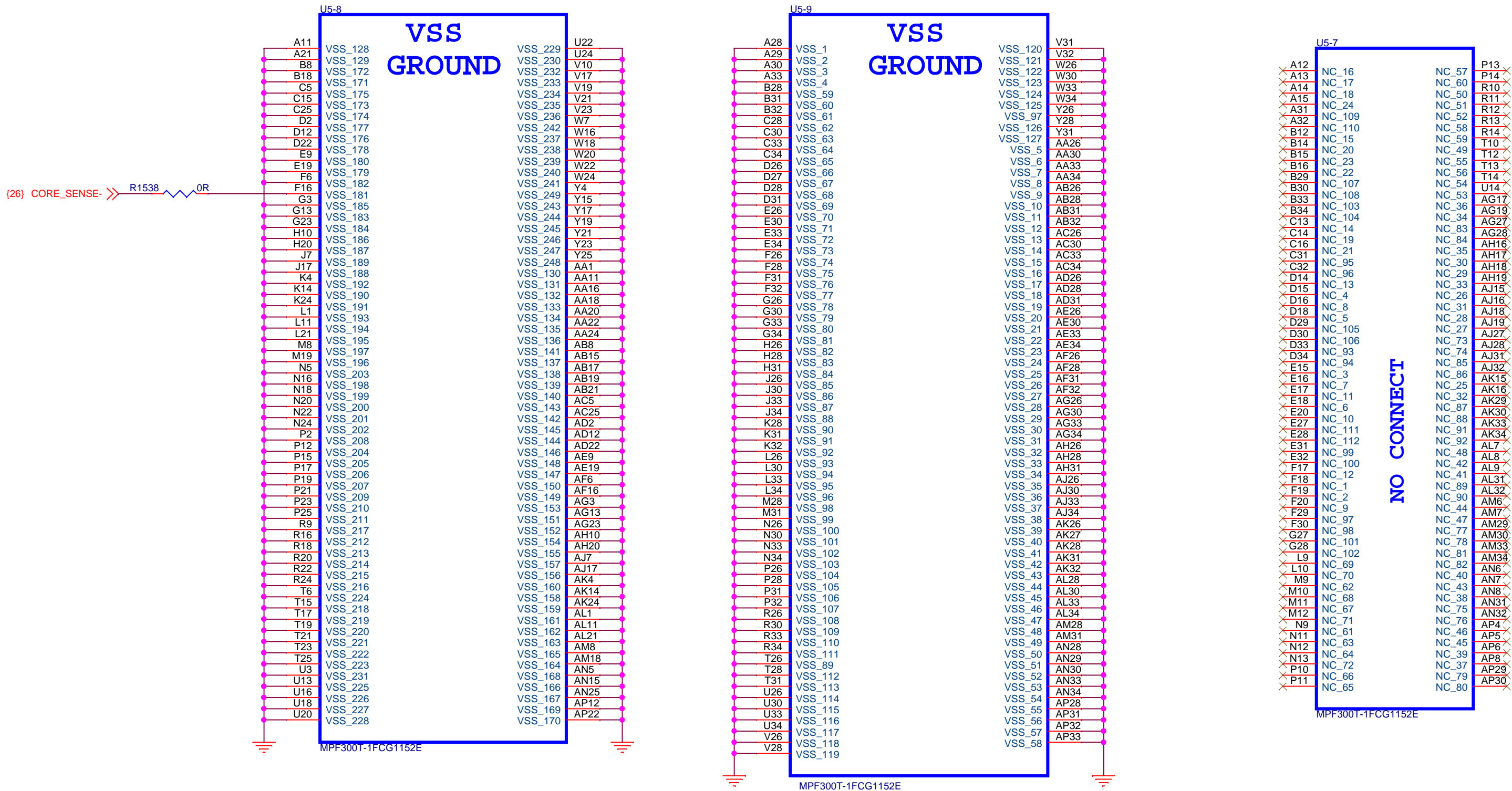
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PolarFire Power Connection



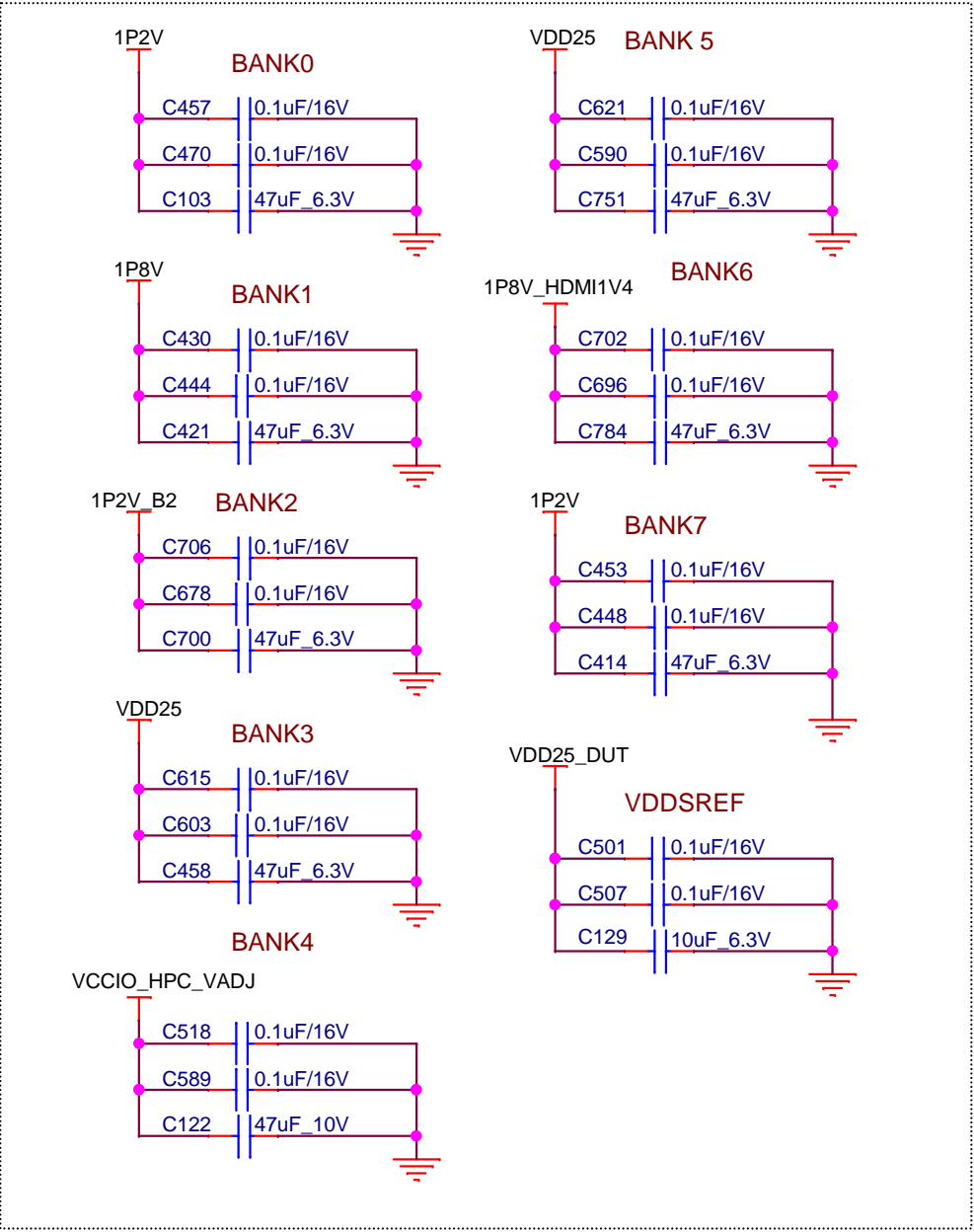
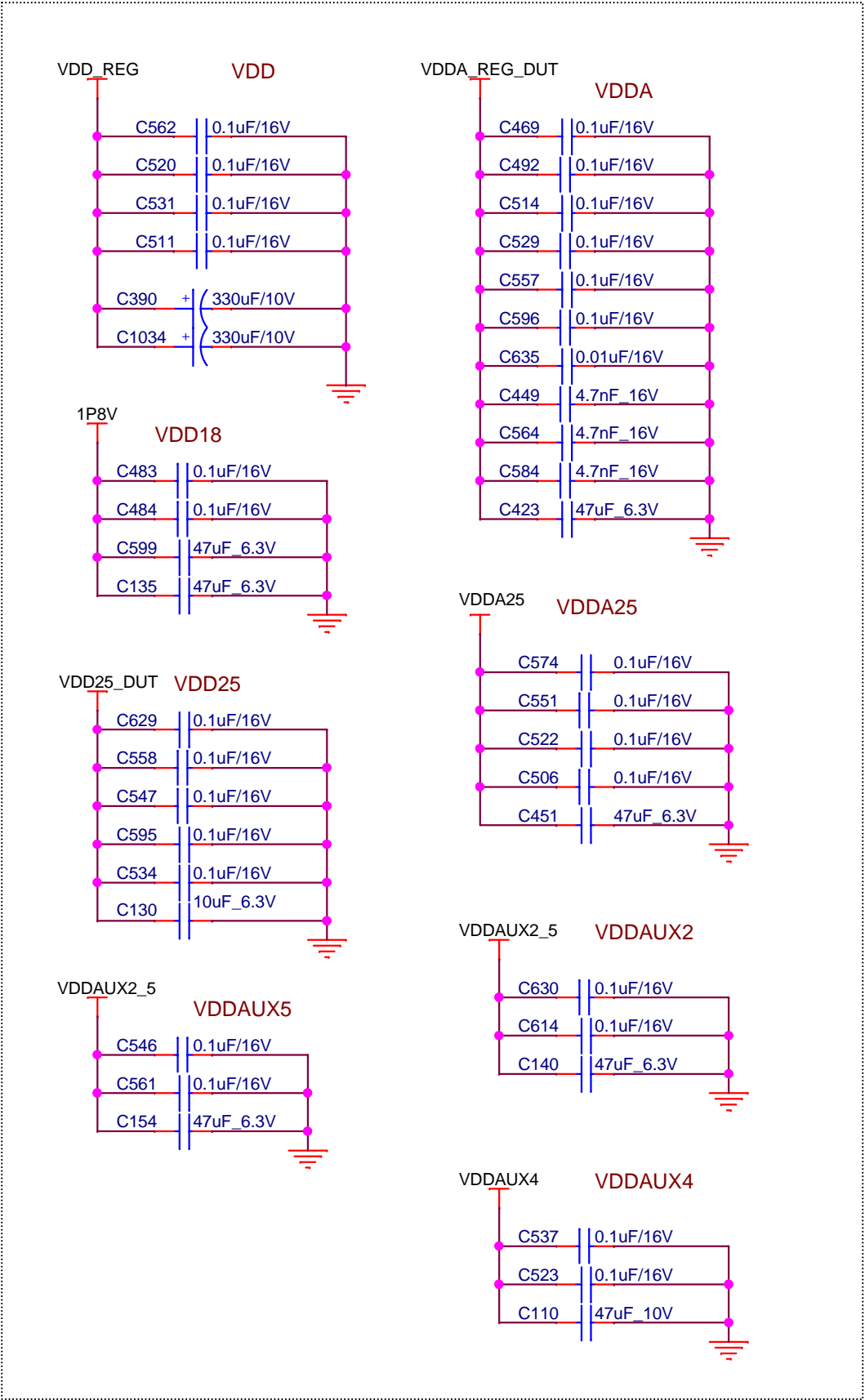
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PolarFire Ground & NC Connection



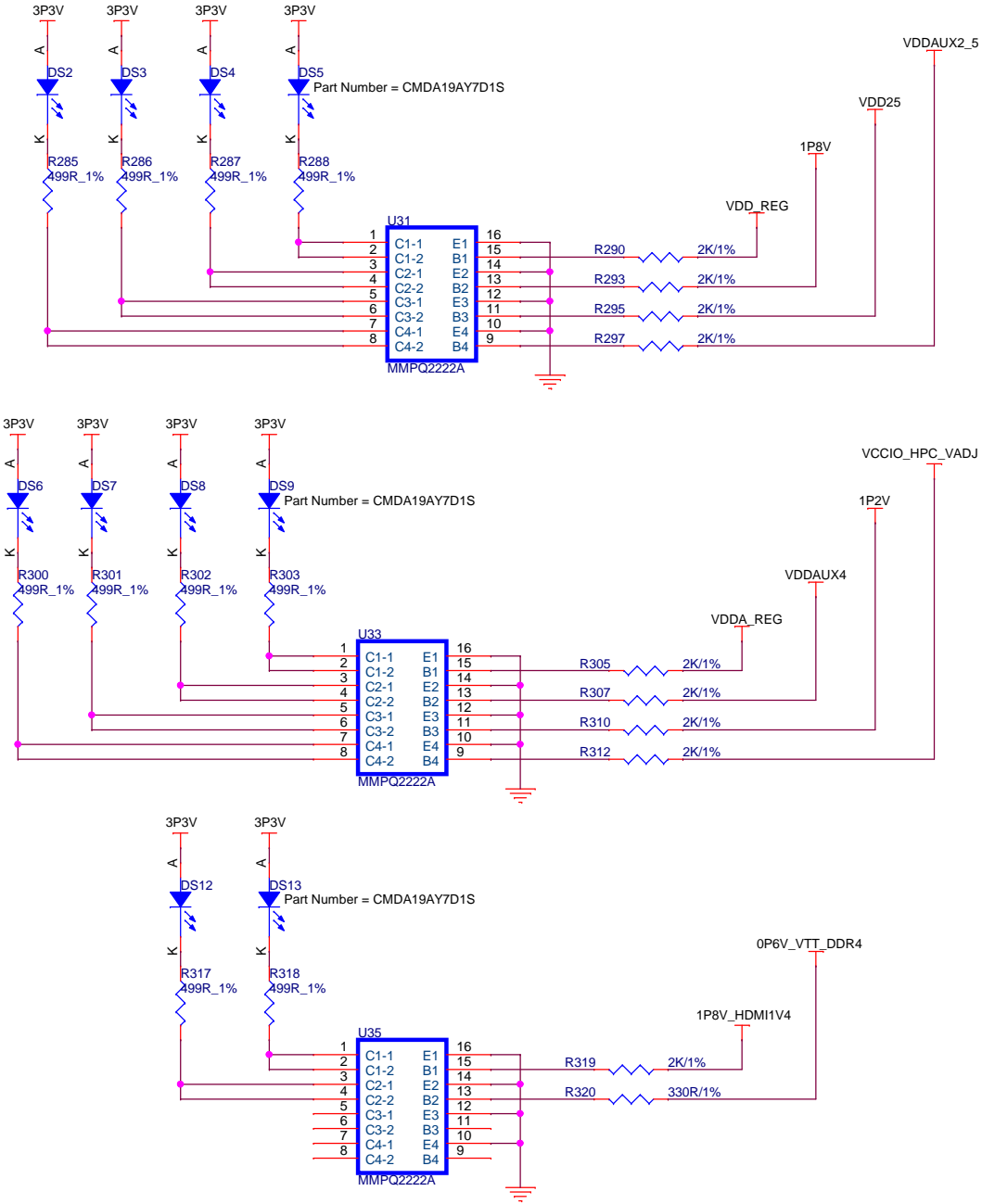
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PolarFire Decoupling Capacitors

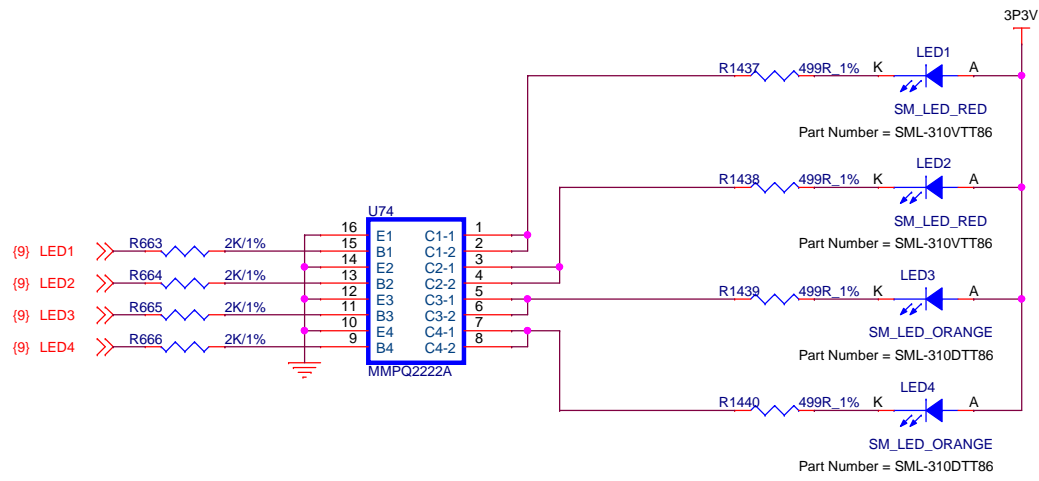


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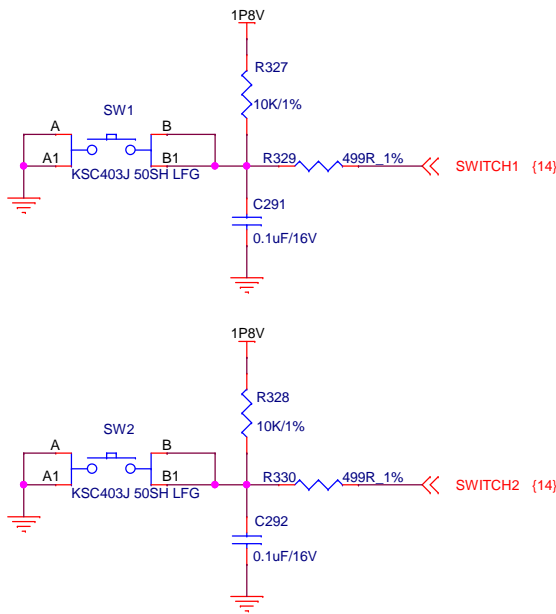
Power LEDs



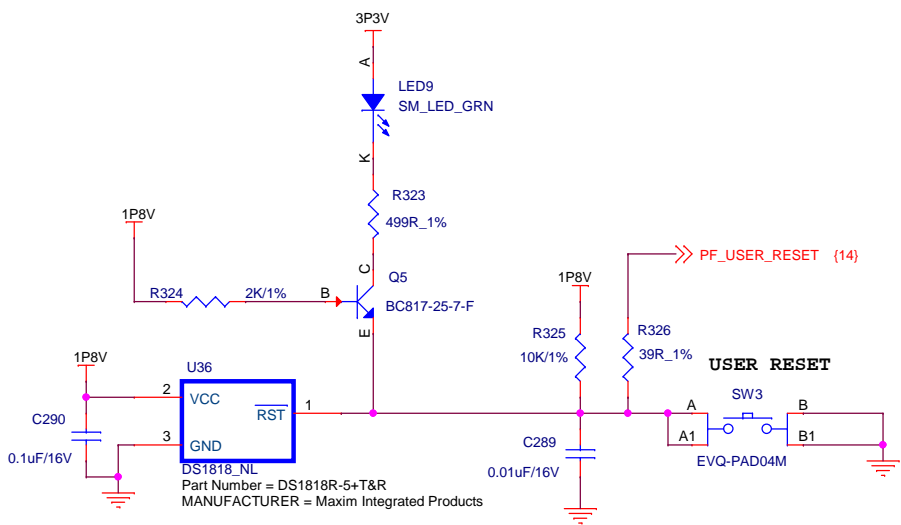
User Defined LEDs



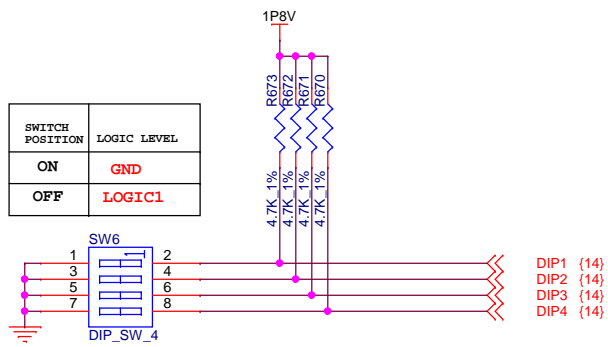
Debug Circuitry



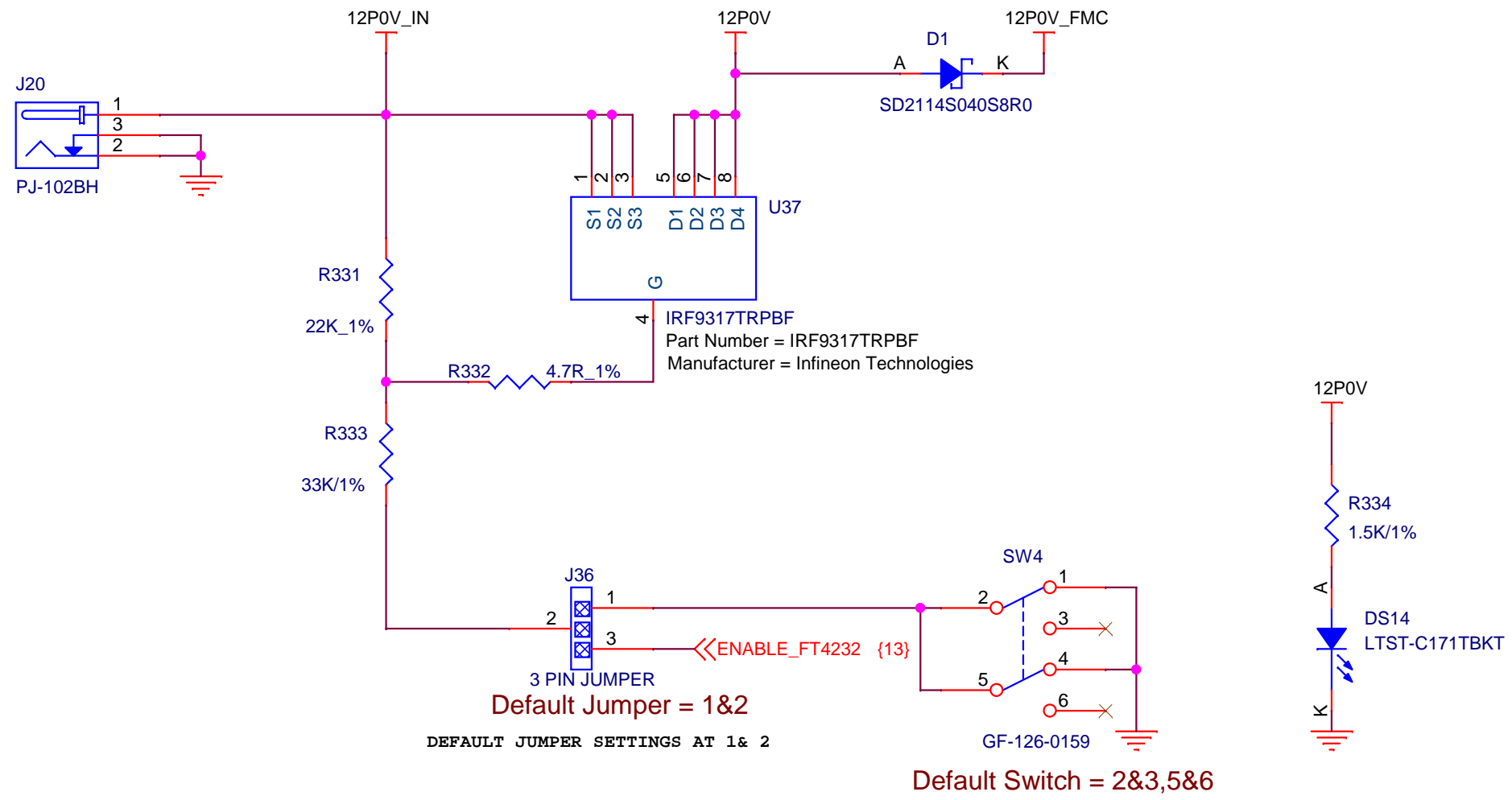
PolarFire User Reset



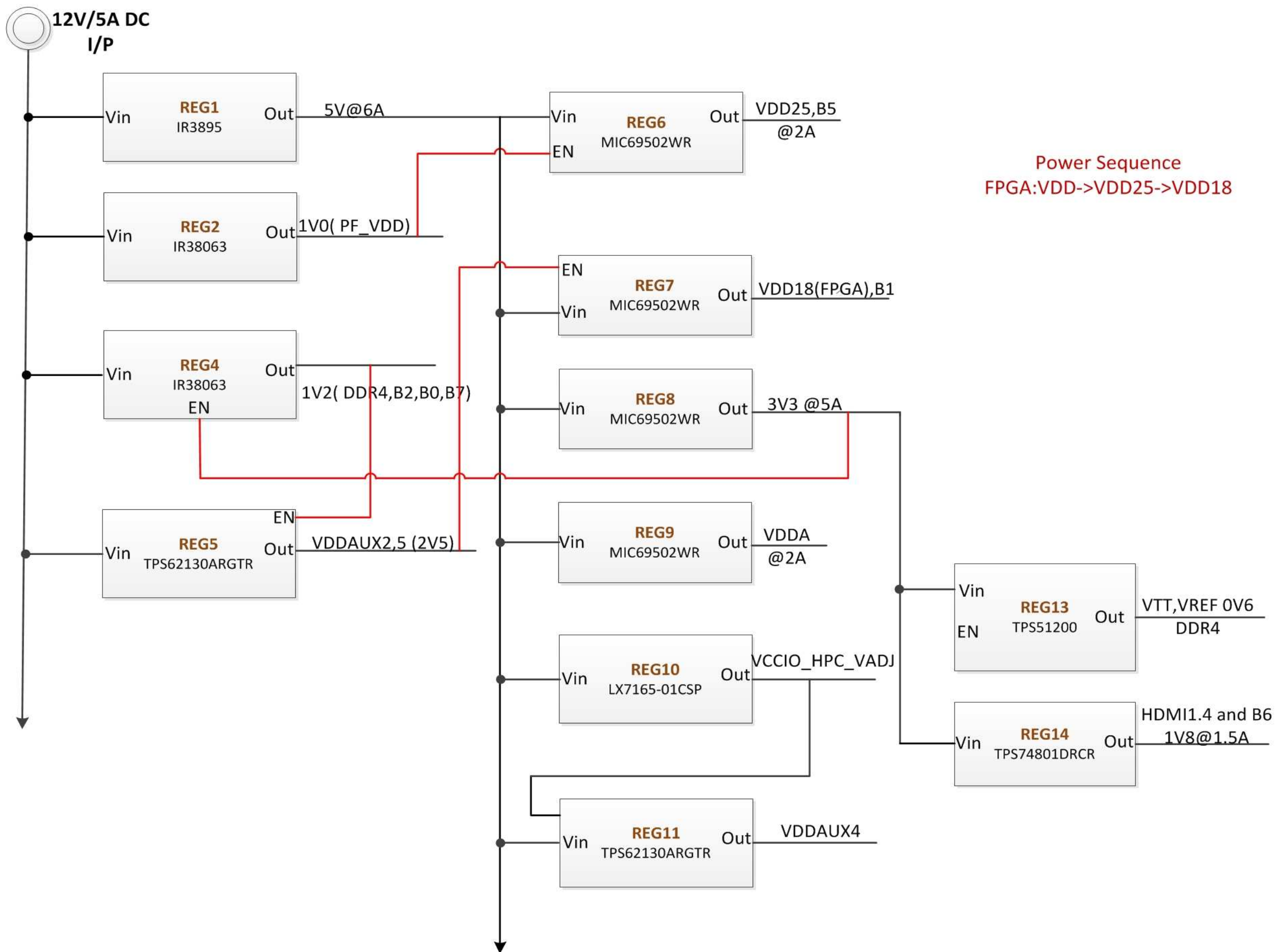
DIP Switch



12V External Supply @ 5A



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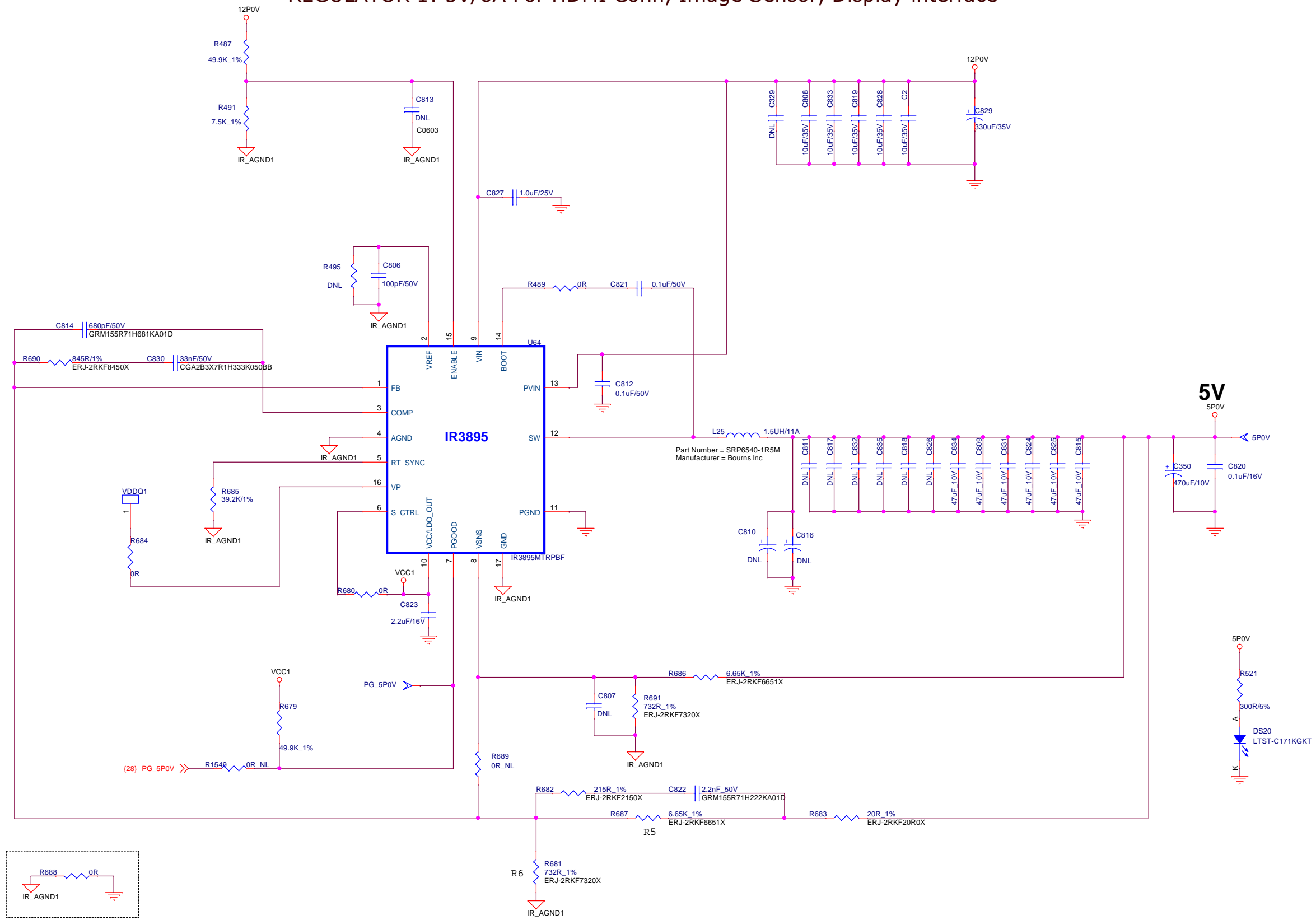


Power Sequence
FPGA:VDD->VDD25->VDD18



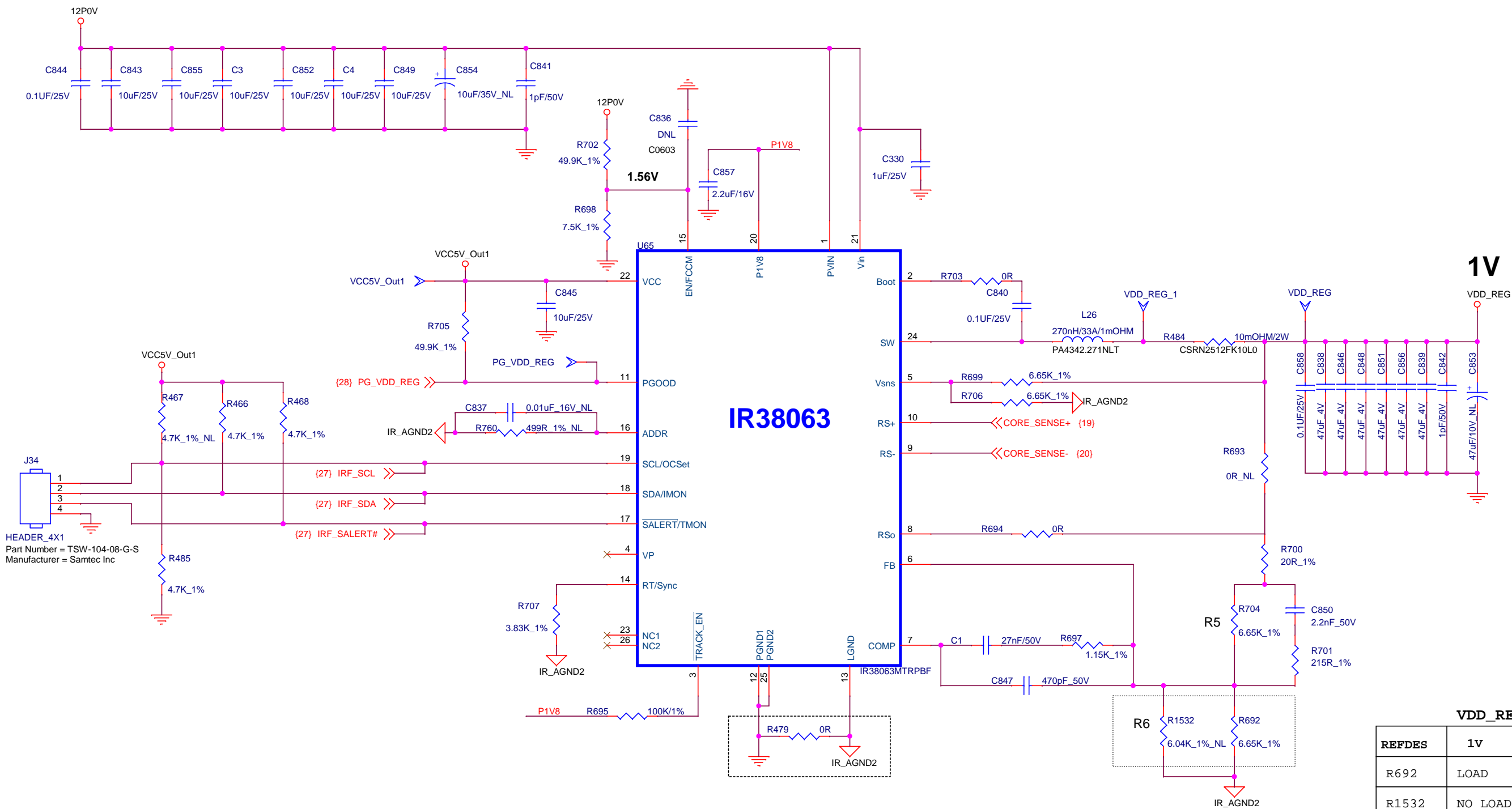
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REGULATOR 1: 5V/6A For HDMI Conn, Image Sensor, Display interface



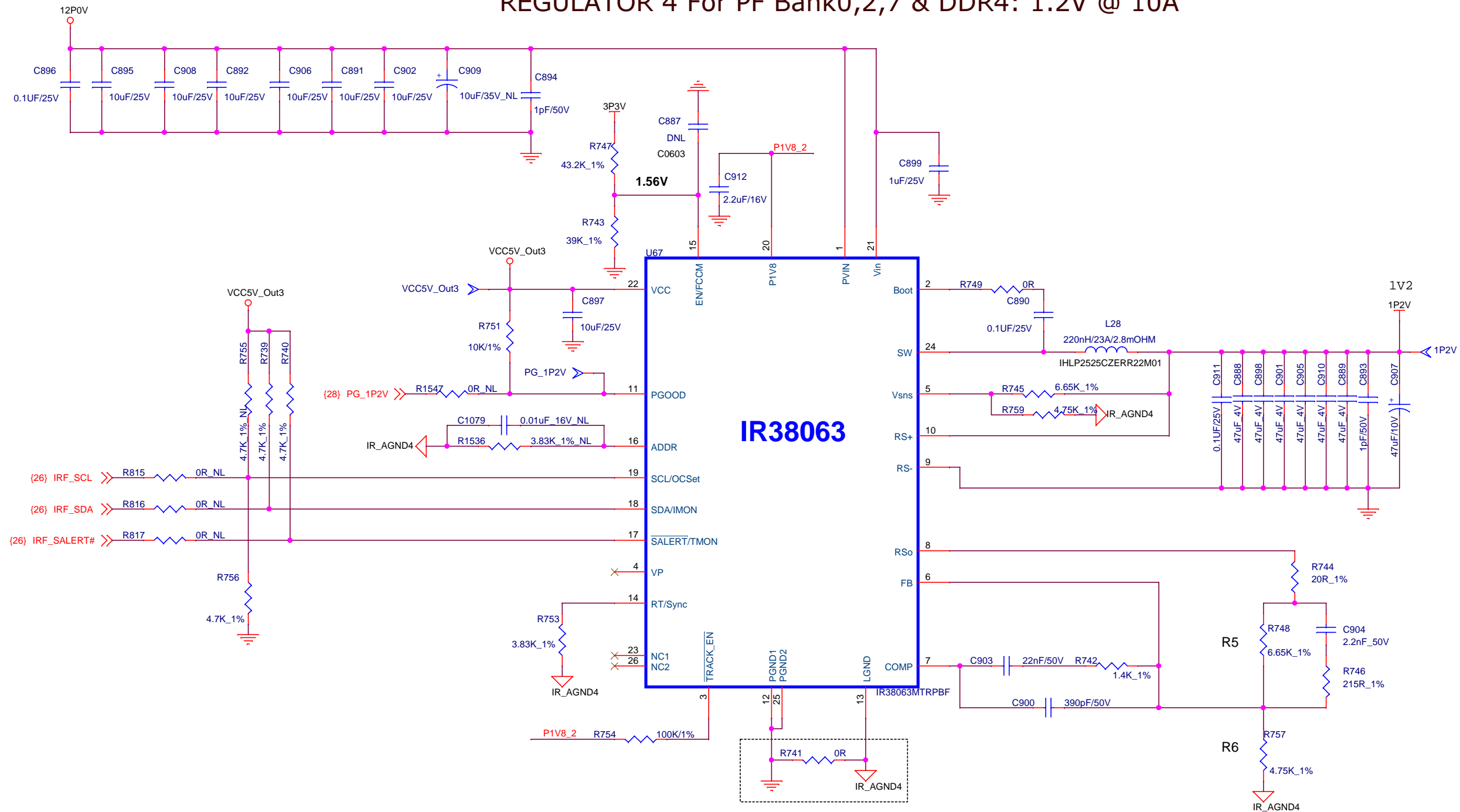
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DATE:	Friday, February 22, 2019		SH 25 OF 29

REGULATOR 2 For PF_VDD: 1.0V/10A

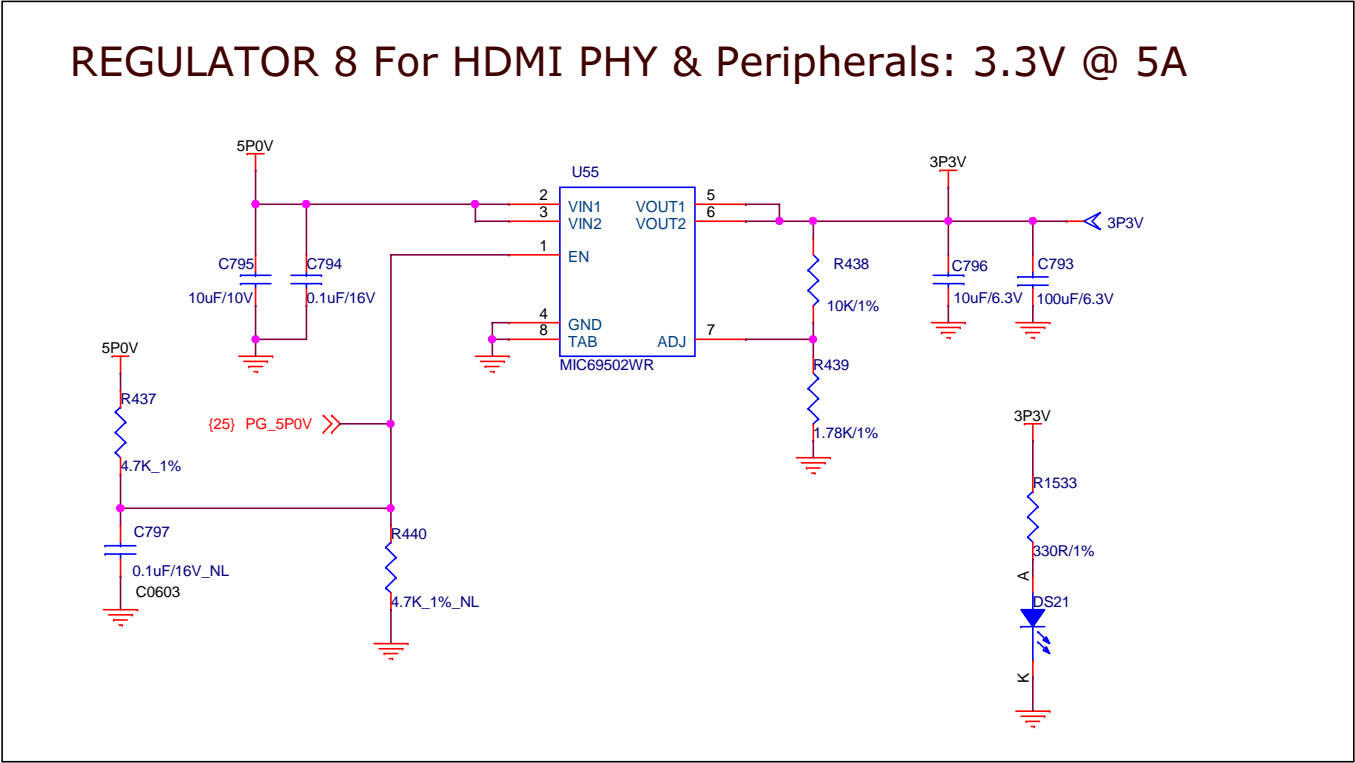
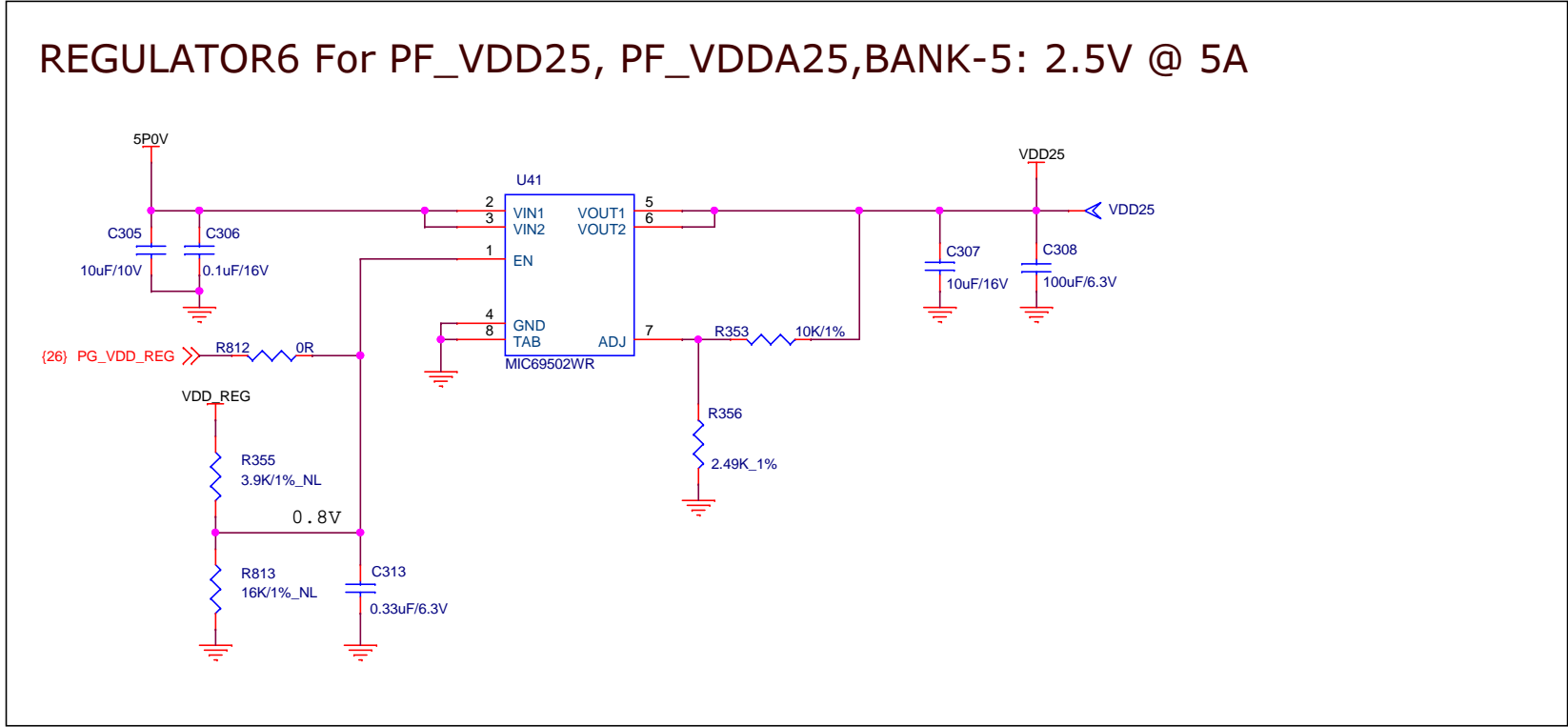
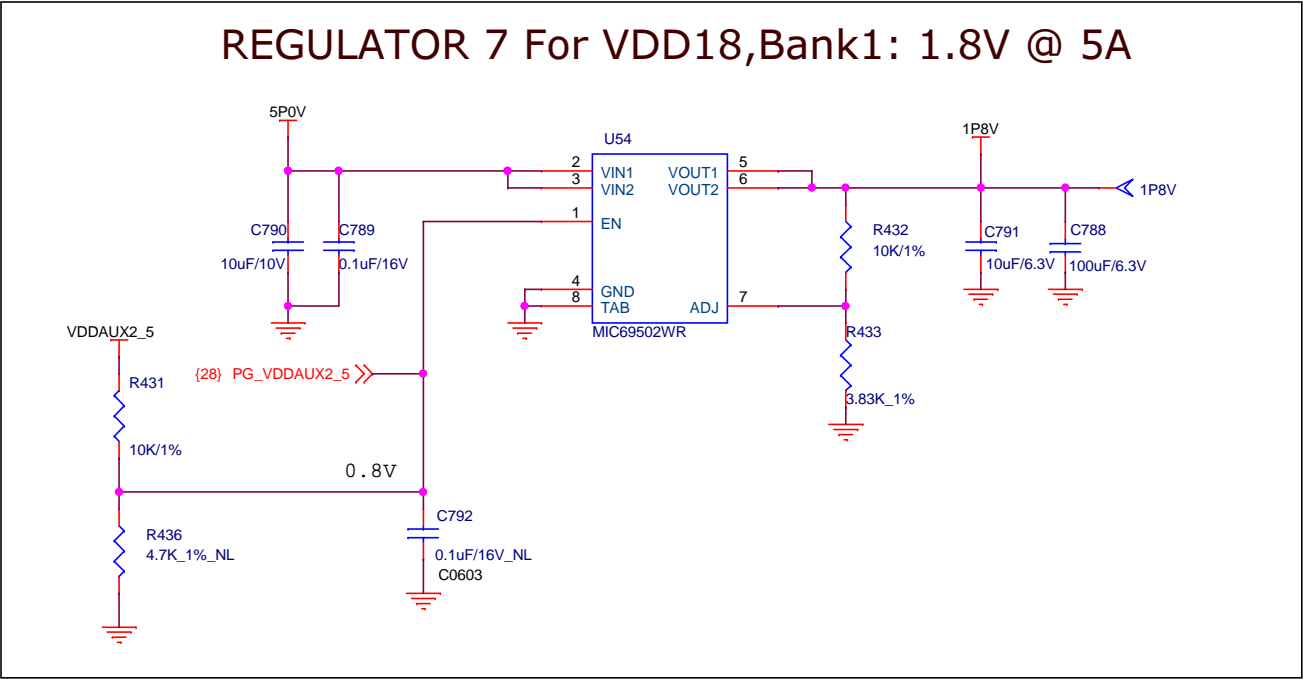
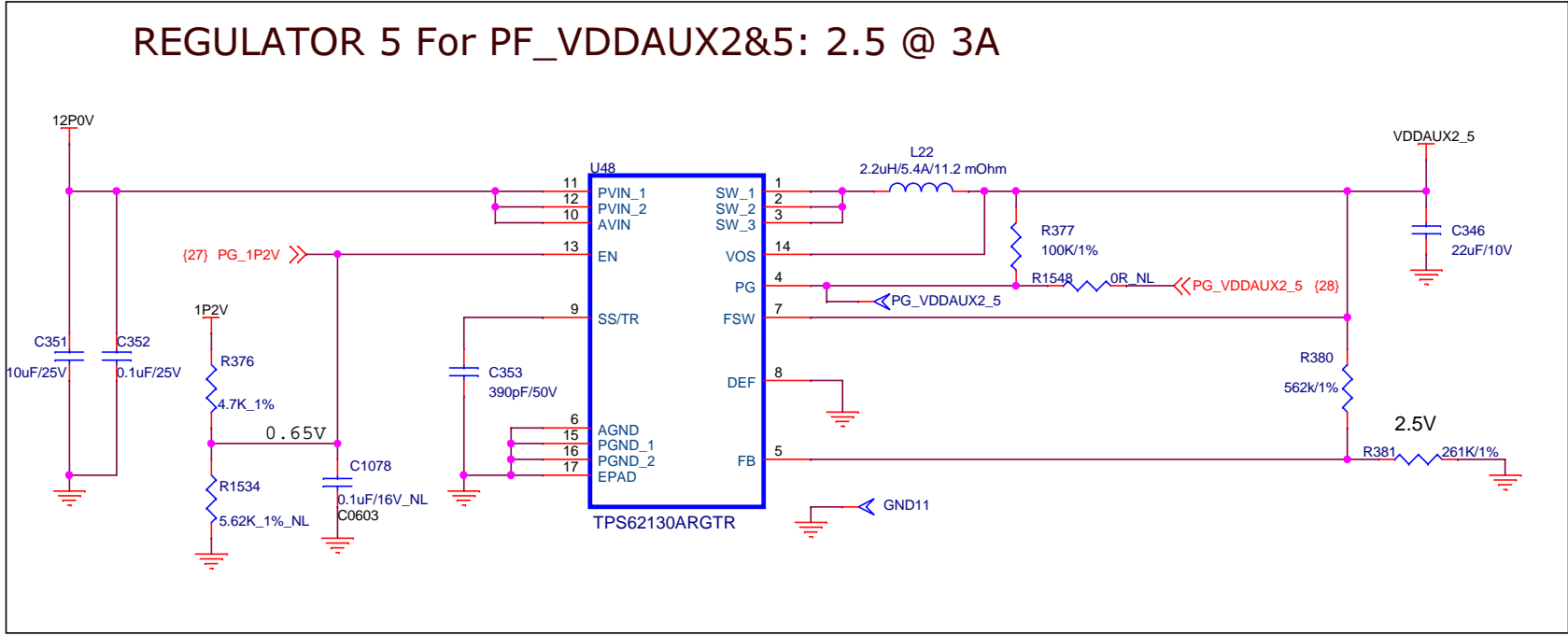


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REGULATOR 4 For PF Bank0,2,7 & DDR4: 1.2V @ 10A

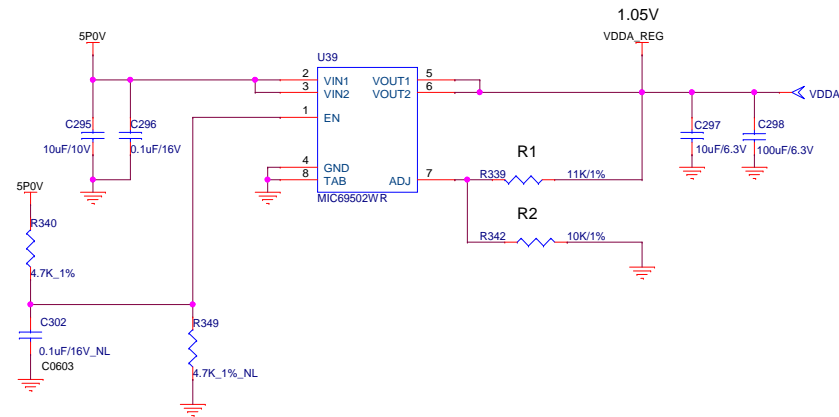


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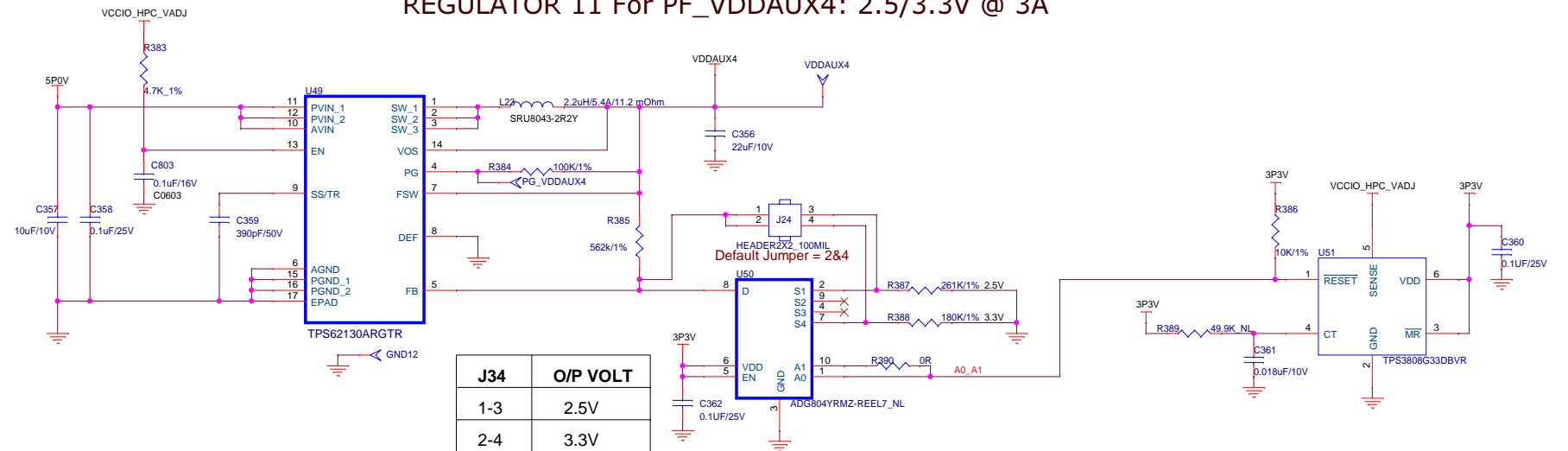


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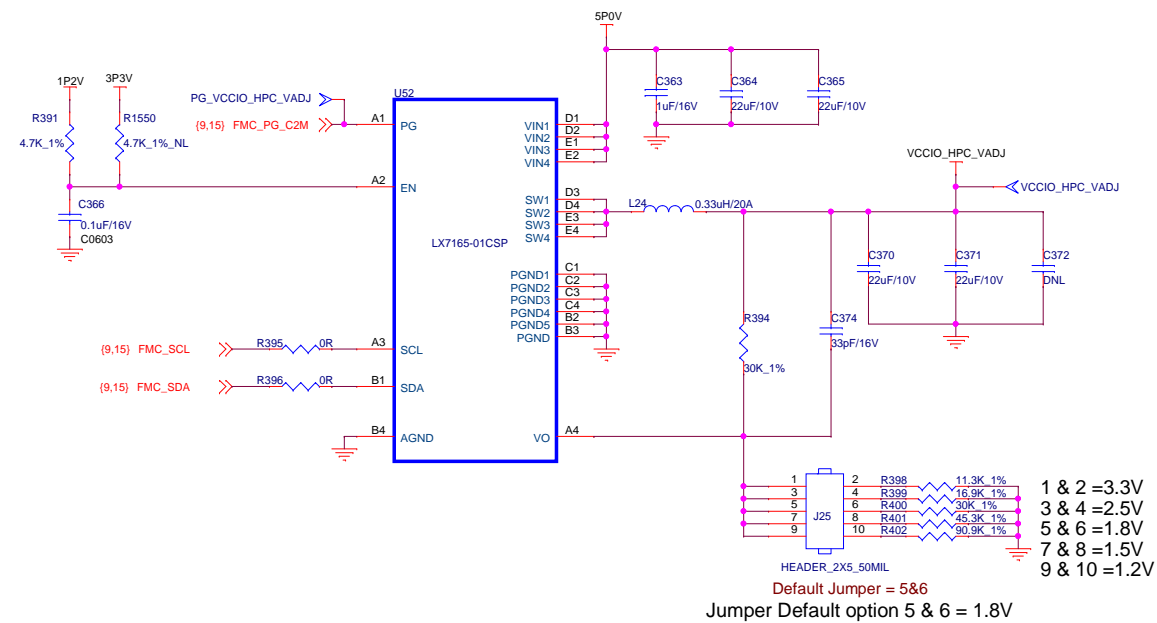
REGULATOR 9 For PF_VDDA: 1.05V@ 5A



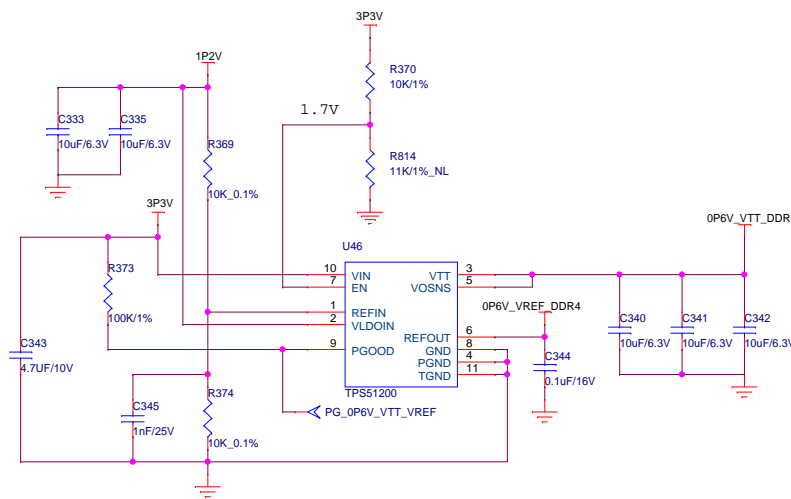
REGULATOR 11 For PF_VDDAUX4: 2.5/3.3V @ 3A



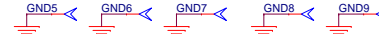
REGULATOR 10 For BANK-4 & HPC FMC: 1.2/1.5/1.8/2.5/3.3V @ 5A



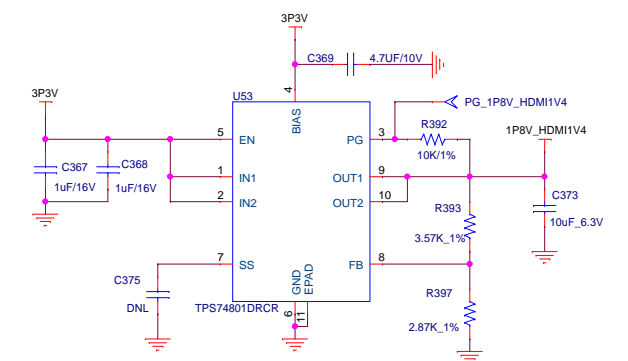
REGULATOR 13 For VTT & VREF of DDR4: 0.6V



TEST POINTS FOR GND



REGULATOR 14 For PF_Bank6, HDMI1.4 TX 1.8 @ 1.5A



TITLE: POLARFIRE_VIDEO_KIT		
Microsemi		
SIZE: Custom	DOCUMENT NO.: DVP-100-000512-001	REV: 1
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