Libero SoC v11.9 SP4

Release Notes

06/2019

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.0

Revision 1.0 is the first publication of this document.

Revision 1.1

6/10/2019: Section 7.1: Refined instructions for Megavault users

Contents

1 Libero SoC v11.9 SP4 Release Notes

Libero® system on chip (SoC) v11.9 SP4 is a service pack release of the Libero SoC v11.9 software for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Note: Enhancements and new features for SmartFusion2, IGLOO2, and RTG4 device families will no longer be added to the Libero SoC v11.9 software branch. Please create new projects in **Libero SoC v12.1** release or later using the **Enhanced Constraints Flow**.

Note: The Classic Constraints Flow is no longer recommended for SmartFusion2, IGLOO2, and RTG4. Consider migrating such designs to a new project using the **Enhanced Constraints Flow**. Refer to the Migration Guide.

2 What's New in Libero SoC v11.9 SP4

Libero SoC v11.9 SP4 includes the following updates.

2.1 RTG4 CN19009: PLL Lock Stability

In some cases, the RTG4 PLL can experience a loss of lock event from which it does not automatically self-recover. In these cases, the assertion of the PLL_ARST_N input is required to regain lock. In Libero SoC v11.9 SP4, the RTG4 CCC configurator **v2.0.101** introduces an option to **Enable PLL Loss of Lock Auto Reset Logic**. This option is enabled by default whenever the PLL is not bypassed, and will insert an additional fabric logic circuit to monitor the PLL lock signal and issue a reset command to the PLL, if loss of lock is detected. This circuit requires a 50 MHz free-running clock that is readily available from the on-chip RC oscillator. You must instantiate the RCOSC_50MHZ macro and distribute its output through a GLx of any one CCC and eventually connect to the exposed CLK50_MHZ input pin of the CCC using the PLL. The CCC connected to RCOSC_50MHZ could even be the same CCC containing the PLL whose reset logic requires the CLK50_MHZ input. If you do not want to use the on-chip RC oscillator, the CLK50_MHZ input pin of the CCC can be driven by an external free-running oscillator running at 50MHz or slower.

Review Customer Notifications 19009 and 18009.7 for more information.

When the PLL is not bypassed, PLL_ARST_N, PLL_POWERDOWN_N, and READY_VDDPLL signals are always exposed to provide additional user access to these signals. The auto-reset circuit for the PLL will still function even if you connect the exposed PLL_ARST_N input to a logic-high because the circuit combines this user input with the status of the voted lock. If the PLL_ARST_N, PLL_POWERDOWN_N, and READY_VDDPLL inputs are unused in your design, these additional exposed ports can be tied to logic-high.

Note: Refer to UG0586: RTG4 FPGA Clocking Resources User Guide for guidelines on selecting the appropriate PLL Lock Window. This is especially important for applications requiring phase alignment between the CCC input reference clock and the CCC outputs.

2.2 RTG4 CN19011.2: I/O Driven High Momentarily at the Start of Programming

Libero SoC v11.9 SP4 eliminates an I/O glitch at the end of programming a blank RTG4 device. See CN19011.2 for details. When a design that has completed Place and Route in a prior release is first opened in Libero SoC v11.9 SP4, there is no design state invalidation. To take advantage of the new behavior, you must use Libero SoC v11.9 SP4 to regenerate the bitstream for programming.

3 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC v11.9 SP4. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

3.1 List of Resolved Issues

Case Number	Description
493642-2164708663, 493642-2220598517, 493642-2357498226	RTG4 uPROM addressing user prog space as warnings/errors/ - using ModelSim simulation
493642-2582937640	RTG4 LSRAM: Libero Log should report in ECC, non-pipelined mode
493642-2544111080	RTG4: IO glitch during programming
493642-2575742710	RTG4 CQFP 352: Pop up of unrecognized package while opening SynplifyPro interactively
493642-2551173245	RTG4 PLL LOCK Delay: not supported in simulation
	RTG4 CCC: Extra ports exposed when PLL is bypassed
	RTG4 FDDR w/INIT - disable verbose sim
	Mismatch between BA netlist and SDF bit order for carry chains
	RTG4 PCIe RTL simulation fails to access config space after link up
	SmartFusion2 SmartDebug: DPK not working when permanent settings are enabled

4 Design Migration

Note the following when migrating a project created Libero SoC v11.9 SP3 (or earlier releases) to Libero SoC v11.9 SP4.

4.1 RTG4 CCC Updates

There have been functional updates to the RTG4 CCC core to address CN19009 (RTG4 PLL Lock Stability).

Existing projects created in prior releases will be invalidated when the project is first opened in Libero SoC v11.9 SP4 if a CCC with PLL is instantiated in the design. Upon opening the project, a pop-up informational window alerts you to the invalidation. The design state reverts to the pre-synthesis state (for Enhanced Constraint Flow) or the pre-compile state (for Classic Constraint Flow). Download the latest RTG4FCCC core version (**v2.0.101** or later) and replace the component by right-clicking it in the Design Hierarchy pane and selecting “Replace Component Version”. Make the new port connections as necessary for any additional ports added to the component and regenerate the design. To continue with the design flow, rerun synthesis (for Enhanced Constraint Flow) or compile (for Classic Constraint Flow). Designs which continue to use an older RTG4FCCC will fail to synthesize (for ECF) or compile (for CCF) until the FCCC instance is migrated to v2.0.101 or later.

Note the following changes:

- The PLL Options Tab, Miscellaneous settings includes a new setting called “Enable PLL Loss of Lock Auto-Reset Logic”. This setting is enabled by default. Before unchecking this option, designers are encouraged to review CN19009 and CN18009.7 for additional details.
- When the PLL is not bypassed, and the PLL Loss of Lock Auto-Reset Logic is enabled, the PLL_ARST_N, PLL_POWERDOWN_N, and READY_VDDPLL signals are always exposed to provide additional user access to these signals. They can be tied to logic high if they are not used in the design.
- A new INFO bubble tooltip will be added on the PLL options tab to direct the user to the RTG4 FPGA Clocking Resources User’s Guide for more information on selecting the minimum PLL Lock Window setting for a given PLL configuration.

5 Known Limitations, Issues and Workarounds

Known issues from Libero SoC v11.9 also apply to Libero SoC v11.9 SP4. Review the Libero SoC v11.9 Release Notes for Known Issues in Libero SoC v11.9.

5.1 Secure IP flow is failing at Compile when Mentor simulation key is removed

Compile fails in the Secure IP flow when the Mentor simulation key is removed. This issue is fixed in the Libero SoC v12.0 release.

5.2 FlashPro will error out, if an existing PDB is modified to disable the fabric

If an existing PDB file is modified to disable the fabric and programmed only with eNVM, FlashPro will error out.

Workaround:

Create a new FlashPro project and create a new PDB. Enable eNVM and import the efc file required for programming eNVM. Save the PDB and use this PDB to program the device.

5.3 SmartTime reports False Failure during max/best or min/worst case analysis

Timing reports may have incorrect slacks for the secondary corners “max/best” and “min/worst” if they were created with the constraint coverage option turned on. The reports for “max/worst” and “min/best” corners are not affected.

Workaround:

1. First, enable the constraint coverage option before running Verify Timing to generate and analyze the coverage report (but disregard the timing reports for “max/best” and “min/worst”). Then, disable the constraint coverage option before re-running Verify Timing to generate and analyze the timing reports at all corners, including “max/best” and “min/worst”.
2. Upgrade to Libero SoC v12.0, or later, where this issue has been fixed.

6 System Requirements

For information about operating system support and minimum system requirements, see the System Requirements web page.

For Linux OS setup instructions, see How to Set Up Linux Environment for Libero User Guide:

6.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating systems
- Windows XP
- Support for the following operating systems has ceased with Libero SoC v12.0 release. For more information, refer to PCN17031.
    - RedHat Enterprise Linux 5.x through 6.5
    - CentOS 5.x through 6.5

7 Libero SoC v11.9 SP4 Download

Click the following links to download Libero SoC v11.9 SP4 on Windows and Linux operating systems:

- Windows Download
- Linux Download

Note: Installation requires administrator privileges to the system.

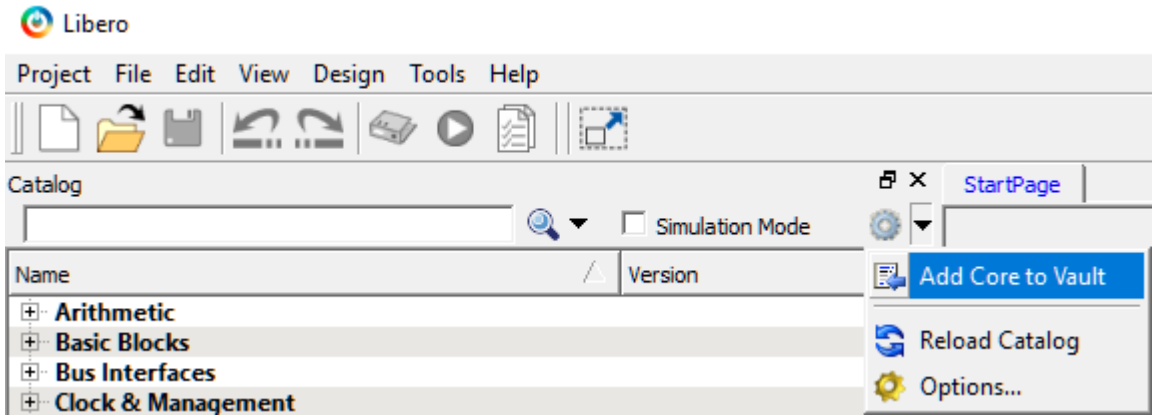
Libero SoC v11.9 SP4 is an incremental service pack and can be installed over Libero SoC v11.9, or over Libero SoC v11.9 SP3.

After successful installation, clicking **Help-> About Libero** will show Version: 11.9.4.4.

7.1 Instructions for Megavault users

Only one core has changed between Libero SoC v11.9 SP3 and vSP4: the RTG4 FCCC core version has been updated to 2.0.101. As a result, if you do not permit Libero to have access to the Internet, you must do the following:

1. Download and install the Megavault for Libero SoC v11.9 if you haven't already done so
    a. Ensure that you have write access to the Megavault
2. Download the Actel_SgCore_RTG4FCCC_2.0.101.cpz file
3. Install and open Libero SoC v11.9 SP4. From Libero:
    a. Set the vault location to that of the Megavault
    b. Switch to the Catalog view by clicking View -> Windows -> Catalog
    c. Click "Add Core to Vault" to import the Actel_SgCore_RTG4FCCC_2.0.101.cpz file



The above steps need only be done once per instance of a Megavault; they do not need to be repeated for other users whose Libero install points to the same instance of the Megavault

7.2 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.9 SP4 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.x

- SoftConsole Download