AC486

Application Note

Thermal Management of RTG4 FPGAs in Space Applications

Released

April 2019

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This document was first published in April 2019.

2 Introduction

Thermal management of components in space applications is important. In space applications, subject to vacuum conditions, heat flow is restricted to conduction and radiation. Microchip's FPGA Division recommends that heat dissipation from RTG4 devices be accomplished by using a cold plate at the back of the system PCB, directly under the RTG4 devices as shown in the following figures.

Figure 1 • Conduction Heat Flow Path in RT4G150-CG1657 in Space Application

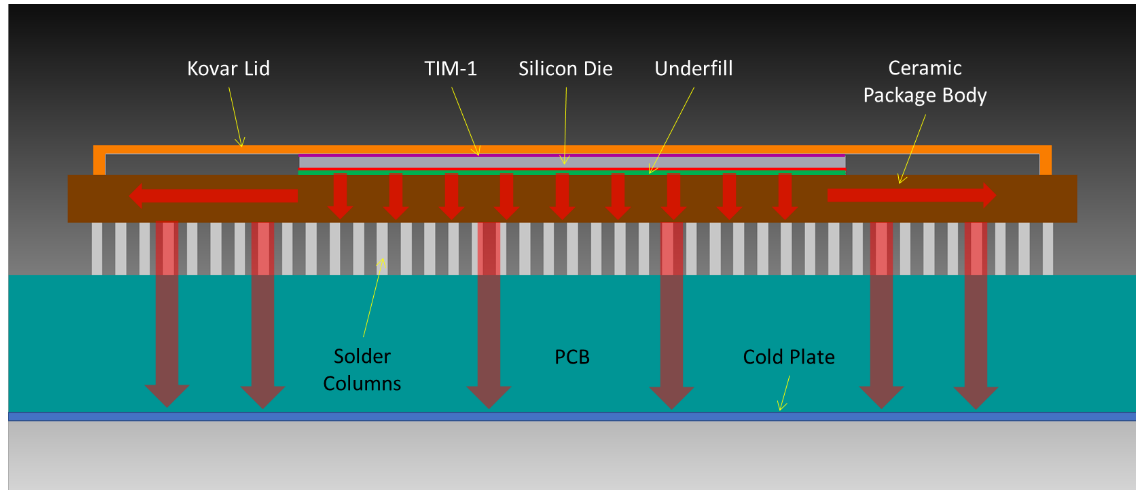
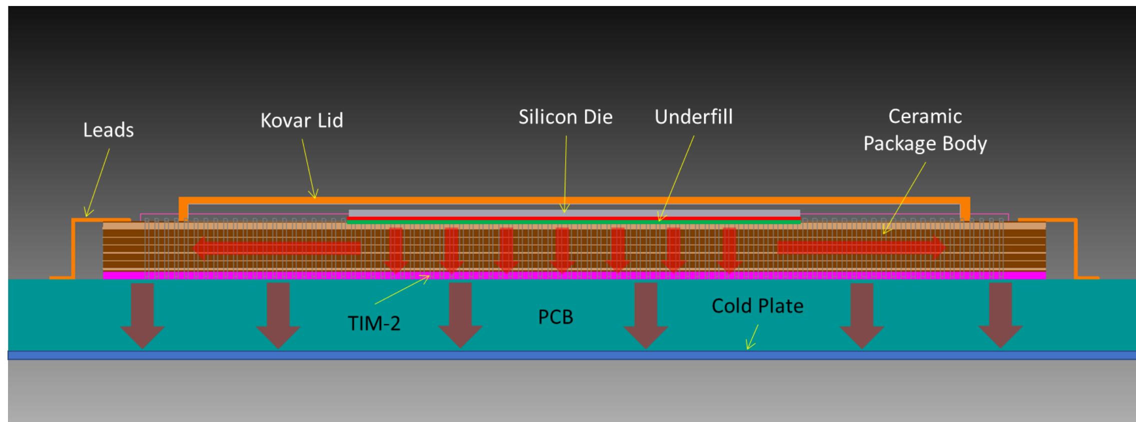


Figure 2 • Conduction Heat Flow Path in RT4G150-CQ352 in Space Application



3 Thermal Resistances of RTG4 Packages

Thermal resistances of RTG4 packages are listed in the table below. However, these thermal resistances are simulated based on JESD51 standards and are intended only for comparing thermal resistances of packages. In real applications, a system-level simulation is needed to predict the actual thermal performance based on the construction of the cabinet, thickness of board, metal layers in system board, and other components near the RTG4 devices that also dissipate heat.

Thermal resistances of RT4G150-CG1657 and RT4G150-CQ352 are as follows.

Table 1 • Thermal Resistances

RT4G150-CG1657	
Junction-to-board, Θ_{jb}	2.50 °C/W
Junction-to-case, Θ_{jc}	0.33 °C/W
RT4G150-CQ352	
Junction-to-bottom of the package, Θ_{jxb}	0.26 °C/W
Junction-to-case, Θ_{jc}	3.12 °C/W

JESD51 defines board size and environment that is different from real system applications.

Junction-to-board (Θ_{jb}) thermal resistance setup: The environmental conditions are specifically designed for testing integrated circuit devices that are mounted on a JESD51 standard test board which has only two internal copper planes. The boundary condition is a ring-style cold plate cooled by a fluid. It clamps the four sides of the test board, with the 80 mm × 80 mm perimeter acting as a boundary condition. The top and bottom insulation fixture comprises low thermal conductivity material. This setup ensures that most of the heat will flow to the board and the cold plate. This is not a true representation of the thermal performance of system level in space. A system-level simulation is needed to predict the actual thermal performance.

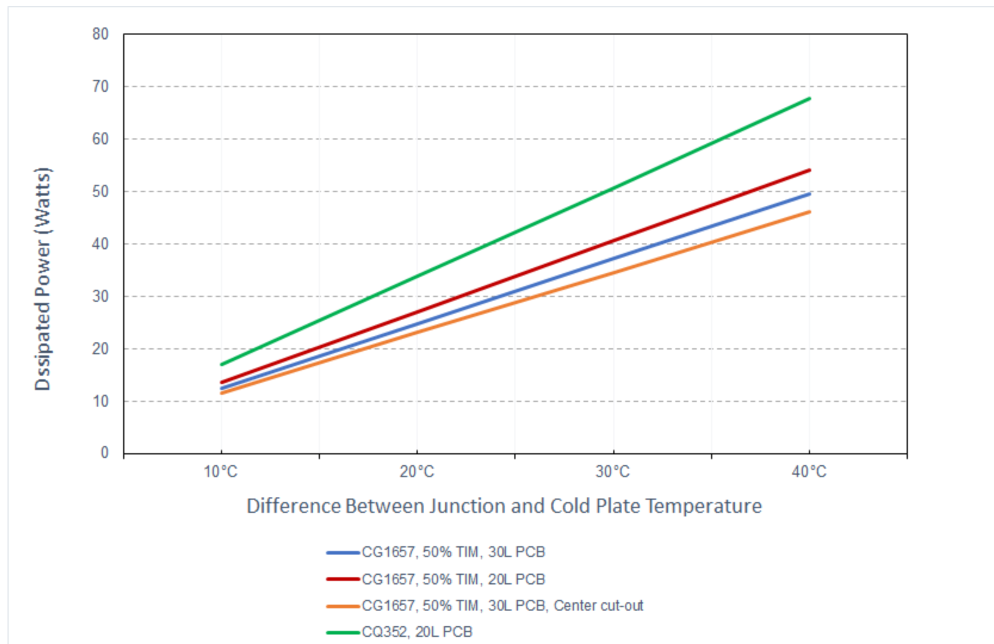
Junction-to-case (Θ_{jc}) thermal resistance setup: A cold plate acting as a boundary condition is attached to the top of the package. The temperature difference between the hotter junction and the cold plate forces the heat to flow from the surface of the die to the top of the package.

Based on the construction of the CG1657 package, it is possible to dissipate heat through the Kovar lid because of the lower junction-to-case thermal resistance (see figure 1 (see page 2) and thermal resistance (see page 3)) . However, the heat sink, which is strapped on top of the Kovar lid, adds mass to the CG1657 package. Shock and vibration experienced by the package during spacecraft launch could put the package's solder column pins under tremendous stress, causing potential damage to column pins and solder joints.

Instead, Microchip recommends attaching a cold plate (full-size or partial with center cut out to accommodate attaching passive components) to the back of the system PCB. This allows the heat generated in the silicon die to flow through the bottom of the package, through the solder columns, and out to the bottom of the PCB as shown in figure 1 (see page 2) and figure 2 (see page 2).

For both CG1657 and CQ352, Microchip simulated a few cases where a cold plate is attached to the back of the PCB. See Appendix (see page 6) regarding the detailed setup. Figure 3 (see page 4) shows the relationship between dissipated power and temperature difference between the device junction and the cold plate attached at the back side of a system PCB.

Figure 3 • Power Dissipation vs. Temperature Delta



Note: The cold plate has a center cutout option to accommodate passive components to the back side of system PCB, directly under the center of CG1657 package.

An approximate power dissipation can be obtained from figure 3 (see page 4). However, to obtain a more accurate power dissipation for each unique space system application, it is highly recommended that customers conduct their own system-level thermal simulation using the material properties described in this application note, along with their specific board material and configuration. Note that power dissipation is highly dependent on board size, layer stack-up, metal fractions of the copper and dielectric on the board, and other components mounted on the PCB near the RTG4 FPGA that also produce heat.

4 Summary

Microchip's recommended cooling method for RTG4 is to attach a cold plate — full size or partial with center cutout) on the bottom of the PCB — directly under the CG1657 or CQ352 packages. This method will minimize potential damage to the RTG4 package as compared to the method of strapping a heat sink on top of the Kovar lid. This will dissipate more than necessary amount of heat for the most challenging space applications using our RTG4 FPGAs in both CG1657 and CQ352 packages.

5 Appendix

Simulation Setup

RT4G150-CG1657, RT4G150-CQ352, and PCB were modeled in a thermal simulation tool. All simulations are set to conduction-only heat transfer. A constant heat source with 95 °C was assigned to the junction of the silicon die. An isothermal temperature cold plate was attached to the back of the PCB, to allow heat to flow from the junction to the cold plate. The material properties that were used for the simulation are listed in the following table.

Table 2 • Materials Used and Their Thermal Conductivity

Material		Thermal Conductivity
Packaged body	Alumina	16.7 W/m*K
Solder columns	Sn20:Pb80 with Cu coil	49.0 W/m*K
Lid/seal ring	Kovar (Fe54:Co17:Ni29)	17.0 W/m*K
Silicon die	Silicon	180.0 W/m*K
Thermal interface - 1		2.0 W/m*K (between the die and package lid of CG1657 only)
PCB plane/traces	FR4/Copper	FRA = 0.35 W/m*K / Cu = 387.0 W/m*K
Cold plate (attached to the back side or the bottom of the PCB, either 30-layer or 20-layer)	Copper	387.0 W/m*K (in this simulation)
Thermal interface - 2		2.0 W/m*K (between the bottom of the CQ352 package body and the PCB)

Note: For the TIM-1 (thermal interface material), contact Microchip. TIM-2 depends on end-user’s choice of thermal interface material. Microchip assumes a TIM-2 with 2.0 W/m*K in the thermal model.

The following are the different simulation cases:

Case 1

RT4G150-CG1657 mounted on top of a 30-layer PCB is 95.5 mm x 81.6 mm x 6.0 mm thick. Cold plate size is 44.5 mm x 44.5 mm directly under CG1657. TIM-1 between the back of the flip chip die is assumed to have a worst case 50% coverage.

Case 2

RT4G150-CG1657 mounted on top of a 20-layer PCB is 95.5 mm x 81.6 mm x 4.0 mm thick. Cold plate size is 44.5 mm x 44.5 mm directly under CG1657. TIM-1 between the back of the flip chip die is assumed to have a worst case 50% coverage.

Case 3

RT4G150-CG1657 mounted on top of a 30-layer PCB is 95.5 mm x 81.6 mm x 6.0 mm thick. Cold plate size is 44.5 mm x 44.5 mm directly under CG1657. The cold plate has a cut-out center area of 20.5 mm x 20.5 mm for mounting decoupling capacitors. TIM-1 between the back of the flip chip die is assumed to have a worst case 50% coverage.

Case 4

RT4G150-CQ352 mounted on top of a 20-layer PCB is 95.5 mm x 81.6 mm x 4.0 mm thick. Cold plate size is 44.5 mm x 44.5 mm directly under CQ352.

Figure 4 • RT4G150-CG1657 Temperature Plot with Full Size Cold Plate (Case 1 and Case 2)

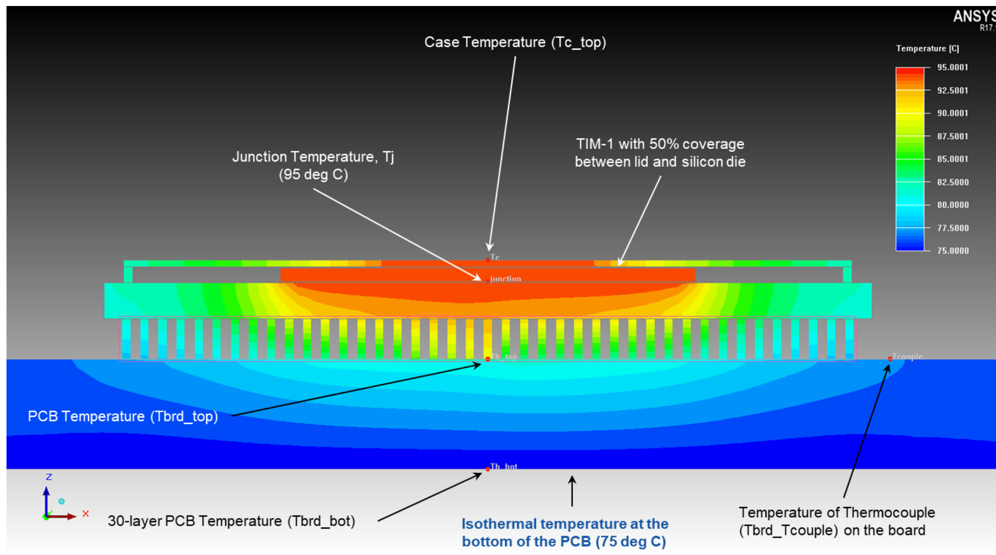


Figure 5 • Cold Plate with Center Cutout Attached Behind PCB, Under the RT4G150-CG1657 (Case 3)

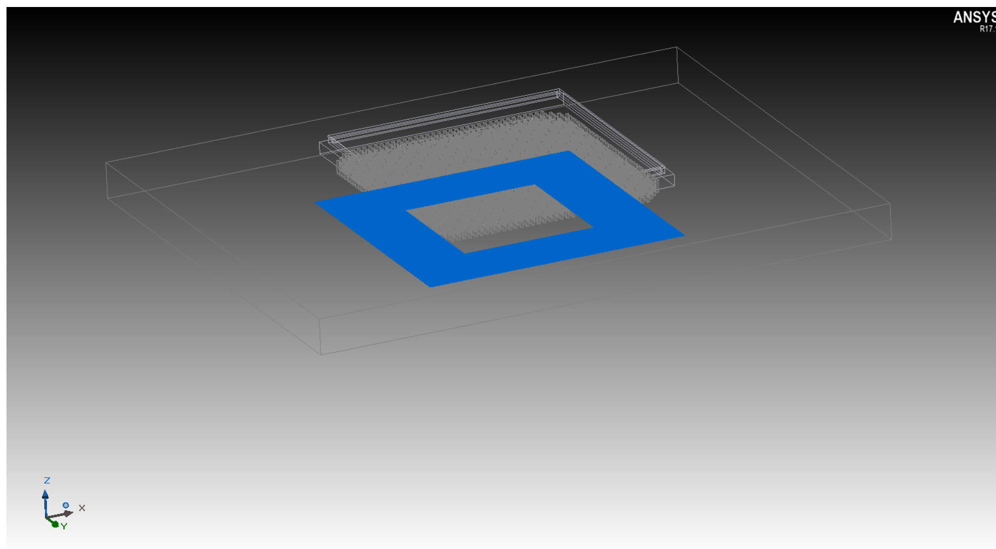


Figure 6 • RT4G150-CG1657 Temperature Plot with Cold Plate Cutout at the Center (Case 3)

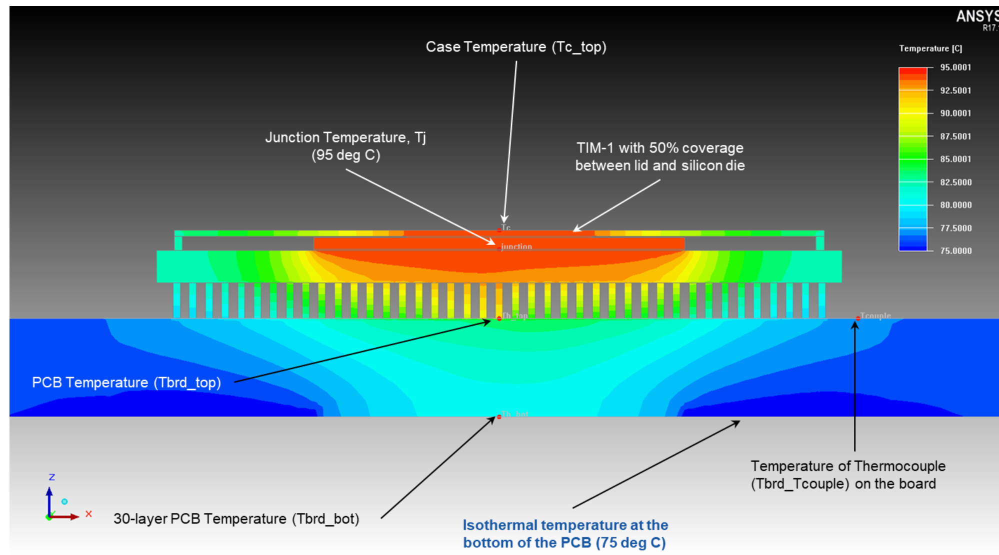


Figure 7 • RT4G150-CQ352 Temperature Plot with Full Size Cold Plate (Case 4)

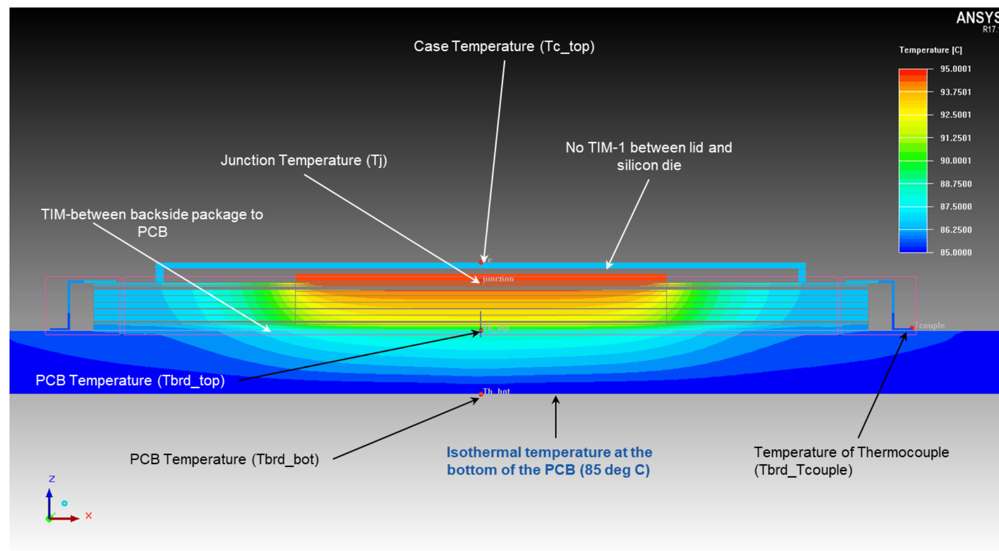


Table 3 • Thermal Model Layers — Thickness and Copper Percentage

Layer Name	Thickness (mm)	Copper Percentage (%)
SOLDERMASK_TOP	0.020	
L01_TOP	0.050	14.4
DIELECTRIC	0.120	
L02_PLANE	0.030	95.3
DIELECTRIC	0.150	
L03_SIG-1	0.030	35.7
DIELECTRIC	0.210	

Layer Name	Thickness (mm)	Copper Percentage (%)
L04_SIG-2	0.030	25.3
DIELECTRIC	0.150	
L05_PLANE	0.030	94.8
DIELECTRIC	0.160	
L06_SIG-3	0.030	7.0
DIELECTRIC	0.200	
L07_SIG-4	0.030	24.8
DIELECTRIC	0.160	
L08_PLANE	0.030	95.0
DIELECTRIC	0.150	
L09_SIG-5	0.030	28.9
DIELECTRIC	0.210	
L10_SIG-6	0.030	22.0
DIELECTRIC	0.150	
L11_PLANE	0.030	95.0
DIELECTRIC	0.160	
L12_SIG-7	0.030	24.2
DIELECTRIC	0.200	
L13_SIG-8	0.030	18.1
DIELECTRIC	0.160	
L14_PLANE	0.030	95.0
DIELECTRIC	0.200	
L15_PLANE	0.030	87.2
DIELECTRIC	0.200	
L16_PLANE	0.030	89.2
DIELECTRIC	0.200	
L17_PLANE	0.030	94.6
DIELECTRIC	0.200	
L18_PLANE	0.030	90.6
DIELECTRIC	0.200	
L19_PLANE	0.030	92.2
DIELECTRIC	0.200	
L20_PLANE	0.030	93.8
DIELECTRIC	0.150	
L21_SIG-9	0.030	18.0
DIELECTRIC	0.210	
L22_SIG-10	0.030	21.0
DIELECTRIC	0.150	
L23_PLANE	0.030	94.7
DIELECTRIC	0.160	
L24_SIG-11	0.030	23.2
DIELECTRIC	0.200	

Layer Name	Thickness (mm)	Copper Percentage (%)
L25_SIG-12	0.030	26.0
DIELECTRIC	0.160	
L26_PLANE	0.030	94.5
DIELECTRIC	0.150	
L27_SIG-13	0.030	8.1
DIELECTRIC	0.210	
L28_SIG-14	0.030	14.2
DIELECTRIC	0.150	
L29_PLANE	0.030	95.1
DIELECTRIC	0.120	
L30_SIG-15	0.058	21.5
SOLDERMASK_BOTTOM	0.020	
Total Thickness	6.028	

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