Microsemi Corporation: CN19009

March 26, 2019

Customer Notification (CN): CN19009

Subject
RTG4 PLL Lock Stability

CN19009 is an early notification of an issue under investigation for the RTG4 FPGA family. There is no action required at this time. An amendment letter will be issued when the investigation is concluded.

Description of Change
RTG4 PLLs can experience loss of lock at high temperature after being initialized, via device power-up or PLL reset, at cold temperature. Once loss of lock happens, the PLL lock can be recovered by issuing a reset to the PLL.

The root cause of the PLL loss of lock has been identified. During RTG4 PLL initialization, a VCO gain setting is automatically chosen to ensure optimal operation. When the PLL is initialized at cold temperature, the automatically chosen VCO gain setting does not provide enough margin for the PLL to operate across the full military temperature range (-55 °C to 125 °C). Rising temperature normally reduces transistor performance, which slows down the VCO to the point where the PLL cannot remain locked. The PLL's VCO performance is similarly affected if the 3.3 V PLL power supply, VDDPLL, decreases after initial PLL reset.

The RTG4 junction temperature at power-up, or after PLL reset, determines the PLL operating temperature window before the loss of lock occurs. Resetting the PLL at higher temperatures selects a higher VCO gain, allowing the PLL to operate to a higher temperature.

Application Impact
1. Temperature ramping direction
   The PLL loss of lock for the identified root cause has only been observed to occur at temperatures higher than the initial PLL reset temperature.
   There is no loss of lock when operating at temperatures lower than the initial PLL reset temperature. (Characterized values for PLL reset temperature and VDDPLL impact will be published in a subsequent datasheet release and CN amendment).
2. Only certain RTG4 PLLs are impacted:

   - Clock Conditioning Circuitry (CCC) PLLs available in the FPGA fabric
   - FDDR PLLs used in the fabric DDR controllers
   - SerDes SPLLs being utilized in PCI Express (PCIe) and XAUI modes to synchronize data to the fabric clock rate

The SerDes PMA PLLs found in each SerDes lane are not impacted. The SerDes PMA PLLs do not use the same VCO gain setting at initialization as the SerDes SPLLs. The SerDes External PCS (EPCS) mode requires that the user implement the serial protocol's PCS logic in the FPGA fabric. The EPCS mode only uses the SerDes PMA PLLs and is not impacted by this issue.

Workaround Under Evaluation
Microsemi is currently evaluating a workaround for this issue, taking into account any variation due to process, voltage, temperature, aging, and radiation effects. A future CN amendment will provide details on the workaround.

Products Affected by this Change
See Appendix A.

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Contact Information

If you have further questions about this subject, contact Microsemi's Technical Support department by using the Support Portal: https://soc.microsemi.com/Portal/Default.aspx.

Regards,

Microsemi Corporation

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Appendix A

Table 1 • Products Affected by This Change

Microsemi Part Number	DLA SMD Number
RT4G150-CB1657PROTO	-
RT4G150-CG1657B	5962-1620801QXF
RT4G150-CG1657E	5962-1620805QXF
RT4G150-CG1657EV	-
RT4G150-CG1657V	5962-1620809VXF
RT4G150-CG1657PROTO	
RT4G150-CQ352B	-
RT4G150-CQ352E	-
RT4G150-CQ352EV	-
RT4G150-CQ352PROTO	-
RT4G150-LG1657B	5962-1620803QZC
RT4G150-LG1657E	5962-1620807QZC
RT4G150-LG1657EV	
RT4G150-LG1657V	5962-1620811VZC
RT4G150-LG1657PROTO	-
RT4G150-1CB1657PROTO	-
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-1CG1657EV	-
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-1CG1657PROTO	-
RT4G150-1CQ352B	-
RT4G150-1CQ352E	-
RT4G150-1CQ352EV	-
RT4G150-1CQ352PROTO	
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-1LG1657EV	-
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-1LG1657PROTO	-

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