LX7712

120V, 5A, LCL/RLCL Programmable Current Limiting Power Switch For Space

Description

The LX7712 is a radiation-hardened-by-design power switch for integration into spacecraft power distribution systems as an electronic fuse for power line protection. DC supplies up to 120V with continuous current rating up to 5A can be easily turned on and off with slew rate programmability. The LX7712 includes a P-channel MOSFET power switch and catch diode for inductive loads.

The LX7712 is configurable as either a latchable current limiter or a fold-back current limiter, with optional thermal shutdown. Multiple LX7712 devices can be paralleled to increase the current rating. The current limit, on/off slew rate, and fault response fault timers are programmed with passive external components.

The latchable current limiter is configurable to either latch off (LCL) under fault conditions, or to attempt to restart in hiccup mode (RLCL). A fault time integrating function accumulates the thermal effects of short fault pulses. The fault timer is configurable for either a fixed duration or a duration that is a function of the voltage drop from line input to load output across the switch. A resistor programmable fault timer discharge function ensures that the LX7712 has dissipated excess energy to a safe level before restarting.

In fold-back current limit (FCL) mode, the profile of the fold-back load current versus load voltage curve is resistor programmable. Fold-back allows automatic fault recovery. An overload condition forces the current limit to a safe trickle level, and when the overload is removed the current limit returns to its normal level. This prevents soft-short fault situations which can cause the switch to over-dissipate.

A programmable current ramp function limits the slew rate of the current during turn on and turn off.

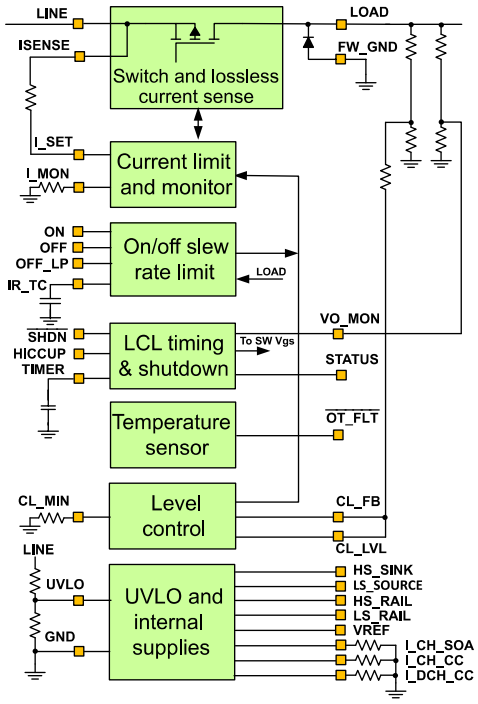
The LX7712MFM is packaged in a 48-pin hermetic hybrid tub flatpack (HTF) package. It operates over a -55°C to 125°C temperature range and is radiation tolerant to a minimum of 100krad(Si) TID and a minimum of 50krad(Si) ELDRS, as well as single event effects.

Features

- Internal 120V, 5A rated power switch
- Internal catch diode for inductive loads
- Constant current or fold-back current limit
- Safe management of soft overload faults
- Optional hiccup automatic restart mode (RLCL)
- Programmable current levels
- Programmable fault timer
- Current monitor output
- Separate ON, OFF, and low power OFF control inputs
- Low power switch voltage drop
- Over temperature shutdown and optional restart
- Load current slew rate control
- Small hermetic 48 lead HTF package
- Radiation tolerant: 100krad(Si) TID, 50krad(Si) ELDRS, SEL immune up to 60 MeV.cm²/mg and 125°C (fluence of 10^7 particles/cm²)

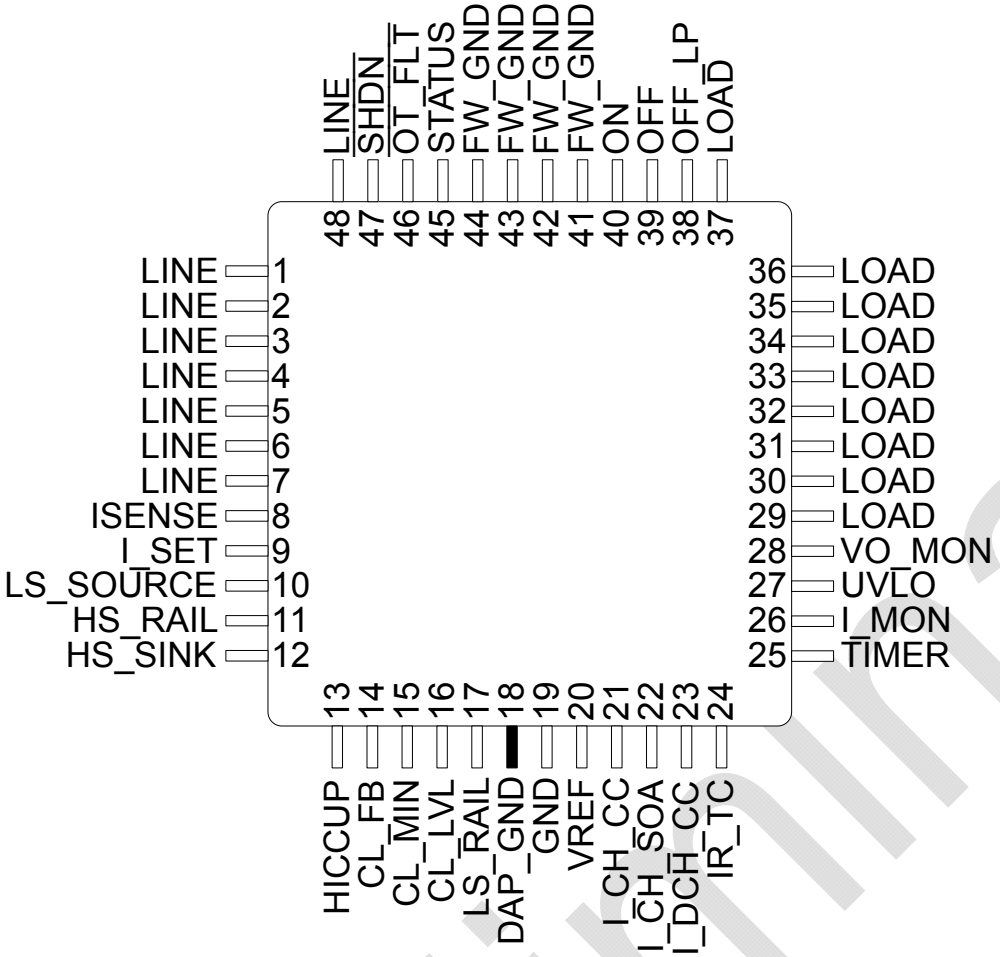
Applications

- Spacecraft power control and distribution



Typical Power Switch System

1 HTF-48 Pin Configuration and Pinout



Notes

1. Pin 18 is directly connected to the metal package body and wire bonded to the die (see Figure 20 on page 26). Pin 18, the GND pin 19, and the four FW_GND pins 41, 42, 43, and 44 must be connected to the same ground potential
2. The metal package top is electrically conductive to the metal package body, and so is at ground potential (GND)
3. The top or the base of the package can be used as the heat conducting surface. It is recommended to use the base of the package as the surface for conducting heat from the package. The metal package top is attached to the package body at the top of relatively thin cavity walls, and so has a much higher thermal resistance from the die than the base of the package. The leads can be formed to mount the part upside down if necessary. It is recommended to apply a thermal interface material between the package and its heat dissipater. The heat dissipater can be copper layers within a multilayer circuit board to spread heat laterally across the board, or a direct mounted dissipation element

2 Ordering Information

Operating Temperature	Package Type	Package	Part Number	SMD Number	Flow	Shipping Type
-55°C to 125°C	Hermetic Metal	HTF-48	LX7712MFM-EV	TBD	MIL-PRF-38535 Class V	Tray
			LX7712MFM-EQ	TBD	MIL-PRF-38535 Class Q	
			LX7712-ES[1]	-	Engineering Samples[1]	

[1] Engineering samples are intended for design evaluation purposes only. They are only tested and trimmed at room temperature, and do not undergo any thermal, environmental, or hermeticity testing

3 Pin Numbering and Pin Descriptions

Pin	Name	Pin Type	Pin Function	Description
1-7	LINE	Power	Power Switch Input	All LINE pins 1 to 7 and 48 must be used, connected to the power supply to be switched. LINE is also the power input for the HS_RAIL regulator. Bypass the group of LINE pins with a single 100nF capacitor to GND
8	ISENSE	Power Kelvin Sense Input	Current Monitor Input	Connect a resistor R_{I_SET} = 10kΩ between ISENSE and I_SET to configure the power switch's current limit. ISENSE is internally bonded to LINE and provides a Kelvin connection to LINE since it does not carry any of the LINE/LOAD current. The voltage across R_{I_SET} is 1V per amp of load current, so 5V maximum at 5A load current
9	I_SET	Analog Input	Current Monitor Reference	
10	LS_SOURCE	Power	Low-Side Rail Power Source	Input to the LS_RAIL linear regulator. Connect directly to a voltage between 12V and 30V, or to a higher voltage via a series ballast resistor and/or pre-regulator. Bypass LS_SOURCE with a 100nF capacitor to GND. See the LS_SOURCE and LS_RAIL section 12.3 on page 13
11	HS_RAIL	Power	High-Side Rail	Output of an internal linear regulator delivering 10V ±1V below LINE. Regulator input is HS_SINK pin 11. Bypass HS_RAIL with a 100nF capacitor to LINE. See the HS_SINK and HS_RAIL section 12.2 on page 12
12	HS_SINK	Power	High-Side Rail Power Source	Input to the HS_RAIL linear regulator. Connect to a voltage at least 12V below VLINE, typically GND. See the HS_SINK and HS_RAIL section 12.2 on page 12
13	HICCUP	Logic Input (4MΩ to GND)	Hiccup Mode Enable	To enable hiccup mode, which resets a latched over-current fault under fault timer control, tie HICCUP to either VREF or to a 2.5V to 5V logic supply. To disable hiccup mode, either leave HICCUP open or tie HICCUP to GND. See the Fault Timer section 16 on page 21
14	CL_FB	Analog Output	Current Limit Fold Back	This pin is used to generate a negative current limit offset when fold back current limiting is used. This pin should be shorted to CL_LVL if the function is desired, otherwise, the pin can be left open. This pin is an open collector current sink with a value of ½ of the discharge current
15	CL_MIN	Analog Input	Current Limit Minimum Level	The voltage on this pin sets the minimum level of current limit. This pin features a source current equal to ½ of the discharge current. In current-foldback mode, a resistor shall be used to connect this pin to ground and generate the desired voltage level to clip CL_LVL. In other modes, the voltage on this pin should be smaller than the level on CL_LVL to not interfere with the desired function (e.g. short to GND)
16	CL_LVL	Analog Input	Current Limit Level	The voltage on this pin sets the current limit reference level. A specific resistor network shall be connecting this pin to LOAD and/or VREF, depending on the desired current limit mode
17	LS_RAIL	Power	Low-Side Rail	Output of an internal linear regulator delivering 10V ±1V above GND. Regulator input is LS_SOURCE pin 10. Bypass LS_RAIL with a 100nF capacitor to GND. See the LS_SOURCE and LS_RAIL section 12.3 on page 13
18	DAP	Power	Die Attach Pad	This pin must be connected to GND
19	GND	Power	GND	This pin is the GND point for analog and logic signals
20	VREF	Analog Output	5V Reference	Output of an internal +5V ±4% reference voltage. VREF can source up to 2mA into external loads such as configuration resistor networks. Bypass VREF with a 100nF capacitor to GND
21	I_CH_CC	Analog Input	Fault Timer Static Charge Current Programming	Connect resistor $R_{I\_CH\_CC}$ from I_CH_CC to GND to set a static reference current to charge the fault timer capacitor. Leave open if not used. See the Fault Timer section 16 on page 21
22	I_CH_SOA	Analog Input	Fault Timer Dynamic Charge Current Programming	Connect resistor $R_{I\_SOA\_CC}$ from I_CH_SOA to GND to set a dynamic reference current to charge the fault timer capacitor. Leave open if not used. See the Fault Timer section 16 on page 21
23	I_DCH_CC	Analog Input	Fault Timer Discharge Current Programming	Connect resistor $R_{I\_DCH\_CC}$ from I_DCH_CC to GND to set a static reference current to discharge the fault timer capacitor, and to set the slew rate during power switch turn on and turn off. See the Fault Timer section 16 on page 21

Pin	Name	Pin Type	Pin Function	Description
24	IR_TC	Analog Input	Current Ramping Timing Capacitor	Connect capacitor C_{IR_TC} from IR_TC to GND to set the slew rate during power switch turn on and turn off or leave open. $R_{I\_DCH\_CC}$ on I_DCH_CC pin 23 is the other programming element. See the On and Off Controls section 13 on page 15
25	TIMER	Analog Input	Latchable Current Limit Fault Timer	Connect capacitor C_{TIMER} from TIMER to GND to set the programmable fault timer time constant together with resistors $R_{I\_CH\_CC}$, $R_{I\_DCH\_CC}$, and $R_{I\_DCH\_CC}$. Grounding TIMER disables the fault timer function. See the Fault Timer section 16 on page 21
26	I_MON	Analog Output	Load Current Monitor	Connect resistor R_{I_MON} from I_MON to GND to monitor the load current. The output current on this pin is 1/5000 x the load current
27	UVLO	Analog Input	LINE Under-Voltage Lock-Out	This input is used to monitor the LINE voltage. The under-voltage level is set with a LINE to GND external voltage divider. See the External Voltage Monitor Inputs section 13.2 on page 16
28	VO_MON	Analog Input	LOAD Voltage Monitor	This input is used to monitor the LOAD voltage. The under-voltage level is set with a LOAD to GND external voltage divider. See the External Voltage Monitor Inputs section 13.2 on page 16
29-37	LOAD	Power	Power Switch Output	All LOAD pins 29 to 37 must be used, connected to the external load. An internal reverse biased diode from LOAD to GND clamps inductive flyback voltages on turn-off
38	OFF_LP	Power (2.4MΩ to GND)	OFF (Low Power) Control	A logic high level on OFF_LP will turn off the power switch and enter low power mode by shutting down internal power supplies
39	OFF	Logic Input (4MΩ to GND)	OFF Control	A logic high pulse or level on this pin will turn off the power switch. The OFF input has priority over the ON pin if both are high
40	ON	Logic Input (4MΩ to GND)	ON Control	A logic high pulse or level on this pin will turn on the power switch
41-44	FW_GND	Power GND	Free-wheel Diode Ground	This pin provides a path for current to flow through the free-wheeling diode that provides a path of inductive load current if the power switch shuts off abruptly
45	STATUS	Open Collector Logic Output	On/Off Status	A low level on this open collector output indicates that the switch is on, and that the VO_MON is monitoring a LOAD voltage greater than the under-voltage threshold
46	$\overline{\text{OT\_FLT}}$	Open Collector Logic I/O	Over Temperature Fault	A low level on this open collector output indicates that an over-temperature fault has occurred. The over-temperature sensor has hysteresis and resets after cooling down. This pin can be connected to $\overline{\text{SHDN}}$. Multiple devices can have $\overline{\text{OT\_FLT}}$ and $\overline{\text{SHDN}}$ connected
47	$\overline{\text{SHDN}}$	Open Collector Logic I/O (1MΩ to LS_RAIL)	Shutdown Fault	A low logic output signal indicates that an LCL timeout has triggered the shutdown latch. This pin can also be used as an input from another device or from the temperature monitor output $\overline{\text{OT\_FLT}}$ to conditionally shutdown the switch. Multiple devices can have $\overline{\text{SHDN}}$ connected
48	LINE	Power	Power Switch Input	All LINE pins 1 to 7 and 48 must be used, connected to the power supply to be switched. LINE is also the power input for the HS_RAIL regulator. Bypass the group of LINE pins with a single 100nF capacitor to GND

4 Absolute Maximum Ratings

Stresses above those listed in ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
LINE input (V_{LINE}) to GND	-3	150	V
V_{LOAD}	-2	V_{LINE} + 1.5	V
V_{HS_SINK}	-0.3	V_{LINE}	V
V_{LS_SOURCE}, when directly connected to a supply	-0.3	32	V
V_{LS_SOURCE}, when connected to a supply via a series current limiting resistor	-0.3	V_{LINE}	V
P_{HS_SINK} HS_SINK regulator dissipation		240	mW
LS_SOURCE regulator dissipation, $V_{LS\_SOURCE} < V_{LS\_CLAMP}$ (P_{LS_SOURCE})		300	mW
LS_SOURCE regulator + clamp dissipation, $V_{LS\_SOURCE} \geq V_{LS\_CLAMP}$ (P_{LS_SOURCE})		600	mW
I_{LINE}, I_{LOAD}	-7.5	7.5	A
I_{FW_GND}		7.5	A
V_{HS_RAIL}	Self-regulated	V_{LINE}	V
V_{I_SET}	V_{LINE} - 7.5	V_{LINE}	V
V_{LS_RAIL}	-0.3	12	V
V_{VREF}	-0.3	Self-regulated	V
V_{IMON}	-0.3	5.6	V
V_{CL_LVL}, V_{CL_MIN}, V_{TIMER}	-0.3	9	V
V_{UVLO}, V_{VO_MON}	-0.3	15	V
V_{CL_FB}, $V_{I\_CH\_CC}$, $V_{I\_CH\_SOA}$, $V_{I\_DCH\_CC}$, V_{IR_TC}	-0.3	11	V
V_{HICCUP}, V_{OFF_LP}, V_{OFF}, V_{ON}, V_{STATUS}, $V_{\overline{OT\_FLT}}$, $V_{\overline{SHDN}}$	-0.3	12	V
STATUS, $\overline{SHDN}$. and $\overline{OT\_FLT}$ sink current		3	mA
I_MON pin current	-1	0	mA

5 Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Parameter	Min	Max	Units
V_{LINE}, V_{LOAD}	12	120	V
P_{HS_SINK} HS_SINK regulator dissipation		180	mW
P_{LS_SOURCE} LS_SOURCE regulator dissipation, $V_{LS\_SOURCE} < V_{LS\_CLAMP}$		225	mW
P_{LS_SOURCE} LS_SOURCE regulator + clamp dissipation, $V_{LS\_SOURCE} \geq V_{LS\_CLAMP}$		450	mW
V_{LS_SOURCE} operating mode, V_{LS_SOURCE} directly connected to a supply (OFF_LP = logic low)	12	30	V
V_{LS_SOURCE} operating mode, V_{LS_SOURCE} connected via a series resistor (OFF_LP = logic low)	12	V_{LINE}	V
V_{LS_SOURCE} low power mode (OFF_LP = logic high)	12	V_{LINE}	V
V_{LS_RAIL}	9	11	V
V_{HS_SINK}	0	V_{LINE} - 12	V
V_{I_SET}	V_{LINE} - 6	V_{LINE}	V
V_{CL_LVL}	0	5.3	V
V_{UVLO}, V_{VO_MON}	0	13	V
V_{CL_FB}, V_{CL_MIN}, $V_{I\_CH\_CC}$, $V_{I\_CH\_SOA}$, $V_{I\_DCH\_CC}$, V_{IR_TC}, V_{TIMER}, V_{HICCUP}, V_{OFF_LP}, V_{OFF}, V_{ON}, V_{STATUS}, $V_{\overline{OT\_FLT}}$, $V_{\overline{SHDN}}$	0	6	V
V_{IMON}	0	(V_{I_SET} - 5) up to 5.5 max	V
STATUS, $\overline{SHDN}$, and $\overline{OT\_FLT}$ sink current	0	2	mA
I_{LINE}, $-I_{LOAD}$ (negative current when switch body diode or catch diode is forward biased)	-5	5	A

6 Electrostatic Discharge Ratings

JEDEC JEP155 states that 500V HBM allows safe manufacturing with a standard ESD controlled process.
JEDEC JEP157 states that 250V CDM allows safe manufacturing with a standard ESD controlled process.
ESD ratings apply to all pins.

ESD Test	Minimum Capability
HBM: Human Body Model, per MIL-STD-883 TM3015	±2kV
CDM: Charged Device Model, per ANSI/ESDA/JEDEC JS-002	±TBDV

7 Electrical Characteristics

The following specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: V_{ON} = V_{HICCUP} = 6V; V_{OFF} = V_{FB_LVL}= GND; V_{HS_SINK} = GND; V_{LS_SOURCE} = 17V; 22V < V_{LINE} < 120V. Typical parameters refer to T_J = 25°C. Positive currents flow into a pin

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Operating						
I_{GND}	Internal IC current consumption flowing to ground via the GND pin	Switch On or Off		-3.5	-8.0	mA
		Switch Off (low power); LS_SOURCE powered internally		-0.6	-2	mA
I_{HS_SINK}	Current for internal linear regulator HS_RAIL	OFF_LP = logic low		-1	-1.5	mA
I_{LS_SOURCE}	Current for internal linear regulator LS_RAIL (part of I_{GND})	LS_SOURCE is supply for LS_RAIL regulator. OFF_LP = logic low	3.5	6.5	10	mA
I_{LS_RAIL}	Current into LS_RAIL	LS_RAIL supplied with external 11V, LS_SOURCE floating	TBD	7	TBD	mA
V_{LS_CLAMP}	Clamp voltage for LS_SOURCE input	Externally driven at 10mA	32	34	36	V
V_{LINE_UVLO}	LINE UVLO	LINE voltage rising, with both LS_RAIL and VREF operating normally	9		10	V
V_{LINE_HYST}	LINE UVLO hysteresis			0.7		V
$V_{LS\_RAIL\_UVLO}$	LS_RAIL UVLO	LS_RAIL voltage rising		7.9		V
$V_{HS\_RAIL\_UVLO}$	HS_RAIL UVLO	(V_{LINE} - V_{HS_RAIL}) voltage rising		7.9		V
V_{VREF_UVLO}	VREF UVLO	LS_RAIL voltage rising		4.25		V
V_{HS_RAIL}	Voltage below line	V_{LINE} - V_{HS_RAIL}	9	10	11	V
V_{LS_RAIL}	Voltage above ground	-5mA < I_{LS_RAIL} < 0 drawn externally	9	10	11	V
I_{VREF}	Current limit	VREF shorted to ground	-2	-12		mA
V_{VREF}	Output voltage	-2mA < I_{VREF} < 0, T_J = 25°C	4.8	5.0	5.2	V
ΔV_{VREF}	Output voltage variation	Across temperature range, I_{VREF} = 100µA, guaranteed by design	-50		+50	mV
ON, OFF, HICCUP, OFF_LP						
V_{INPUT}	Input logic high level		2.0			V
	Input logic low level				0.8	V
	Leakage Current	0V < V_{INPUT} < 5V	0		10	µA
T_{LATCH}	Pulse Width to latch for ON, OFF and HICCUP	Either ON or OFF	1			µs
I_CH_CC, I_CH_SOA, I_DCH_CC						
$V_{I\_CH\_CC}$	Current program voltage	$R_{I\_CH\_CC}$ = 10kΩ to 100kΩ	19.6	20	20.4	%VREF
$V_{I\_DCH\_CC}$	Current program voltage	$R_{I\_DCH\_CC}$ = 10kΩ to 100kΩ	19.6	20	20.4	%VREF
$V_{I\_CH\_SOA}$	Current program voltage	V_{LINE} - V_{LOAD} = 10V, $R_{I\_CH\_SOA}$ = 10kΩ to 100kΩ	0.48	0.5	0.52	V
		V_{LINE} - V_{LOAD} = 100V, $R_{I\_CH\_SOA}$ = 10kΩ to 100kΩ	4.8	5.0	5.2	V

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
CL_MIN and CL_FB under current limiting conditions						
I_{CL_FB}	CL_FB sink current	$R_{I\_DCH\_CC}$ = 50kΩ, 0.5V < V_{CL_FB} < 5V	9	10	11	µA
V_{satCL_FB}	CL_FB saturation voltage	$R_{I\_DCH\_CC}$ = 50kΩ, I_{CL_FB} = 5µA			TBD	mV
ΔI_{LOAD_TRIP} /ΔV_{CL_MIN}	CL_MIN input voltage to LOAD current gain (transconductance)	R_{I_SET} = 10kΩ, R_{DIS} = 50kΩ, for CL_LVL = 0V, CL_FB floating, CL_MIN = 0.2V to 2V	TBD		TBD	Ω^{-1}
$V_{CL\_MIN\ offset}$	CL_MIN input voltage to LOAD current extrapolated offset	R_{I_SET} = 10kΩ, R_{DIS} = 50kΩ, for CL_LVL = 0V, CL_FB floating, CL_MIN = 0.2V to 2V	-TBD		TBD	mV
I_{CL_MIN}	CL_MIN pin current	R_{DIS} = 50kΩ, 0V < V_{CL_MIN} < 4V	-11	-10.5	-9.5	µA
Switch Characteristics						
ΔI_{LOAD_TRIP} /ΔV_{CL_LVL}	CL_LVL input voltage to LOAD current gain (transconductance)	R_{I_SET} = 10kΩ, for CL_LVL = 1V to 5V	TBD		TBD	Ω^{-1}
$I_{LOAD\_TRIP\_2V}$	Load current trip value at 2V	R_{I_SET} = 10kΩ, for CL_LVL = 2V	TBD		TBD	A
$I_{LOAD\_TRIP\_offset}$	Load current trip value extrapolated at 0V	R_{I_SET} = 10kΩ, CL_LVL = 1V, CL_LVL = 2V	TBD		TBD	A
ΔI_{LOAD_TRIP} / 4A	Error from ideal line with respect to 4A scale	R_{I_SET} = 10kΩ, for CL_LVL = 1V to 5V	-10	±5	10	%
I_{LOAD} / I_{I_SET}	I_{I_SET} to I_{LOAD} current gain	Test at I_{LOAD} = 1A and V_{LINE} - V_{LOAD} = 5V		10000		A/A
$I_{I\_MON\_0A}$	I_{I_MON} current at I_{LOAD} = 0A	Test at I_{LOAD} = 0A, CL_LVL = 5.25V, R_{I_MON} = 5kΩ, R_{I_SET} = 10kΩ	0		TBD	µA
$I_{I\_MON\_1A}$	I_{I_MON} current at I_{LOAD} = 1A	Test at I_{LOAD} = 1A, CL_LVL = 5.25V R_{I_MON} = 5kΩ, R_{I_SET} = 10kΩ	TBD		TBD	µA
$I_{I\_MON\_2A}$	I_{I_MON} current at I_{LOAD} = 2A	Test at I_{LOAD} = 1A, CL_LVL = 5.25V, R_{I_MON} = 5KΩ, R_{I_SET} = 10kΩ	TBD		TBD	µA
$I_{I\_MON\_4A}$	I_{I_MON} current at I_{LOAD} = 4A	Test at I_{LOAD} = 4A, CL_LVL = 5.25V R_{I_MON} = 5kΩ, R_{I_SET} = 10kΩ	TBD		TBD	µA
ΔI_{I_MON} / $I_{I\_MON\_4A}$	Error from ideal line with respect to 4A scale for I_{I_MON}	R_{I_SET} = 10kΩ, for CL_LVL = 5.2V, I_{LOAD} = 1A to 4A	4	±1	4	%
$\Delta I_{LOAD\_CLIM\_TRIP}$	Maximum error of load current limit from load trip current (I_{LOAD_CLIM} - I_{LOAD_TRIP})	R_{I_SET} = 10kΩ, for CL_LVL = 1V to 5V, CL condition V_{LINE} - V_{LOAD} = 5V	-0.1	0.0	1.0	A
$V_{LINE-LOAD}$	Switch Voltage drop	Test at I_{LOAD} = 1A		100	200	mV
$I_{LINE-LOAD}$	Switch off leakage	In short circuit			55	µA
t_{PWR_ON}	Switch turn on time	From ON to LOAD; IR_TC = open			150	µs
t_{LP_ON}	Switch turn on time from low power mode	From OFF_LP de-assertion (50%) to LOAD (10%); ON = asserted; IR_TC = open; 100nF capacitor from LS_SOURCE to GND			1.5	ms
t_{C_LIM}	Current limit reaction time	5A current limit, LOAD step from 10kΩ to 1mΩ, I_{LOAD} falls below 5A			100	µs
$V_{Reverse}$	On voltage for switch back diode	$I_{reverse}$ = 5A		1	1.5	V
$I_{Reverse\_sw}$	Maximum reverse current	DC			5	A
Catch Diode Characteristics						
V_{FWD}	Forward voltage from FW_GND to LOAD	I_{FW_GND} = 2A pulsed		1	TBD	V
$I_{FWDcatchD}$	Forward maximum current	DC			0.5	A
P_{FWD}	Average power during pulsed regime	Example 5A x 10ms			0.5	W
Q_{FWD}	Maximum pulse charge	Example 5A x 10ms			50	mC
I_{FW_GND}	Leakage current	V_{LOAD} = 100V		25	50	µA

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Units
Fault Timer						
I_{TIMER}	Fault timer charge current, Under fault condition	$R_{I\_CH\_CC}$ = 100kΩ, $R_{I\_CH\_SOA}$ = open, V_{TIMER} = 2.5V	-12.0	-10.0	-8.0	µA
	Fault timer charge current, Under fault condition	$R_{I\_CH\_CC}$ = open; $R_{I\_CH\_SOA}$ = 100k, V_{LINE} - V_{LOAD} = 20V, V_{TIMER} = 2.5V	-12.0	-10.0	-8.0	
I_{TIMER}	Fault timer discharge current	$R_{I\_DCH\_CC}$ = 10kΩ, V_{TIMER} = 2.5V, non-fault condition	8	10	12	µA
T_{RT_SHDN}	$\overline{SHDN}$ reaction time	Trip detected at $\overline{SHDN}$ to LOAD disconnect, IR_TC = open, 50% to 90%		35	50	µs
V_{TIMER}	Fault timer threshold voltage	Rising; detecting a fault	98	100	102	%VREF
		Falling; detecting end of rest state	19	20	21	
V_{TIMER}	Fault timer discharge voltage	At full discharge state			100	mV
T_{TIMER_PD}	Fault timer trip to $\overline{SHDN}$	Rising or falling fault timer. TIMER driven with external 0V to 5V square wave			5	µs
IR_TC						
V_{I_SET}	IR_TC accuracy	0.2V < V_{IR_TC} < VREF, V_{LINE} - (V_{I_SET} + V_{IR_TC})	-100	0	100	mV
I_{IR_TC}	IR_TC current sink	0.2V < V_{I_RC} < VREF, $R_{I\_DCH\_CC}$ = 10kΩ	96	100	104	µA
I_{IR_TC}	IR_TC current source	0V < V_{I_RC} < VREF, $R_{I\_DCH\_CC}$ = 10kΩ	-104	-100	-96	µA
V_{IR_TC}	VIR_TC Off Voltage	$R_{I\_DCH\_CC}$ = 10kΩ		20	100	mV
Logic Input $\overline{SHDN}$						
$V_{\overline{SHDN}}$	Input logic high level	$\overline{SHDN}$ as input	2.0			V
	Input logic low level				0.8	
	Leakage Current	$\overline{SHDN}$ as input; 0V < $V_{\overline{SHDN}}$ < V_{LS_RAIL}	-50		50	µA
Logic Outputs STATUS, $\overline{OT\_FLT}$, $\overline{SHDN}$						
V_{STATUS}, $V_{\overline{OT\_FLT}}$, $V_{\overline{SHDN}}$	Logic levels $\overline{SHDN}$ as output	High output voltage; 10kΩ pull-up to LS_RAIL	V_{LS_RAIL}-0.5V		V_{LS_RAIL}	V
		Low output voltage; I_{SINK} = 1mA	0		0.5	V
		I_{SINK} internal current limit	2		10	mA
External Under-Voltage Lockout (UVLO)						
V_{UVLO}	Voltage threshold	Voltage rising	49	50	51	%VREF
V_{UVLO}	Hysteresis		1	3	4	%VREF
I_{UVLO}	UVLO monitor leakage	0V < V_{UVLO} < V_{LS_RAIL}	-10		10	µA
$T_{D\ UVLO}$	UVLO to STATUS delay time	UVLO 5V to 0V step, R_{STATUS} = 10kΩ, C_{STATUS} = 100pF, 50% to 50%	0.5		1.5	ms
VO_MON						
V_{VO_MON}	VO_MON threshold	Voltage rising	49	50	51	%VREF
V_{VO_MON}	VO_MON hysteresis	Hysteresis	1	3	4	%VREF
I_{VO_MON}	VO_MON leakage	0 < V_{VO_MON} < V_{LS_RAIL}	-10		10	µA
$T_{D\ VO\_MON}$	VO_MON to STATUS delay time	VO_MON 5V to 0V step, R_{STATUS} = 10kΩ, C_{STATUS} = 100pF, 50% to 50%		TBD		µs
Over Temperature Detect						
$TEMP_{OT}$	Over temperature threshold	Shutdown (die temperature rising)	150		175	°C
	Over temperature hysteresis	Reset (die temperature falling)	25	50	60	°C
t_{TEMP}	Reaction time	Delay from die temp threshold event to OT fault detection		1	2	ms

8 Thermal Properties

Thermal resistance, θ_{JB}, is provided from die to the back surface of the package. Junction temperature T_J is calculated using $T_J = T_B + (PD \times \theta_{JB})$, where T_B is the temperature maintained on the back surface of the package.

Package	Thermal Resistance	Typ	Units
HTF-48	θ_{JB}	1.2	°C/W

9 Heatsink Recommendations

The LX7712 dissipates up to 1W (200mV x 5A) at full normal load, and so thermal considerations are usually necessary even in applications where additional energy absorption under fault conditions is small. The base of the metal package should be used as the heat conducting surface for all but light duty applications. The metal package top is attached to the package body at the top of relatively thin cavity walls, and so has a much higher thermal resistance from the die than the base of the package. It is recommended to apply a thermal interface material between the base of the package and the heat dissipater. The heat dissipater can be copper layers within a multilayer circuit board to spread heat laterally across the board, or a direct mounted dissipation element.

10 Safe Operating Area

The safe operating area curve in Figure 1 shows the maximum operating time allowed versus voltage drop between LINE input and LOAD output for a given current limit setting with a 25°C heat sink. The device can dissipate 40W indefinitely if connected to a 25°C heat sink, and that the maximum safe limit energy dissipated during a current limit pulse is 3.2J. Peak die temperature increase due to a short pulse of 3.2J is 32°C as the energy is mostly absorbed in the die initially. Junction temperature stabilizes at nominally 92°C - 25° = 67° above heatsink temperature under 40W dissipation (Figure 2), with the package base rising to 92°C - (40W x 1.2°C/W) = 44°C.

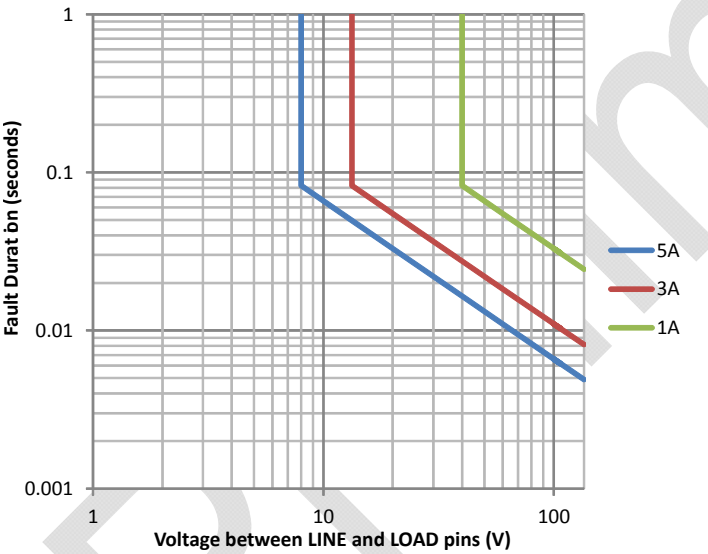


Figure 1. Maximum Safe Operating Curve

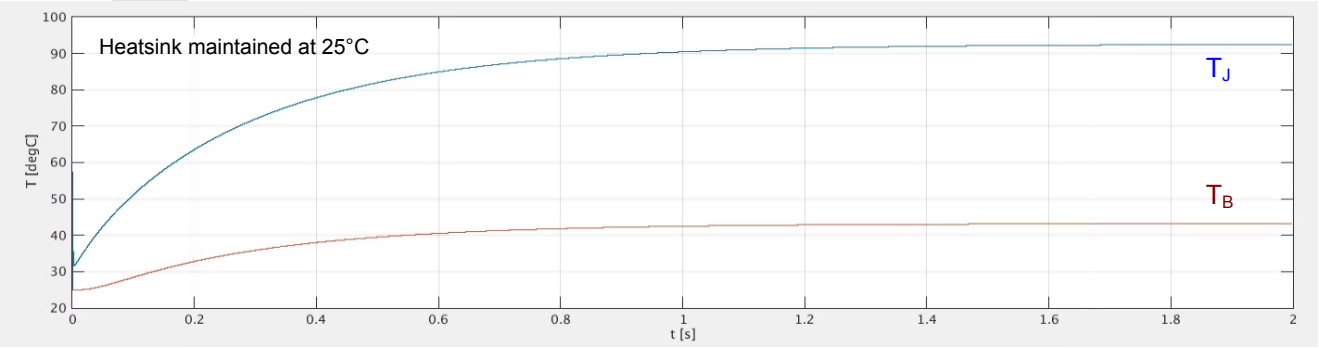


Figure 2. Die and Package Base Temperature Rise Over Time with 40W Dissipation

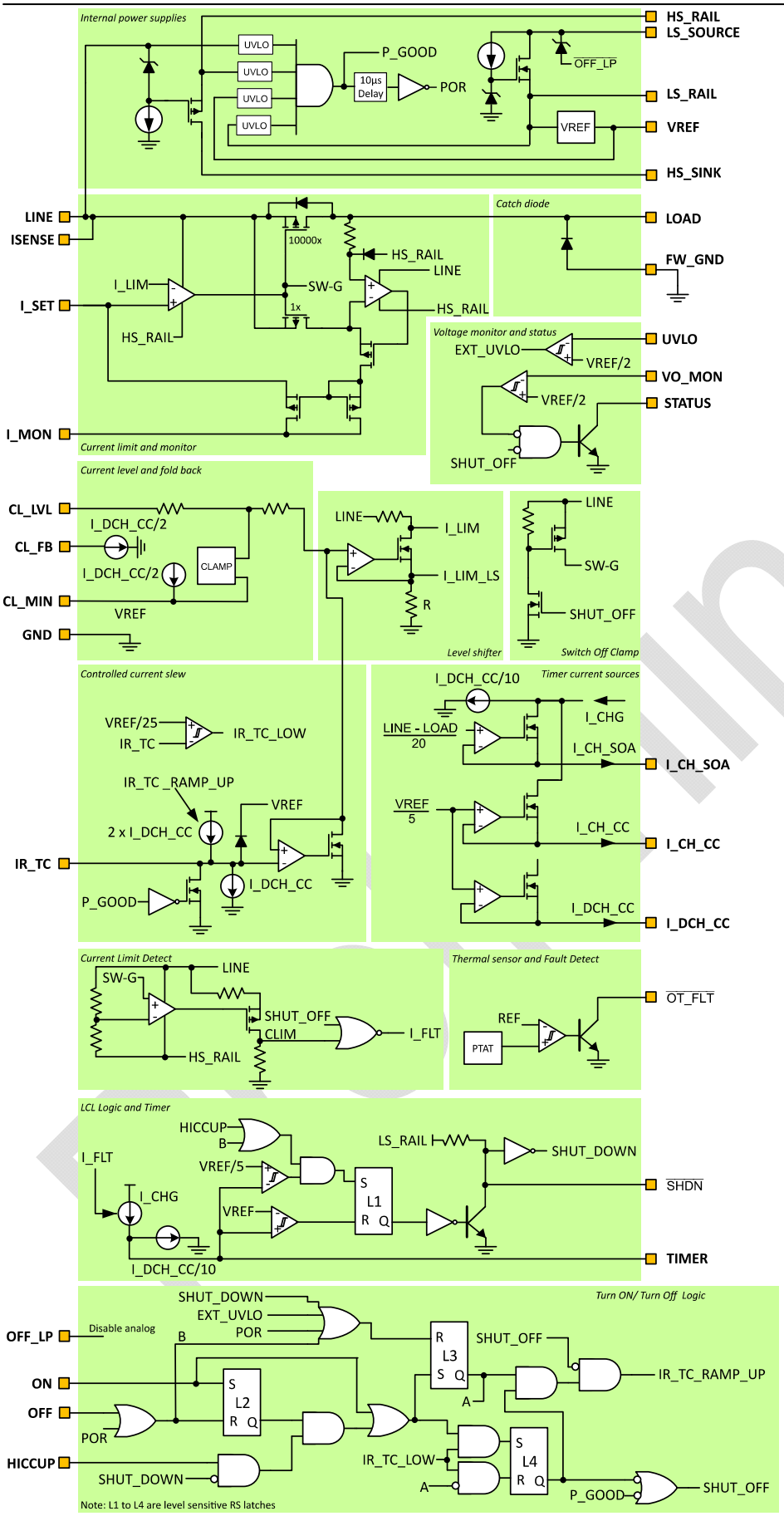


Figure 3. Functional Block Diagram

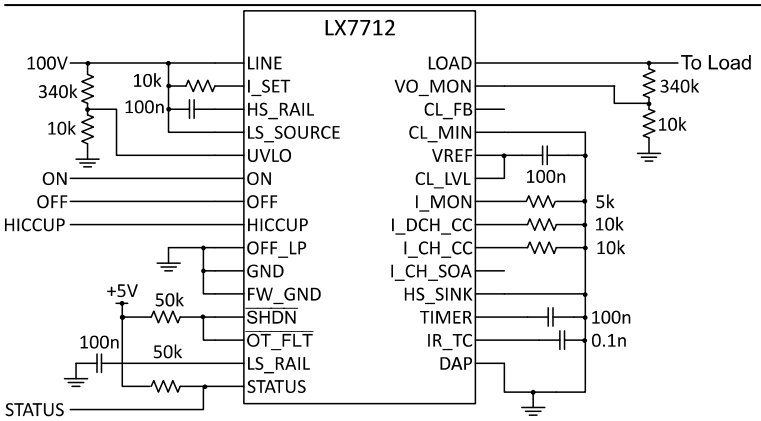


Figure 4. Example Application - Latching 5A Current Limit with 1A/µs Slew Control and 5ms Fault Timer

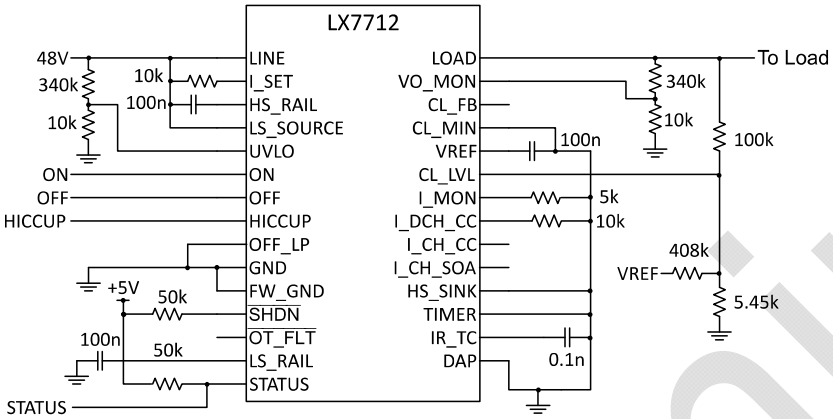


Figure 5. Example Application - Foldback 5A Current Limit with 1A/µs Slew Control

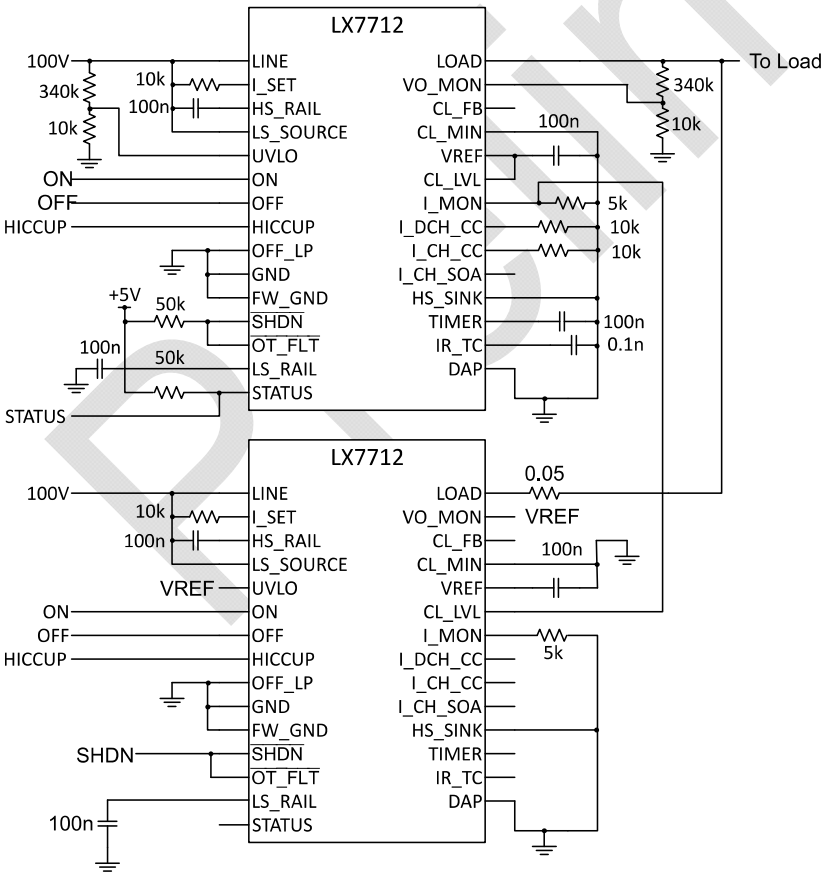


Figure 6. Example Application - Latching 10A Current Limit with 1A/µs Slew Control and 5ms Fault Timer

11 LX7712 System Outline

The LX7712 is a versatile, configurable, resettable e-fuse with integrated PMOS power switch rated at 5A continuous current. The current sensing is performed using a SenseFET which contains a tiny current sense FET buried in the main switch FET body. A closed-loop amplifier matches the operating conditions of the current sense device to the power switch, which ensures that the sense current represents a consistent fraction of the power switch current.

The LX7712's power switch has a reverse body diode, as shown in the Functional Block Diagram on page 10, which provides a path from the LOAD output to the LINE input when the power switch is turned off. See section 17 on page 25 for details how to add an external reverse PFET to block the reverse path automatically when the LX7712 is off.

The LX7712 functional blocks are:

- Internal power supplies and voltage reference (section 12 on page 12)
- ON, OFF, and OFF_LP control inputs (section 13 on page 15)
- Internal under-voltage lockouts and LINE and LOAD voltage monitoring and (sections 13.1 and 13.2 on page 16)
- STATUS output and $\overline{\text{SHDN}}$ I/O (sections 13.3 and 13.4 on page 16)
- Over-temperature detection (section 13.5 on page 16)
- Current monitoring system (section 14 on page 17)
- Current limiting with current ramp control, and a hard or foldback current limit options (section 15 on page 18)
- Overload fault energy integration fault timer and hiccup fault recovery fault timer (section 16 on page 21)

12 Power Supplies, Voltage Reference, and Decoupling

The LX7712 generates two internal rails to operate the internal control circuits, HS_RAIL and LS_RAIL, and an internal 5V reference, VREF (Figure 7). LINE, HS_RAIL, LS_RAIL, and VREF have independent under-voltage detectors which will cause the LX7712 to shut off the power switch if any rail falls too low (section 13.1 on page 16).

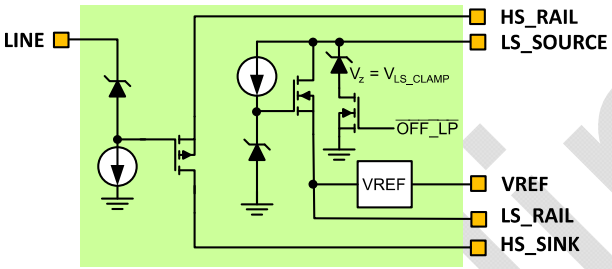


Figure 7. HS_RAIL, LS_RAIL, and VREF

12.1 Reference Output VREF

The reference is available to bias the external resistor configuration networks and is accurate to ±4% over LINE voltage variations with external loading up to 2mA, plus another ±1% tolerance over the -55°C to +125°C temperature range. Bypass VREF with a 100nF capacitor to GND, even if no external loading is applied.

12.2 HS_SINK and HS_RAIL

HS_RAIL is the output of an internal linear regulator which floats at 10V ±1V below LINE. Bypass HS_RAIL with a 100nF capacitor to LINE. HS_RAIL only sinks current (acts as a return).

The HS_RAIL regulator's input is the HS_SINK pin, to be connected to a voltage at least 12V below VLINE, typically GND. This regulator dissipates typically $\{V_{LINE} - 10\}$ mW. For higher LINE voltages, such as above 60V, it is helpful to connect HS_SINK to GND via a series resistor to move some dissipation off-chip. A suitable resistance would be:

Equation 1: $R_{HS\_SINK} = 600 \times \left(V_{LINE(min)} - 12\right) \Omega \pm 10\%$

where $V_{LINE(min)}$ is the lowest LINE input voltage expected.

So, for an example application where V_{LINE} varies from 80V to 120V: $R_{HS\_SINK} = 600 \times (80 - 12) = 40.8k\Omega \pm 10\%$

Since the maximum draw from HS_RAIL is 1.5mA, maximum R_{HS_SINK} dissipation will be $1.5mA^2 \times 40.8k\Omega = 91.8mW$ at the nominal resistor value.

12.3 LS_SOURCE and LS_RAIL

LS_RAIL is the output of an internal linear regulator which delivers 10V ±1V above GND. Bypass LS_RAIL with a 100nF to 2.2µF capacitor to GND. LS_RAIL can source up to 5mA to external loads in addition the 10mA max it provides to the internal circuits.

The LS_RAIL regulator's input is the LS_SOURCE pin, which has an internal 33V nominal (32V to 36V) Zener clamp to GND. The clamp is enabled in normal operation and disabled in low power shutdown when OFF_LP is high (Figure 7 on page 12). The purpose of the 33V Zener clamp is to assist in managing dissipation in the LS_RAIL regulator pass element, which is rated at 225mW. The Zener is rated at an additional 225mW.

When the LX7712 is put into sleep mode via OFF_LP pin, the Zener clamp is disconnected. Since no current is shunted by the Zener, current consumption is just the LX7712's sleep mode current.

Table 1 and Figure 8 below show the options for powering LS_SOURCE and LS_RAIL.

LINE Voltage	LS_SOURCE and LS_RAIL Connection
Any	Connect LS_SOURCE and LS_RAIL together to an external 10V ±1V supply
Any	Connect LS_SOURCE to an existing 12V to 28V supply, which can be LINE if within this range
$V_{LINE(MAX)}$ > 28V	Connect LS_SOURCE to LINE via a series resistor. Note: VLINE(MIN) > 12V, and (VLINE(MAX) - VLINE(MIN)) ≤ 20V
	Connect LS_SOURCE to LINE via a 12V to 28V NMOS or NPN pre-regulator (Figure 8)

Table 1. LS_SOURCE and LS_RAIL Supply Options

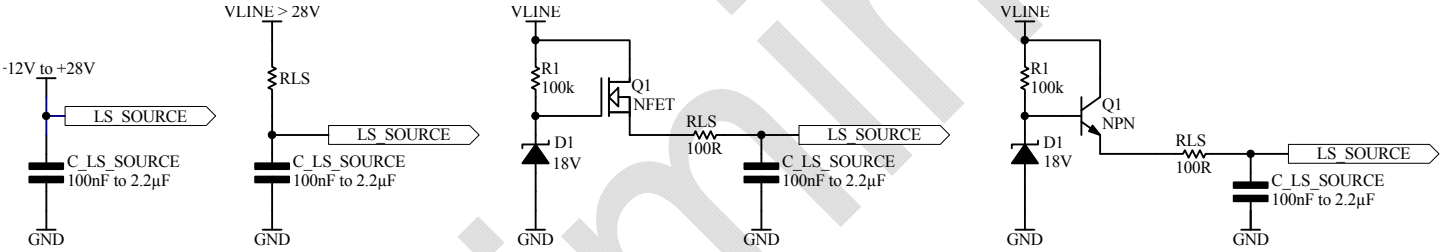


Figure 8. LS_SOURCE and LS_RAIL Supply Options: Direct, Series Resistor, and Pre-Regulator

If LS_SOURCE is to be supplied from the LINE supply greater than 28V, a single series can be used if the range of LINE variation is 20V or less. The equations below and examples show that the limitation is the dissipation of the internal Zener diode. For wide ranging LINE input, a simple pre-regulator is recommended. This is a source/emitter follower using an NMOS or NPS pass transistor. The 100Ω resistor limits the peak charging current into the output capacitor on power-up.

The equations to calculate the resistor between LINE and LS_SOURCE pin use:

$V_{LINE(MAX)}$ is the maximum line input voltage
$V_{LINE(MIN)}$ is the minimum line input voltage
$V_{Z(MIN)}$ is the minimum Zener voltage (32V)
I_Z is the current passing through the Zener
$V_{LS\_SOURCE(MIN)}$ is the minimum allowed LS_SOURCE voltage (12V)
$I_{LS\_SOURCE(MAX)}$ is the maximum LS_SOURCE current draw (10mA)
$I_{LS\_SOURCE(MIN)}$ is the minimum LS_SOURCE current draw (3.5mA)
R_{LS} is the resistor between LINE and LS_SOURCE pin

The maximum allowed series resistance is set by the minimum LINE voltage and maximum current:

Equation 2: $$R_{LS(MAX)} = \frac{V_{LINE(MIN)} - V_{LS\_SOURCE(MIN)}}{I_{LS\_SOURCE(MAX)}} = \frac{V_{LINE(MIN)} - 12}{10mA}\ \Omega$$

This allows R_{LS} to be chosen, with tolerance range from $R_{LS(MAX)}$ to $R_{LS(MIN)}$.

At $V_{LINE(MAX)}$ the maximum current that can pass through the Zener can be calculated. There are two possible maximum currents, using tolerance limits:

Equation 3: $I_{Z(MAX)} = \frac{V_{LINE(MAX)} - V_{Z(MIN)}}{R_{LS(MIN)}} - I_{LS\_SOURCE(MIN)} = \left[\frac{V_{LINE(MAX)} - 32}{R_{LS(MIN)}} - 3.5mA\right] A$

Equation 4: $I_{Z(MAX)} = \frac{V_{LINE(MAX)} - V_{Z(MAX)}}{R_{LS(MIN)}} - I_{LS\_SOURCE(MIN)} = \left[\frac{V_{LINE(MAX)} - 36}{R_{LS(MIN)}} - 3.5mA\right] A$

Example specification 1: V_{LINE} = 22V to 38V
From Equation 2:

$$R_{LS(MAX)} = \frac{22 - 12}{10mA} = 1000\Omega$$

Choosing R_{LS} to be 950Ω ±50Ω, $R_{LS(MIN)}$ = 900Ω

From Equation 3:

$$I_{Z(MAX)} = \left[\frac{38 - 32}{900} - 3.5mA\right] = 3.17mA$$

Zener dissipation is 32V x 3.17mA = 101mW, under the 225mW limit

Example specification 2: V_{LINE} = 20V to 40V
From Equation 2:

$$R_{LS(MAX)} = \frac{20 - 12}{10mA} = 800\Omega$$

Choosing R_{LS} to be 787Ω ±1%, $R_{LS(MIN)}$ = 779.1Ω

From Equation 3:

$$I_{Z(MAX)} = \left[\frac{40 - 32}{779.1} - 3.5mA\right] = 6.77mA$$

Zener dissipation is 32V x 6.77mA = 217mW, under the 225mW limit

Example specification 3: V_{LINE} = 100V to 120V
From Equation 2:

$$R_{LS(MAX)} = \frac{100 - 12}{10mA} = 8800\Omega$$

Choosing R_{LS} to be 8.66kΩ ±1%, $R_{LS(MIN)}$ = 8.57kΩ

From Equation 3:

$$I_{Z(MAX)} = \left[\frac{120 - 32}{8.57k} - 3.5mA\right] = 6.76mA$$

Zener dissipation is 32V x 6.76mA = 216mW, under the 225mW limit

From Equation 4:

$$I_{Z(MAX)} = \left[\frac{120 - 36}{8.57k} - 3.5mA\right] = 6.30mA$$

Zener dissipation is 36V x 6.30mA = 227mW, just over the 225mW limit. R_{LS} needs to be 8.66kΩ ±0.5% to pass.

13 On and Off Controls

The basis of the power switch's on/off mechanism is an internal RS latch operated by the ON and OFF logic inputs, which initiate a programmable slew rate control which limits the rate of the load current increase during turn-on, and decrease during turn-off (see the Current Limiting and Slew Rate Limiting section on page 18).

There is negligible difference in LX7712 power consumption whether the power switch is on or off. The optional OFF_LP input reduces power consumption for long standby periods by powering down much of the internal circuitry. The OFF_LP input is not latched, unlike the ON and OFF inputs, and must be maintained logic high to assert low power mode. Taking OFF_LP high overrides the ON and OFF inputs. The OFF and OFF_LP inputs can be tied together, and a 1µs to 10µs pulse high used to set the internal RS latch OFF without the LX7712 entering low power mode (C_{LS_SOURCE} ≥ 100nF).

The power switch is turned on by a logic-high level (or a high pulse ≥ 1µs) on the ON input. The ON control is overridden, and the power switch turned off, by either a logic input (OFF, OFF_LP, or $\overline{SHDN}$), by the UVLO comparator input, by a latched current limit fault, or by under-voltage on a supply rail.

Control Mode	UVLO Input pin 27	$\overline{SHDN}$ I/O pin 47	ON Input pin 40	OFF Input pin 39	OFF_LP Input pin 38
Normal On/Off Operation in either LCL Mode (HICCUP = low or hi-z) or RLCL Mode (HICCUP = high)					
Switch on via ON input with slew control in LCL Mode (HICCUP = low or hi-z))	V_{UVLO} > VREF/2	High	↑ or ↓	Low	Low
Switch on via ON input with slew control in RLCL Mode (HICCUP = high)			High	Low	Low
Switch off with slew control via OFF input		High	x	↑ or ↓	Low
Switch off instantly into low power mode via OFF_LP input		High	x	x	High
Switch off instantly into low power mode via OFF and OFF_LP inputs connected together		High	x	High	
Switch off with slew control, and then sometime during or after the slew time enter low power mode via OFF and OFF_LP inputs connected together		High	x	↑ for 1µs to 10µs to initiate switch off with slew control. During or after slew time, ↑ to enter low power mode	
Current Limit Fault Handling in LCL Mode (HICCUP = low or hi-z)					
Automatic switch off with slew control due to a timed-out and latched current limit fault	V_{UVLO} > VREF/2	Internally pulled down	↑ or ↓	Both low since power switch was turned on via ON input	
Check whether LX7712 is still in the cool-down timer period; the power switch cannot be turned-on again until the cool-down period has ended and $\overline{SHDN}$ → high (OFF and OFF_LP separate)		Internally pulled down (in cool-down period) → high (when cool-down ends and OFF is high)	x	High	Low
Check whether LX7712 is still in the cool-down timer period; the power switch cannot be turned-on again until the cool-down period has ended and $\overline{SHDN}$ → high (OFF and OFF_LP inputs connected together)		Internally pulled down (in cool-down period) → high (when cool-down ends and OFF is high)	x	↑ for 1µs to 10µs to clear $\overline{SHDN}$	Low
Switch back on via ON input with slew control once the cool-down period has ended		Must be high before; remains high after	↑ or ↓	Low	Low
Current Limit Fault Handling in RLCL Mode (HICCUP = high)					
Automatic switch off with slew control due to a timed-out and latched current limit fault	V_{UVLO} > VREF/2	Internally pulled down	↑ or ↓	Both low since power switch was turned on via ON input	
Automatic switch on with slew control once the cool-down period has ended		High	↑ or ↓	Both low since power switch was turned on via ON input	
Behavior Under Under-Voltage Conditions and using $\overline{SHDN}$ pin					
Automatic switch off due to under-voltage on either LINE or LS_RAIL	x	x	x	x	x
Switch off with slew control via $\overline{SHDN}$ pin	V_{UVLO} > VREF/2	Externally pulled down	x	x	x
Switch off with slew control via UVLO pin	V_{UVLO} < VREF/2	x	x	x	x

Table 2. On and Off Controls

13.1 Internal Under-Voltage Lockout

The LX7712 includes under-voltage comparators monitoring the LINE input voltage, the HS_RAIL regulated from LINE, the LS_RAIL regulated supply, and VREF (Figure 9 below). The power switch is turned off while any one of these supplies is under-voltage. If the ON input is high and both the OFF and OFF_LP inputs are low when the under-voltage event(s) clear, such as after power-up, then the power switch will turn on.

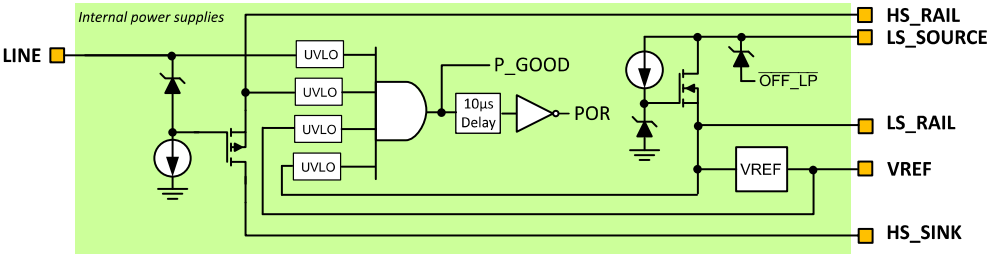


Figure 9. Internal Regulators and Under Voltage Detectors

13.2 External Voltage Monitor Inputs UVLO and VO_MON

The LX7712 includes two under-voltage comparators with a threshold of VREF/2, nominally 2.5V (Figure 10 below).

UVLO is intended to monitor the LINE input via 2-resistor potential divider from LINE to GND. If a voltage under VREF/2 is detected on UVLO, a power switch turn off with slew rate control is initiated. When the voltage on the UVLO pin exceeds VREF/2, the power switch will remain off or turn on with slew rate control depending on the state of the ON, OFF, and OFF_LP inputs. Tie UVLO to VREF if unused.

VO_MON is intended to monitor the LOAD output via 2-resistor potential divider from LOAD to GND. If a voltage under VREF/2 is detected on VO_MON, the STATUS output goes hi-z to indicate that LOAD output is under-voltage. Tie VO_MON to VREF if unused.

A 10kΩ resistor is recommended for GND-side resistor in the potential dividers. The value of the high-side resistor (to LINE or LOAD) is therefore {(4 x V_{TRIP}) - 10} kΩ, where V_{TRIP} is the desired under-voltage trip threshold.

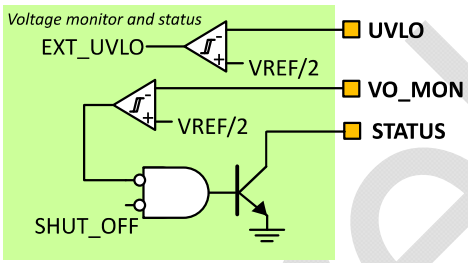


Figure 10. External UVLO

13.3 Status Output STATUS

The open-collector STATUS output is low when the power switch is on and the VO_MON comparator indicates the LOAD voltage is above the user-configured LOAD minimum voltage. Fit a resistor from STATUS to a supply up to 6V to provide the desired logic high output.

13.4 Shutdown I/O $\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin is an open-collector I/O. As an output, a low logic output signal indicates that an LCL timeout has triggered the shutdown latch. $\overline{\text{SHDN}}$ can also be used as a shutdown input from another device, and multiple LX7712s can interconnect $\overline{\text{SHDN}}$ to cross-couple shutdown events. Fit a resistor from $\overline{\text{SHDN}}$ to a supply up to 6V to provide the desired logic high output.

13.5 Over Temperature Output $\overline{\text{OT\_FLT}}$

The $\overline{\text{OT\_FLT}}$ output trips active low on die over-temperature, with nominally 50°C hysteresis. $\overline{\text{OT\_FLT}}$ can be connected to $\overline{\text{SHDN}}$ to shut down the LX7712 automatically during over-temperature faults. Fit a resistor from $\overline{\text{OT\_FLT}}$ to a supply up to 6V to provide the desired logic high output, unless connected to $\overline{\text{SHDN}}$ with an existing pullup resistor.

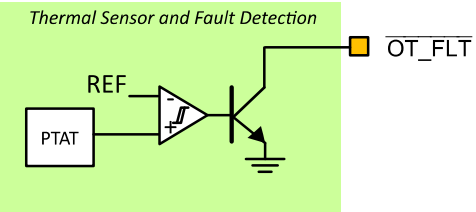


Figure 11. Over-Temperature Fault Output

14 Current Monitoring System

The LX7712 uses a SenseFET architecture comprising an extra current sense PFET buried in the power switch PFET body. The current sense PFET is 1/10,000 the size of the power switch PFET, and mirrors 1/10,000 of the load current if it's V_{DS} is kept the same as the power switch PFET's V_{DS}, which is V_{LINE} - V_{LOAD}. This is managed by the sense amplifier in Figure 12 below.

The sense amplifier sources the sense current (1/10,000 of the switch current) into the right-hand side of the sense current mirror. This mirror sinks the same current from the LINE input supply through the external resistor R_{I_SET} via the I_SET pin. The combined current from the two sides of the mirror, 1/5,000 of the switch current, goes to ground through the external resistor R_{I_MON} via the I_MON pin. The voltage at I_MON provides a ground-referenced measure of the load current passing through the switch.

The recommended value for R_{I_SET} is 10kΩ for all current limit requirements. The voltage V_{I_SET} across R_{I_SET} is then 1V per amp of load current, and 5V maximum at 5A load current, I_{LOAD} (Equation 5).

Equation 5. $$V_{I\_SET} = \frac{I_{LOAD} \times R_{I\_SET}}{10000} = \frac{I_{LOAD} \times 10000}{10000} = I_{LOAD} \text{ V}$$

The recommended maximum value for R_{I_MON} is 5kΩ maximum for a 5A current limit requirement, with V_{LINE} ≥ 15V. This sets a 5V full-scale output V_{I_MON} for load current monitoring (Equation 6). For 12V ≤ V_{LINE} < 15V, the full-scale output must be dropped accordingly. For $V_{LINE(MIN)}$ = 12V, 13V, and 14V use R_{I_MON} = 2kΩ, 3kΩ, and 4kΩ maximum to set a corresponding 2V, 3V, and 4V full scale output V_{I_MON}.

Equation 6. $$V_{I\_MON} = \frac{I_{LOAD} \times R_{I\_MON}}{5000} \text{ V}$$

If the LX7712 is configured for a lower than 5A current limit (I_{LOAD}), then the value of R_{I_MON} can be increased to maintain a 5V full scale output V_{I_MON} at the lower current. For example, use R_{I_MON} = 12.5kΩ for a 2A current limit application (Equation 7).

Equation 7. $$R_{I\_SET(max)} = \frac{V_{I\_MON} \times 5000}{I_{LOAD}} = \frac{5 \times 5000}{I_{LOAD}} = \frac{25000}{I_{LOAD}} \ \Omega$$

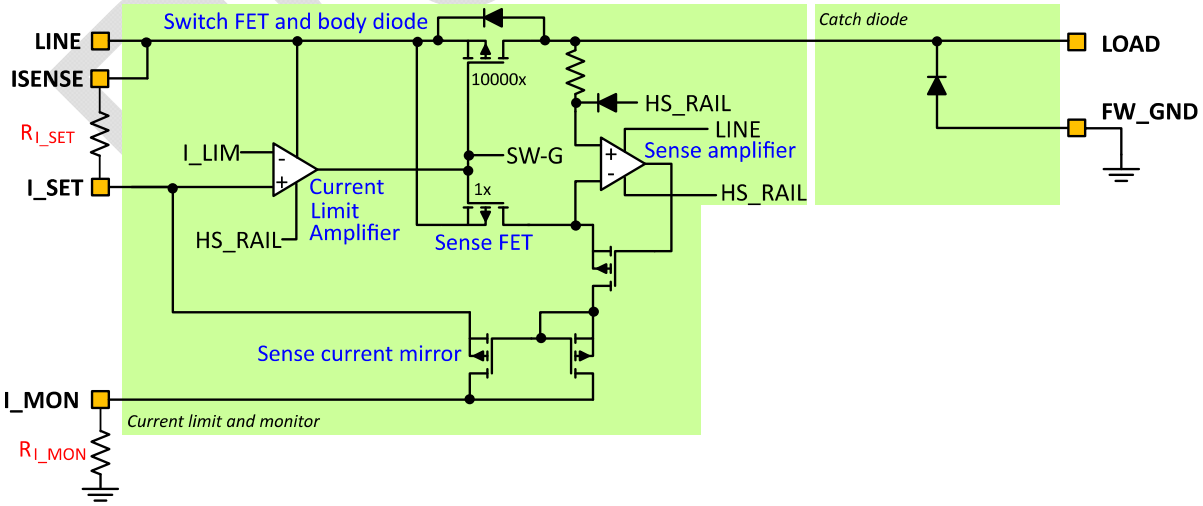


Figure 12. Power Switch and Current Sense Circuit

15 Current Limiting and Slew Rate Limiting

The LX7712 has configurable current limiting and slew rate control. The current limit can be set to either a hard limit or a fold-back limit. See the Fault Timer section 16 on page 21 on setting how long a sustained over-current fault (or multiple short over-current fault in quick succession) can be sustained before the power switch is turned off.

15.1 Slew Rate Limiting

The slew rate control limits the rate of the load current increase when the power switch is turned on, and an identical ramp down when the power switch is turned off. During the slew time, the power switch current limit ramps up from 0A to the configured current limit. The slew time is set by the combination of an external capacitor C_{IR_TC} on the IR_TC pin, and the constant current I_{DCH_CC} set by resistor R_{DCH_CC} on the I_DCH_CC pin (Figure 13 below).

At power switch turn-on, C_{IR_TC} starts discharged, and charges from 0V to VREF with constant current I_{DCH_CC}. At power switch turn-off, C_{IR_TC} discharges from VREF to 0V at I_{DCH_CC}, causing a matching power switch current limit ramp down.

The value of resistor R_{DCH_CC} is normally selected to suit the fault timer (Section 16 on page 21). If the fault timer function is disabled, then select a value for R_{DCH_CC} in the range 10kΩ to 100kΩ from the I_DCH_CC pin to GND to suit the slew control requirements. Leave the IR_TC pin open (no external capacitor C_{IR_TC}) to select the fastest slew rate.

The complete slew time is the time taken to charge C_{IR_TC} from 0V to VREF with constant current I_{DCH_CC}:

Equation 8: $$t_{SLEW} = \frac{C_{IR\_TC} \times VREF}{I_{DCH\_CC}} \ s$$

Substituting $I_{DCH\_CC} = \frac{VREF}{5 \times R_{DCH\_CC}} \ A$ from Table 4 on page 22, this simplifies to:

Equation 9: $$t_{SLEW} = 5 \times C_{IR\_TC} \times R_{DCH\_CC} \ s$$

For example, the ramp time using C_{IR_TC} = 100nF and R_{DCH_CC} = 100kΩ is $t_{SLEW} = 5 \times 100n \times 100k = 50ms$.

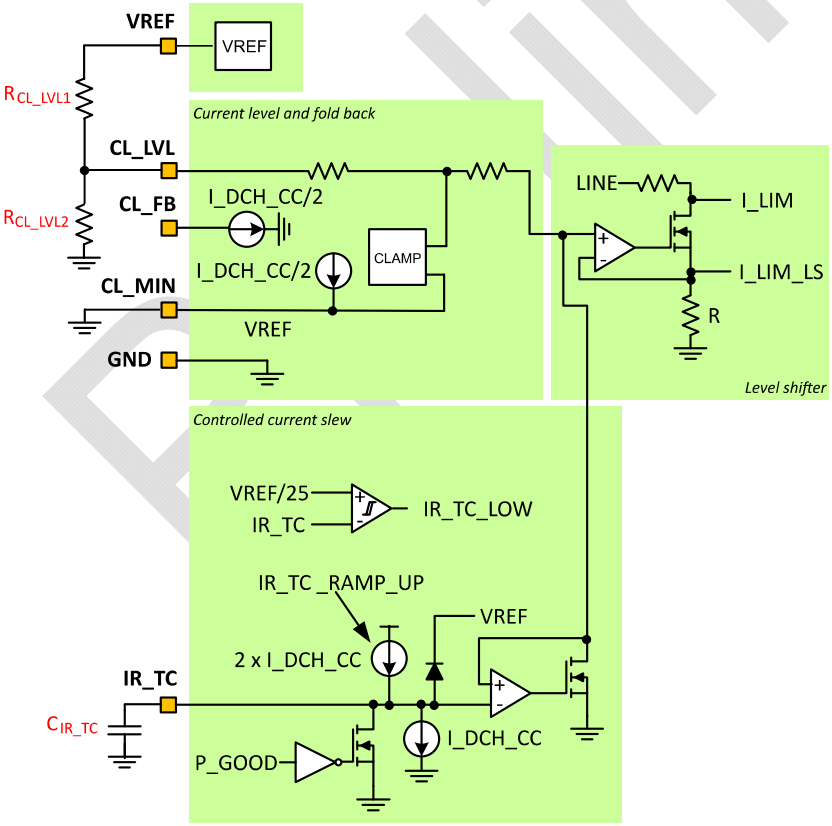


Figure 13. Current Limiting Without Foldback

15.2 Setting a Hard Current Limit (no foldback)

The current limit amplifier in Figure 12 compares the I_SET voltage (which is a measure of load current) with the I_LIM reference voltage. Both these voltages are with respect to the line input voltage.

The I_LIM reference voltage is set by two resistors R_{CL_LVL1} and R_{CL_LVL2} at the CL_LVL pin with respect to GND (Figure 13 on page 18). The current limit occurs when the magnitude of $V_{I\_SET} = V_{CL\_LVL}$ (ignoring that V_{I_SET} is with respect to V_{LINE}, while V_{CL_LVL} is with respect to GND).

At current limit:

Equation 10. $$V_{I\_SET} = V_{CL\_LVL} = \frac{I_{LOAD} \times R_{I\_SET}}{10000} = \frac{VREF \times R_{CL\_LVL2}}{R_{CL\_LVL1} + R_{CL\_LVL2}}$$

Substituting the recommended R_{I_SET} = 10kΩ and solving for R_{CL_LVL1} this simplifies to:

Equation 11. $$R_{CL\_LVL1} = R_{CL\_LVL2} \times \left(\frac{VREF}{I_{LOAD}} - 1\right) \Omega$$

Table 3 shows typical ideal resistor values, using VREF = 5V.

Current Limit	R_{CL_LVL1}	R_{CL_LVL2}
5A	Tie to VREF	-
4.5A	2kΩ	18kΩ
4A	4kΩ	16kΩ
3.5A	6kΩ	14kΩ
3A	8kΩ	12kΩ
2.5A	10kΩ	10kΩ
2A	12kΩ	8kΩ
1.5A	14kΩ	6kΩ
1A	16kΩ	4kΩ

Table 3. Example Current Limit Resistor Values

15.3 Setting a Fold-back Current Limit

The fold-back current limit mode is selected by using a resistive network that drives CL_LVL based on VREF and LOAD voltage levels. The fold-back current limit is designed to reduce the current to a safe level in the event of a load fault and provide automatic recovery when the fault is removed. The switch will dissipate power if operated with a high current in linear mode; this occurs when using the traditional feedback mode. To prevent excessive die temperature with a soft short, an over temperature detect circuit can be configured to force a latched shutdown.

For a traditional current foldback configured part, the current limit is determined by the following equations. Picking a value for R_A allows R_B and R_C to be determined:

Equation 12. $$I_{LIM} = \frac{10000}{R_{I\_SET}} \times \left[\left(V_{LOAD} \times \frac{R_B \parallel R_C}{R_A + (R_B \parallel R_C)}\right) + \left(V_{VREF} \times \frac{R_A \parallel R_B}{R_C + (R_A \parallel R_B)}\right)\right] A$$

Equation 13. $$I_{SC} = \frac{10000}{R_{I\_SET}} \times V_{VREF} \times \frac{R_A \parallel R_B}{R_C + (R_A \parallel R_B)} A$$

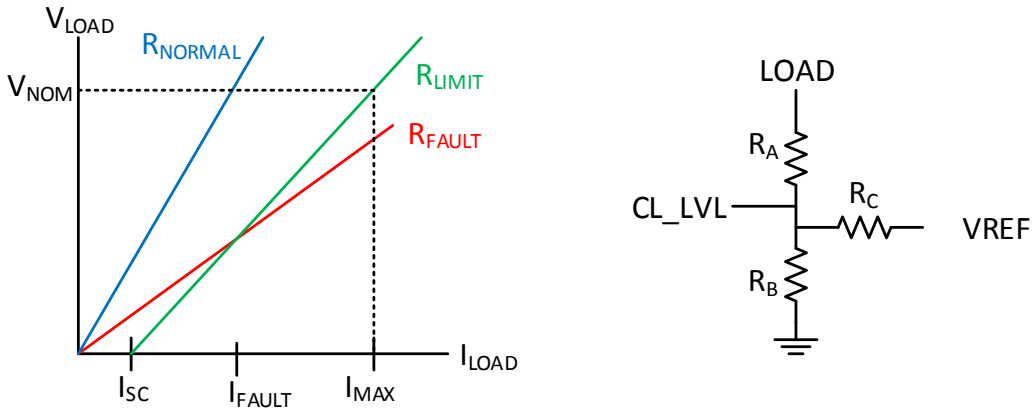


Figure 14. Traditional Current Fold-back

The bi-level fold-back configuration contains a soft short prevention provision that deters stable operation under high switch current with high switch voltage conditions. The current limit load line is purposely tilted so that a resistive overload will not settle at an intermediate level of fault current. The level of negative offset is determined by an $I_{DCH\_CC}/2$ current sink that will offset the built-in level shifter. The fault current is determined by the voltage applied to the CL_LVL pin.

Equation 14. $$I_{LIM} = \frac{10000}{R_{I\_SET}} \times \left[\left(V_{LOAD} \times \frac{R_B}{R_A + R_B} \right) - \left(\frac{I_{DCH\_CC}}{2} \times \left(R_C + \left(R_A \parallel R_B \right) \right) \right) \right] A$$

Equation 15. $$I_{FAULT} = \frac{10000 \times V_{CL\_MIN}}{R_{I\_SET}} A$$

The current limit is the greater of I_{LIM} or I_{FAULT}, and $I_{LIM} = I_{MAX}$ when $V_{LOAD} = V_{NOM}$. Automatic recovery occurs when the load is reduced to the point that:

Equation 16. $$V_{LOAD} = I_{FAULT} \times R_{LOAD} = \left(V_{CL\_MIN} + \left(\frac{I_{DCH\_CC}}{2} \times \left(R_C + \left(R_A \parallel R_B \right) \right) \right) \right) \times \frac{R_A + R_B}{R_B} V$$

Additionally, the CL_MIN pin has also a current source equal to $I_{DCH\_CC}/2$, so instead of forcing a voltage on this pin the controlled voltage is obtained by just connecting a resistor to ground on the CL_MIN pin:

Equation 17. $$V_{CL\_MIN} = R_{CL\_MIN} \times \frac{I_{DCH\_CC}}{2}$$

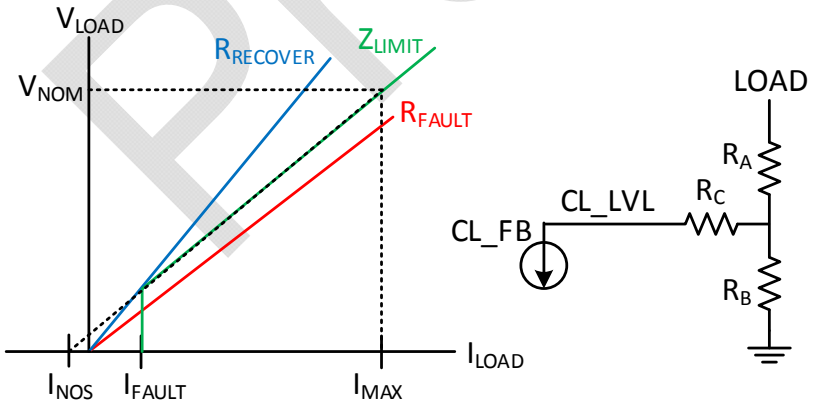


Figure 15. Bi-Level Fold-back

16 Fault Timer

The LX7712 uses a fault timer to determine how long an over-current fault can be sustained before the power switch is turned off. This fault timer is the LX7712's primary safe dissipation manager. The secondary system is the die over-temperature detection and associated auto-shutdown logic. The fault timer is configured by the user to initially maintain a fault energy pulse under the LX7712's 3.2J rating, and then to allow enough time for the system to remove the heat.

The fault timer operates as a dual-slope integrator around external capacitor C_{TIMER}, and external resistors R_{CH_CC}, R_{CH_SOA}, and R_{DCH_CC} (Figure 16 below). The capacitor charge/discharge time constants emulate the cumulative ongoing energy absorption of the power switch, and the subsequent conduction of that thermal energy into the system's heatsink.

To disable the fault timer, tie the TIMER pin to GND, leave the I_CH_SOA and I_CH_CC pins open, and fit resistor R_{DCH_CC} in the range 10kΩ to 100kΩ from the I_DCH_CC pin to GND. The current I_{DCH_CC} set by R_{DCH_CC} is used for slew control (see the Slew Rate Limiting section 15.1 on page 18) even if the fault timer is unused.

R_{CH_CC} and R_{CH_SOA} set capacitor *charging* currents and define the time that an over-current fault is sustained before the power switch is turned off. Resistor R_{CH_CC} sets a fixed charge current. Resistor R_{CH_SOA} sets a charge current that is proportional to power switch dissipation, therefore varying with time depending on the nature of the load fault. The fault timer latches the power switch off when the voltage across C_{TIMER} rises to VREF (Figure 17 on page 22).

R_{DCH_CC} sets the capacitor *discharging* current and defines the time that the power switch must remain off. This emulates the heatsink's thermal time constant to dissipate the heat built up during a current limit fault. R_{DCH_CC} discharges C_{TIMER} from VREF to a trip point of VREF/5, after which the power switch can be turned back on. Note that the current set by R_{DCH_CC} is used a reference current (I_{DCH_CC}) by the current limit and slew control circuits (Section 15 on page 18).

If any over-current fault is of too short a duration to trigger the fault timer threshold, C_{TIMER} still retains the voltage it charged to during the fault. This provides a cumulative effect, so multiple short over-current pulses occurring in a short period of time (before the discharge current clears C_{TIMER}) can eventually trigger the fault timer threshold.

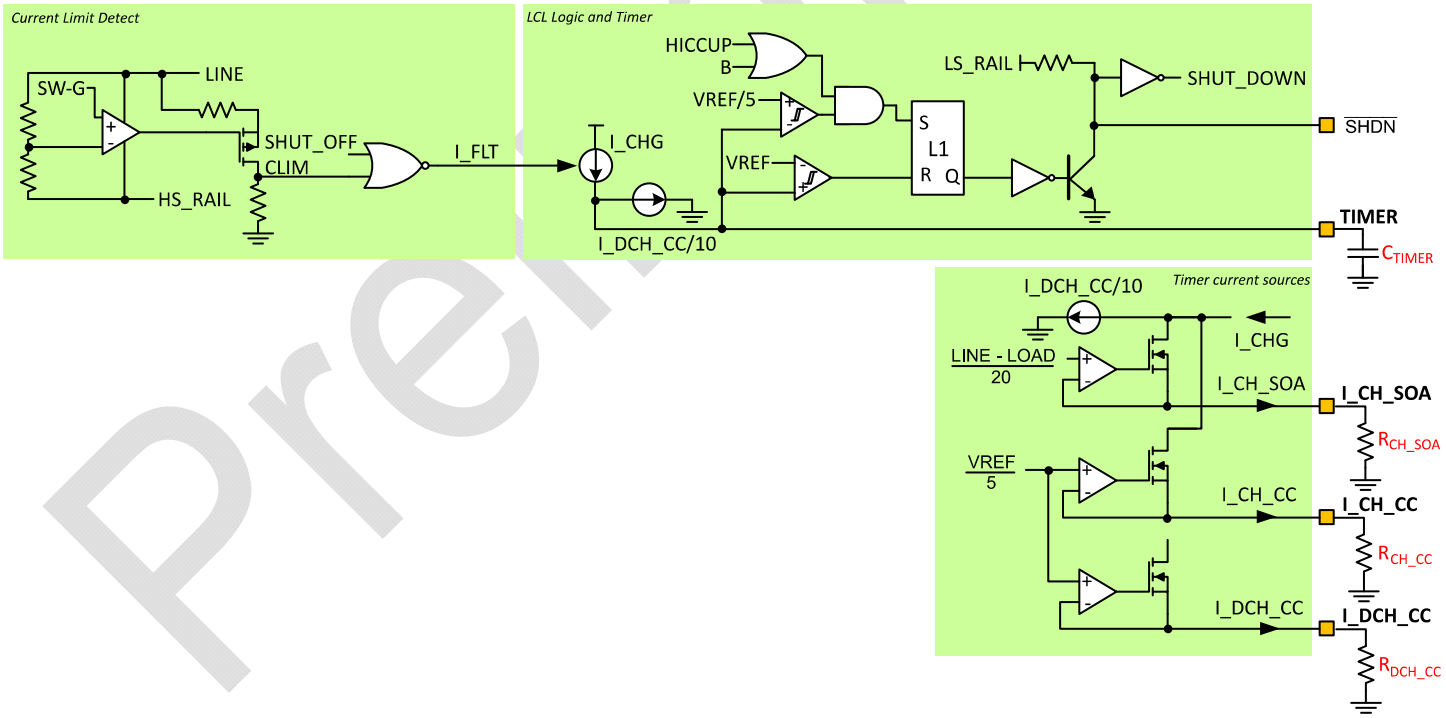


Figure 16. Fault Timer Current Sources and Sink

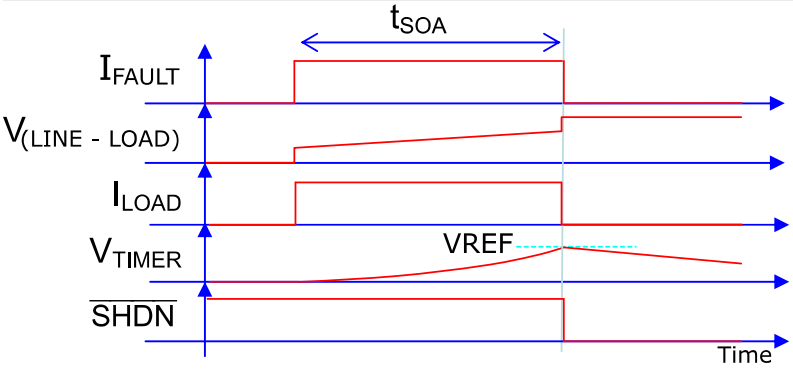


Figure 17. Power Switch Energy Rising During Fault

In LCL (latched current limiting) mode, the power switch remains latched off after the load switch is turned off due to an over-current fault. The LX7712 can be restarted through the ON logic input after the fault timer discharge time (C_{TIMER} discharged to VREF/5). To enable LCL mode, tie the HICCUP pin 13 to GND.

In RLCL (retriggerable latched current limiting) or hiccup mode, the power switch remains off until the fault timer discharge time has tripped (C_{TIMER} discharged to VREF/5), and then restarts automatically. To enable RLCL/hiccup mode, tie the HICCUP pin 13 to logic high (3.3V, 5V, or the 5V VREF pin 20).

16.1 Fault Timer Component Selection

The fault timer equations are given in Table 4 below, where:

R_{CH_CC} is the external resistor from I_CH_CC pin 21 to GND which sets the current I_{CH_CC}
R_{CH_SOA} is the external resistor from I_CH_SOA pin 22 to GND which sets the current I_{CH_SOA}
R_{DCH_CC} is the external resistor from I_DCH_CC pin 23 to GND which sets the current I_{DCH_CC}
C_{TIMER} is the external capacitor from TIMER pin 25 to GND
VREF is the internal 5V reference voltage on pin 20
V_{LINE} is the line input to the power switch, pins 1 to 8, and 48
V_{LOAD} is the voltage at the output of the power switch, pins 29 to 37

The preferred range of values for R_{CH_CC}, R_{CH_SOA}, and R_{DCH_CC} are 10kΩ to 100kΩ, because the fault timer trip voltages are guaranteed in the electrical characteristics for this range. However, resistor currents up to 800µA may be programmed. This current limit corresponds to minimum resistor values shown in Table 4.

Resistor (minimum Ω)	Fault Timer Behavior	Constant Current Equation	Resistance Calculation (at nominal VREF = 5V)
R_{CH_CC} (≥1.25kΩ)	Sets a fixed charge current into capacitor C_{TIMER} and therefore sets a fixed time to power switch turn-off after an over-current fault	$I_{CH\_CC} = \frac{VREF}{5 \times R_{CH\_CC}}$ A	$R_{CH\_CC} = \frac{1}{I_{CH\_CC}}$ Ω
R_{CH_SOA} (≥7.5kΩ, V_{LINE}=120V) (≥3.25kΩ, V_{LINE}=52V)	Sets a variable charge current into capacitor C_{TIMER} proportional to power switch voltage drop. This emulates the power switch's safe operating area (SOA) for energy absorption	$I_{CH\_SOA} = \frac{V_{LINE} - V_{LOAD}}{20 \times R_{CH\_SOA}}$ A	
R_{DCH_CC} (≥1.25kΩ)	Sets a fixed discharge current of I_{DCH_CC}/10 from capacitor C_{TIMER} and therefore sets a fixed time after power switch turn-off before hiccup	$I_{DCH\_CC} = \frac{VREF}{5 \times R_{DCH\_CC}}$ A	$R_{DCH\_CC} = \frac{1}{I_{DCH\_CC}}$ Ω

Table 4. Fault Timer Charge/Discharge Equations

The final charging current for the fault timer capacitor is the sum of I_{CH_CC} and I_{CH_SOA}:

Equation 18. $I_{CHG} = I_{CH\_CC} + I_{CH\_SOA}$ A

The final discharging current for the fault timer capacitor is a tenth of I_{DCH_CC}:

Equation 19. $I_{DISCHG} = \frac{I_{DCH\_CC}}{10}$ A

16.1.1 EXAMPLE FIXED-FAULT TIMER COMPONENT DESIGN 1 (USING R_{CH_CC} AND R_{DCH_CC} ONLY)

Example specification: V_{LINE} = 22V to 38V, I_{LIM} = 5A, E_{LIM} = 2J, over-current fault dissipation recovery time = 300ms

To calculate the energy when R_{CH_CC} is the only setting for the fault timer, use the worst-case limit where there is the full V_{LINE} across the power switch during the fault:

Equation 20. $E_{LIM} = I_{LIM} \times V_{LINE} \times t = \left(I_{LIM} \times V_{LINE} \times C_{TIMER} \times 5 \times R_{CH\_CC}\right)$ J

since: $t = \dfrac{C_{TIMER} \times VREF}{I_{CH\_CC}} = \left(C_{TIMER} \times 5 \times R_{CH\_CC}\right)$ s

Rearranging Equation 20:

Equation 21. $C_{TIMER} = \dfrac{E_{LIM}}{I_{LIM} \times V_{LINE} \times 5 \times R_{CH\_CC}}$ F

The recommended range of values for R_{CH_CC} is 10kΩ to 100kΩ, so selecting the initial R_{CH_CC} = 22kΩ and putting the requirements into
Equation 21 to calculate C_{TIMER}:

$$C_{TIMER} = \left(\frac{2}{5 \times 38 \times 5 \times 22k}\right) = 96nF$$

Selecting 100nF as the nearest standard capacitor value, and recalculate R_{CH_CC} (if desired):

$$R_{CH\_CC} = \left(\frac{2}{5 \times 38 \times 5 \times 100n}\right) = 21.05k\Omega$$

The discharge current I_{DCH_CC} is calculated using the 300ms recovery time specified in the example, allowing R_{DCH_CC} to be determined. During this time, $I_{DISCHG} = I_{DSC\_CC}/10$ discharges C_{TIMER} from VREF to the VREF/5 trip point, which is a ΔV of 4/5ths VREF:

$$I_{DISCHG} = \frac{C_{TIMER} \times (0.8 \times VREF)}{t} = \frac{100n \times 4}{0.3} = 1.33\mu A$$

Therefore $R_{DCH\_CC} = \dfrac{1}{10 \times I_{DISCHG}} = \dfrac{1}{10 \times 1.33\mu} = 75k\Omega$

16.1.2 EXAMPLE SOA-FAULT TIMER COMPONENT DESIGN 2 (USING R_{CH_CC}, R_{CH_SOA} AND R_{DCH_CC})

Example specification: V_{LINE} = 22V to 38V, I_{LIM} = 5A, E_{LIM} = 2J, over-current fault dissipation recovery time = 2s

In this example, R_{CH_SOA} is used to adjust the timeout according to the real time voltage across power switch during the fault. However, we also use R_{CH_CC} to set a small fraction of the minimum timeout delay (5% to 10%) independently, to guarantee a reasonably short timeout in the event of a soft fault. A soft fault trips the over-current threshold but has sufficiently high resistance that the voltage drop across the power switch remains small when current limiting. If R_{CH_SOA} is used to adjust the timeout alone, then the timeout would be long in such a fault scenario with a low voltage drop across the power switch.

Since the capacitor C_{TIMER} will be charged simultaneously from two sources (I_{CH_SOA} and I_{CH_CC}), Equation 20 from the first example is rearranged to reflect the sum of these currents instead of a single resistor:

Equation 22. $E_{LIM} = I_{LIM} \times V_{LINE} \times t = \dfrac{I_{LIM} \times V_{LINE} \times C_{TIMER} \times 5}{I_{CH\_SOA} + I_{CH\_CC}}$ J

since: $t = \dfrac{C_{TIMER} \times VREF}{I_{CH\_SOA} + I_{CH\_CC}} = \dfrac{C_{TIMER} \times 5}{I_{CH\_SOA} + I_{CH\_CC}}$ s

Rearranging Equation 22:

Equation 23. $C_{TIMER} = \frac{E_{LIM} \times \left(I_{CH\_SOA} + I_{CH\_CC}\right)}{I_{LIM} \times V_{LINE} \times 5}$ F

Select 200µA current (split to 90% from I_{CH_SOA}, 10% from I_{CH_CC}) into C_{TIMER} at worst case dissipation point V_{LINE} = 38V and V_{LOAD} =0V. Putting our requirements into Equation 23 to calculate C_{TIMER}:

$$C_{TIMER} = \left(\frac{2 \times 200\mu}{5 \times 38 \times 5}\right) = 421nF$$

Selecting 470nF as the nearest standard capacitor value, and recalculating the charging current:

$$I_{CH\_SOA} + I_{CH\_CC} = \frac{C_{TIMER} \times I_{LIM} \times V_{LINE} \times 5}{E_{LIM}} = \frac{470n \times 5 \times 38 \times 5}{2} = 233\mu A$$

From this I_{CH_SOA} = 0.9 x 233µA = 210µA and I_{CH_CC} = 0.1 x 233µA = 23µA. Now R_{CH_CC} and R_{CH_SOA} can be calculated. R_{CH_SOA} is calculated at the worst-case limit where there is the full V_{LINE} across the power switch during the fault:

$$R_{CH\_CC} = \frac{1}{I_{CH\_CC}} = \frac{1}{23\mu} = 43.5k\Omega$$

$$R_{CH\_SOA} = \frac{V_{LINE} - V_{LOAD}}{20 \times I_{CH\_SOA}} = \frac{38 - 0}{20 \times 233\mu} = 8.15k\Omega$$

The shortest time from over-current fault to fault timer cutoff is when there is the full V_{LINE} across the power switch:

$$t = \frac{C_{TIMER} \times VREF}{I_{CH\_SOA} + I_{CH\_CC}} = \frac{470n \times 5}{233\mu} = 10.1ms$$

The longest time from over-current fault to fault timer cutoff is when there is essentially no voltage across the power switch:

$$t = \frac{C_{TIMER} \times VREF}{I_{CH\_CC}} = \frac{470n \times 5}{23\mu} = 102ms$$

The discharge current I_{DCH_CC} is calculated using the 2s recovery time specified in the example, allowing R_{DCH_CC} to be determined. During this time, I_{DCH_CC} discharges C_{TIMER} from VREF to the VREF/5 trip point, which is a ΔV of 4/5ths VREF:

$$I_{CH\_SOA} = \frac{C_{TIMER} \times (0.8 \times VREF)}{t} = \frac{0.47\mu \times 4}{2} = 0.94\mu A$$

Therefore: $R_{DCH\_CC} = \frac{1}{10 \times I_{DCH\_CC}} = \frac{1}{10 \times 0.94\mu} = 106.4k\Omega$

17 Power Switch Reverse Current Protection

The LX7712's power switch has a reverse body diode (Figure 12 on page 17) which provides a path from the LOAD output to the LINE input when the power switch is turned off. If LX7712s are used to hot-swap multiple supplies to a load, then an external reverse PFET can be added to each LX7712 to block the reverse path when the LX7712 is off.

The circuit (Figure 18 below) uses the STATUS output to automatically switch on and off an external PFET in reverse-series with the internal PMOS from LINE to LOAD. A signal NPN operates as a cascode level-shifter to derive the high-side gate drive.

When the LX7712 is powered up but in OFF or OFF_LP mode, Q1's integral body diode (shown in gray in Figure 18) provides the initial power path to the LX7712. When the LX7712 is put in ON mode, Q1 is initially off, and load current passed through Q1's body diode and the LX7712's internal power PFET to the load. As soon as the LOAD voltage has risen past the LOAD under-voltage threshold set at the UVLO pin (Figure 10 on page 16), the STATUS output goes active low and turns on Q1. On fault or OFF or OFF_LP mode, STATUS rises and Q1 is turned off.

In the example below, Vlogic = +5V, and $I_{cascode}$ is selected to be 0.5mA (¼ of the STATUS pin's 2mA rating). The pullup resistor R3 from STATUS to Vlogic achieves the logic high level for other circuits monitoring the STATUS output, and ensure that Q2 stays off despite up to 10µA leakage into the STATUS output when it is off and high impedance.

Equation 24. $$R2 = \frac{V_{LOGIC} - V_{BE} - V_{STATUS}}{I_{cascode}} = \frac{5 - 0.65 - 0.25}{0.5mA} = 8.2k\Omega$$

Q2 is operating as a constant current sink, so ignoring base current $I_{R1} = I_{R2} = I_{cascode}$, which is 0.5mA in the example. Setting R1 = 22kΩ defines the nominal gate drive for Q1 at 11V.

The LINE input voltage can be regulated or unregulated since Q1's gate drive is from a constant current sink. However, the LINE input voltage must be above $V_{LOGIC} + (R1 \times I_{cascode}) + 1V = 5V + 11V + 1V = 17V$, where the 1V is a nominal minimum voltage across Q2. Allowing for tolerances, this example is suitable for a LINE voltage of 20V minimum.

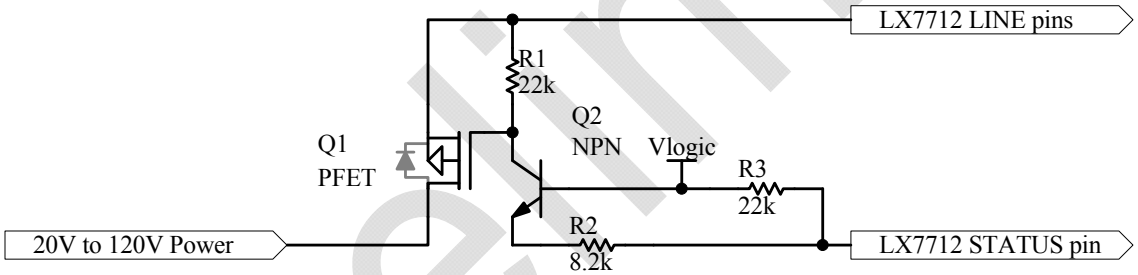
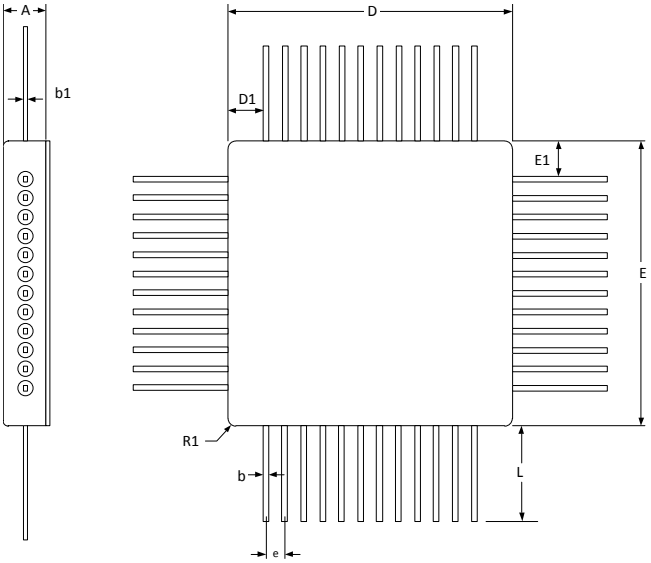


Figure 18. Adding a Back-to-Back PFET for Reverse Current Protection

18 HTF-48 (Hybrid Tub Flatpack) Dimensions



Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	3.05	3.30	0.120	0.130
b	0.305	0.457	0.012	0.018
b1	0.203	0.305	0.008	0.012
D	18.92	19.18	0.745	0.755
D1	2.29	2.41	0.090	0.095
E	18.92	19.18	0.745	0.755
E1	2.29	2.41	0.090	0.095
e	1.27 BSC		0.050 BSC	
R1	0.051	0.076	0.020	0.030
L	13.2 typical		0.52 typical	

Figure 19. 48-Lead Metal HTF Package Dimensions

Note:
1. Controlling dimensions are in inches. Metric equivalents are shown for general information
2. Parts are shipped with unformed leads
3. Package mass is 5g typical with shipped lead length
4. Package body is Kovar iron-nickel-cobalt alloy to ASTM F15 standard
5. Lead and lid material are Kovar with NiAu plating (nickel under-plate followed by gold plating)
6. The lid is stepped with a seam seal
7. Pin 18 is directly connected to the metal package body and wire bonded to the die. Pin 18, the GND pin 19, and the four FW_GND pins 41, 42, 43, and 44 must be connected to the same ground potential
8. The metal package top is electrically conductive to the metal package body, and so is at ground potential (GND)
9. Use the base of the package as the surface for conducting heat from the package

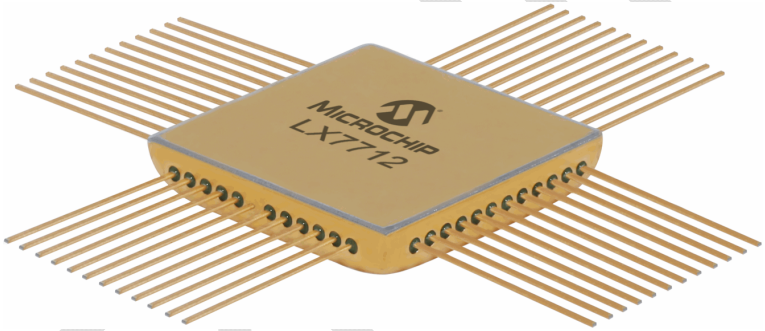


Figure 20. Package as shipped with untrimmed and unformed leads (showing pin 18 directly connected to body)

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20 Revision History

20.1 Revision 0.2 - January 2021

Pre-release. Changes not logged.

20.2 Revision 1 - xxx 2021

First release.

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