

Libero SoC v11.9 SP3

Release Notes

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.0

Revision 1.0 is the first publication of this document.

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1 Libero SoC v11.9 SP3 Release Notes

The Libero® system on chip (SoC) v11.9 SP3 is a service pack release of the Libero SoC v11.9 software for designing with Microsemi's power efficient flash [FPGAs](#), [SoC FPGAs](#), and [rad-tolerant FPGAs](#). The suite integrates industry standard Synopsys [Synplify Pro](#)® synthesis and Mentor Graphics [ModelSim](#)® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v11.9 SP3 for designing with Microsemi's [RTG4](#) Rad-Tolerant FPGAs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. [Development Kits & Boards](#) are listed in the **Design Resources** tab.

2 What's New in Libero SoC v11.9 SP3

Libero SoC v11.9 SP3 includes the following updates.

2.1 RTG4: Dynamic on-die termination (ODT) Access per I/O Bank

RTG4 production devices support the Dynamic ODT I/O attribute setting. Libero SoC v11.9 SP3 provides the RTG4_ODT_DYNAMIC core that can be instantiated for each I/O bank requiring dynamic ODT control.

The RTG4_ODT_DYNAMIC core grants access to the I/O bank-level dynamic on-die termination (ODT) control signal, and provides a single, active-low input signal, An . When An is '0', it enables the Dynamic ODT setting for the selected I/O bank and specifically any user I/Os configured to use dynamic ODT. Any I/O within the bank with I/O attributes set to ODT_STATIC = OFF and ODT_DYNAMIC = ON will have the ODT resistor turned on (An = '0') or off (An = '1') dynamically during design operation. The ODT value will match the selected value in the I/O Editor, if the I/O standard supports configurable ODT values, or default to the only supported value for I/O standards supporting a single ODT value. I/Os within the bank which are configured with ODT_DYNAMIC = OFF will not be affected by the value of input An .

Dynamic ODT supports the following I/O standards:

- LVDS, RSDS, MINILVDS, LVPECL, HSTLI, HSTLII, SSTL15I, SSTL15II, SSTL18I, SSTL18II, HSTL18I, HSTL18II, LPDDR1, LPDDR2

Note: The DDRIO banks can support this feature, but not when the FDDR controller is instantiated on the same bank. FDDR controller PHY takes priority over the An fabric input to the Dynamic ODT core.

For more information, see the following documents:

- [RTG4 Macro Library Guide](#)
- [PDC Commands User Guide](#)

2.2 RTG4: Weak Pullup/pulldown Resistor for Differential Inputs

Libero SoC v11.9 SP3 enables optional weak pullup/pulldown resistor attributes on input I/Os for the following differential I/O standards in RTG4 designs.

- LVDS, RSDS, MINILVDS, LVPECL

Note: When the weak pullup resistor I/O attribute is applied to PADP of a differential I/O, the I/O Editor shows pullup for both PADP and PADN, but PADN will be correctly pulled down.

2.3 RTG4: LVDS Fail-safe Solution

Libero SoC v11.9 SP3 enables RTG4 designs to create an internal LVDS fail-safe solution. This configuration uses a combination of the above new features:

- Dynamic on-die-termination (ODT) access per I/O bank
- Weak pullup/pulldown Resistor for differential inputs

When the LVDS input temporarily floats during operation, there is a new bank-level input signal that can dynamically turn off the on-die termination resistor so that each leg of the LVDS pair will only see the weak pullup and pulldown resistor enabled, creating an LVDS fail-safe input.

The RTG4_ODT_Dynamic core should be instantiated for each bank which requires any LVDS fail-safe I/O. The LVDS inputs which could float need to "subscribe" in the I/O Editor to join the group of inputs

affected by the RTG4_ODT_Dynamic core input for the I/O bank selected. Enable the weak pullup resistor I/O attribute on PADP of the LVDS I/O. PADN will be weakly pulled down automatically. During normal operation, the internal ODT should be present for the LVDS receiver. During fail-safe, drive $An = '1'$ to disable ODT.

For more information, see the following document:

- [UG0741: RTG4 FPGA I/O User Guide](#)

2.4 RTG4: LSRAM BLK Select Deassertion Circuit for Pipelined ECC

The RTG4 Two-Port and Dual-Port LSRAM configurators in Libero SoC v11.9 SP3 have been updated to generate an additional circuit for the pipelined-ECC mode.

- This change only applies to pipelined-ECC LSRAM components generated from the IP catalog. Manually instantiated LSRAM instances will need to migrate to the respective configurator.
- The additional circuit avoids a hold time issue by delaying BLK select de-assertion to each LSRAM block.
- Note: Single-depth Dual-port LSRAM which uses the BLK select input will no longer hold the most recent Read-data after de-asserting REN. Read-data output is gated by the pipelined BLK select input, and thus Read-data will output zero after the valid read.

To insert the additional circuit, existing designs must update to Libero SoC v11.9 SP3 and regenerate any LSRAM components with pipelined-ECC mode.

- Existing designs opened in Libero SoC v11.9 SP3 will be invalidated if it contains any pipelined-ECC LSRAM component and you will be asked to regenerate the affected LSRAMs.
- Compile will generate an error if pipelined-ECC LSRAM catalog components still require regeneration.
- You must rerun Static Timing Analysis to check whether the updated LSRAM component with the additional circuit still meets timing requirements.

2.5 SmartFusion2, IGLOO2, RTG4: Double accounting of clock latency when applied to generated clocks

When a clock latency constraint is set on a generated clock, the Static Timing Analyzer uses the late clock latency (and respectively early clock latency) value in the calculation of the data arrival time (and respectively the data required time). However, due to an error introduced in Libero SoC v11.7.SP1, an additional delay (equal to late - early) is incorrectly added to the clock net driven by the clock source in the required time calculation.

This issue is fixed in the Libero SoC v11.9 SP3 release.

3 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC v11.9 SP3. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

3.1 List of Resolved Issues

Case Number	Description
493642-2559621344	RTG4: Two Port Memory ECC Error Flags going 'X' in x36 mode
493642-2544434392	RTG4: Creation of unnecessary CDC due to derived constraints for CCC
	RTG4: LSRAM pre-synth simulation does not match correct LSRAM behavior
	RTG4: Improve placer messaging when GB0 error occurs
	RTG4: Global SET setting overrides ndc file
	Unable to open documentation for serial interfaces

4 Known Limitations, Issues and Workarounds

Known issues from Libero SoC v11.9 also apply to Libero SoC v11.9 SP3. Review the [Libero SoC v11.9 Release Notes](#) for Known Issues in Libero SoC v11.9.

4.1 RTG4 CCC: Extra ports exposed when PLL is bypassed

The RTG4 CCC configurator will expose extra ports when the FBCLK option is “PLL Internal”, but a GL multiplexor bypasses the PLL and selects one of the following sources:

- Dedicated Input
- Fabric Input
- Clock recovery Circuitry
- Oscillators

Workaround: Make sure that the FBCLK option is “CCC Internal” (the default) before selecting the GL multiplexor source. This issue will be fixed in Libero SoC v12.1.

4.2 VHDL RAM: Spurious message about generic ramindex

When the HDL files generated by Libero SoC is VHDL and the design contains any RAM component, messages like the following are issued before invoking the Synthesis tool.

- Error: binding entity \RAM1K18\ does not have generic ramindex (VHDL-1323)

Workaround: Ignore the spurious messages. This issue will be fixed in Libero SoC v12.1.

4.3 SmartTime reports False Failure during max/best or min/worst case analysis

Timing reports may have incorrect slacks for the secondary corners “max/best” and “min/worst” if they were created with the constraint coverage option turned on. The reports for “max/worst” and “min/best” corners are not affected.

Workaround:

1. First, enable the constraint coverage option before running Verify Timing to generate and analyze the coverage report (but disregard the timing reports for “max/best” and “min/worst”). Then, disable the constraint coverage option before re-running Verify Timing to generate and analyze the timing reports at all corners, including “max/best” and “min/worst”.
2. Upgrade to Libero SoC v12.0, where this issue has been fixed.

5 System Requirements

For information about operating system support and minimum system requirements, see the [System Requirements](#) web page.

For Linux OS setup instructions, see [How to Set Up Linux Environment for Libero User Guide:](#)

5.1 Operating System Support

Supported

- Windows 7, Windows 8.1, Windows 10
- RHEL 5*, RHEL 6, RHEL 7, CentOS 5*, CentOS 6, and CentOS 7
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: * RHEL 5 and CentOS 5 do not support programming using FlashPro5.

Not Supported

- 32-bit operating systems
- Windows XP
- Support for the following operating systems will cease with the next major Libero SoC release. For more information, refer to [PCN17031](#).
 - RedHat Enterprise Linux 5.x through 6.5
 - CentOS 5.x through 6.5

6 Libero SoC v11.9 SP3 Download

Click the following links to download Libero SoC v11.9 SP3 on Windows and Linux operating systems:

- [Windows Download](#)
- [Linux Download](#)
- [Mega Vault Download](#)

Note: Libero SoC v11.9 SP3 includes the following new core:

Core	Libero SoC v11.9 SP3 version	Description
RTG4_ODT_DYN	1.0.101	Grants access to the I/O bank-level dynamic on-die termination (ODT) control signal

Note: Installation requires administrator privileges to the system.

Libero SoC v11.9 SP3 is an incremental service pack and can be installed over Libero SoC v11.9, or over Libero SoC v11.9 SP1 or Libero SoC v11.9 SP2.

After successful installation, clicking **Help-> About Libero** will show Version: 11.9.3.5.

6.1 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.9 SP2 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.x

- [SoftConsole Download](#)