AC485
Application Note
PolarFire FPGA Low Power

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 3.0

Added Appendix 4: Running the TCL Script, page 25.

1.2 Revision 2.0

The following is a summary of the changes made in this revision.

- Updated the document for Libero SoC v12.2.
- Removed the references to Libero version numbers.

1.3 Revision 1.0

The first publication of this document. This documents replaces *PolarFire Low Power User Guide* and *PolarFire Low Power Demo Guide* documents.

2 PolarFire FPGA Low-Power

Microsemi PolarFire® FPGAs are designed to meet the demand for low-power applications. PolarFire devices exhibit lower-power consumption in static and dynamic modes. PolarFire devices offer several low-power features for the FPGA fabric, Fabric Clock Conditioning Circuitry (CCC), Transceiver, PCIe, DDR memory, and other hard and soft IP blocks. This application note provides an overview of low power advantages of PolarFire devices and techniques for low power design implementation using PolarFire.

2.1 Lower Power Options

The following low-power options are available in PolarFire devices:

- Transceiver Low-Power Options, page 2
- PCIe Low-Power Option, page 3
- DDR Controller Low-Power Option, page 3
- PLL Low-Power Option, page 4
- RAM Blocks Low-Power Option, page 4

2.1.1 Transceiver Low-Power Options

The Transceiver Quad and External PLLs have several registers that power down different parts of the circuitry. This allows enabling only those circuits that are used in the design to reduce the transceiver power.

The following table lists the registers that are required to disable parts of the Transceiver Quad circuitry and external PLL circuitry.

Table 1 • **Transceiver Quad Circuitry**

Name of Register	Field Name	Value for Low power	Description
DES_RSTPD	RXPD	1	Power down the Rx circuitry
	PDDFE	1	Power down the DFE circuit
	PDEM	1	Power down the Eye Monitor circuit
	RCVEN	1	Disable Rx receiver
DES_PKDET	RXPKDETEN	0	Disable the Rx peak detector
DES_IN_TERM	RXTEN	0	Disable Rx termination resistor
DES_RXPLL_DIV	CDR_GAIN	0	Set CDR Gain to 0
DES_DFE_CAL_CTRL_0	EN_OFFSET_CAL	0	Disable offset calibration
SER_RSTPD	TXPD	1	Power down the TX circuitry
SER_TERM_CTRL	TXTEN	0	Disable the Tx termination resistor
SERDES_RTT	RTT_CURRENT_PROG	0	Disable RTT trim circuit
TXPLL_CTRL	TXPLL_AUXDIVPD	1	Disable the Aux clock output
	TXPLL_VBGREF_SEL	0	Disable the Tx voltage regulator
	TXPLL_PD	1	Disable TX PLL

Table 1 • **Transceiver Quad Circuitry**

Name of Register	Field Name	Value for Low power	Description
TXPLL_CLKBUF	TXPLL_DUALCLK1_MODE	0	Disable the refclkp input buffer
	TXPLL_DUALCLK0_MODE	0	Disable the refclkn input buffer
	TXPLL_DUALCLK1_ENTERM	0	Disable the refclkp input buffer single ended termination
	TXPLL_DUALCLK0_ENTERM	0	Disable the refclkn input buffer single ended termination
	EXTPLL_CLKBUF_EN_RDIFF	0	Disable 100 ohm differential termination between refclkp and refclkn

Table 2 • **External PLL Circuitry**

Name of Register	Field Name	Value for Low Power	Description
EXTPLL_CTRL	EXTPLL_PD	1	Power down the External PLL
	EXTPLL_VBGREF_SEL	0	Disable the Tx voltage regulator
EXTPLL_CLKBUF	EXTPLL_DUALCLK1_MODE	0	Disable the refclkp input buffer
	EXTPLL_DUALCLK0_MODE	0	Disable the refclkn input buffer
	EXTPLL_DUALCLK1_ENTERM	0	Disable the refclkp input buffer single ended termination
	EXTPLL_DUALCLK0_ENTERM	0	Disable the refclkn input buffer single ended termination
	EXTPLL_CLKBUF_EN_APAD	0	Disable analog connection to refclkn pad
	EXTPLL_CLKBUF_EN_RDIFF	0	Disable 100 ohm differential termination between refclkp and refclkn

Note: For more information about register configuration, see *AC475: PolarFire FPGA Dynamic Reconfiguration* Interface and *PolarFire Device Register Map.*

2.1.2 PCIe Low-Power Option

The PolarFire PCIESS supports PCIe low-power operation states known as L2 and P2 states. The PCIe hot reset and L2 and P2 compatibility settings can be selected when customizing the PCIESS design. L2 states are available in both root port and endpoint configurations. For more information about PCIe Low-Power Option, see *UG0685: PolarFire FPGA PCI Express User Guide*.

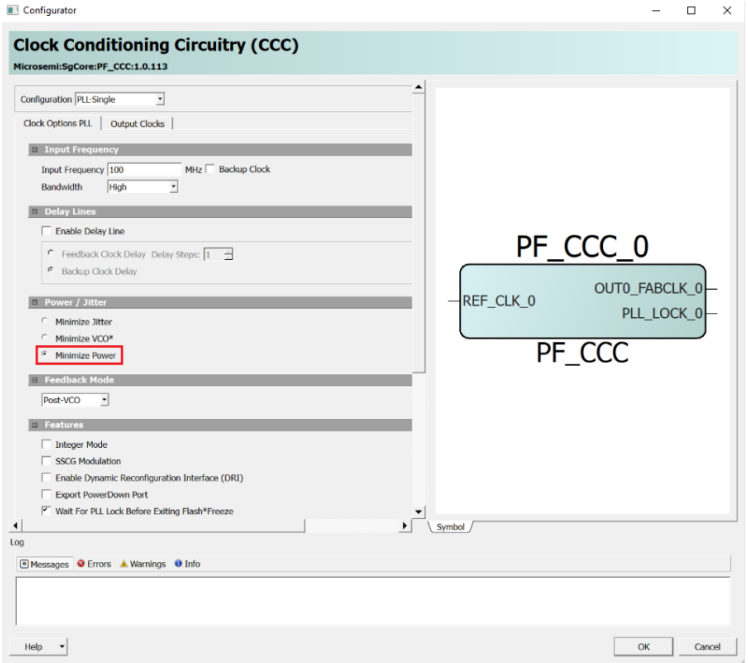
2.1.3 DDR Controller Low-Power Option

The PolarFire FPGA DDR subsystem supports low-power operating option which puts the DDR memory in low-power option and issues refresh commands automatically to retain data. For more information about DDR low-power options, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

2.1.4 PLL Low-Power Option

PLL can be set to Low Power option by selecting **Minimize Power**, as shown in the following figure.

Figure 1 • **Setting to Minimize Power in CCC Configurator**



2.1.5 RAM Blocks Low-Power Option

The dual-port LSRAM, two-port LSRAM, and micro SRAM can also be set for minimum power consumption. The following figures show how the dual-port LSRAM, two-port LSRAM, and micro SRAM are set to low power.

Figure 2 • **Low-Power Setting for Dual-Port LSRAM**

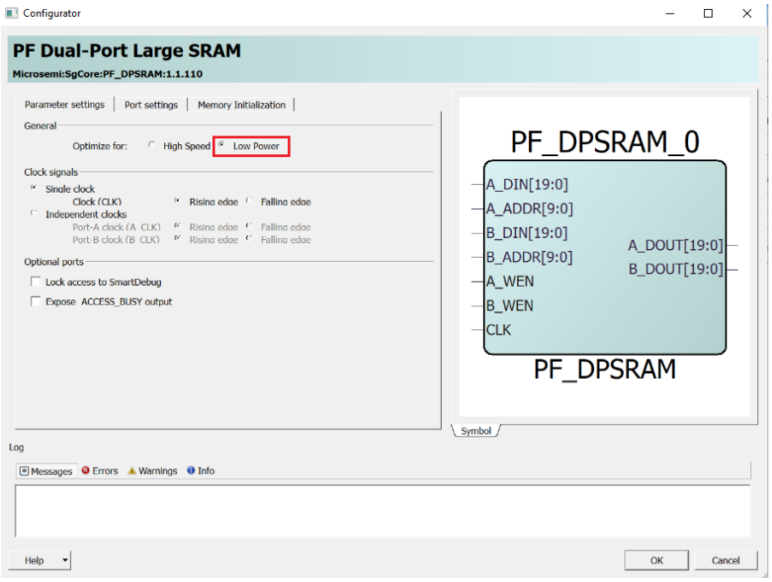


Figure 3 • **Low-Power Setting for Two-Port LSRAM**

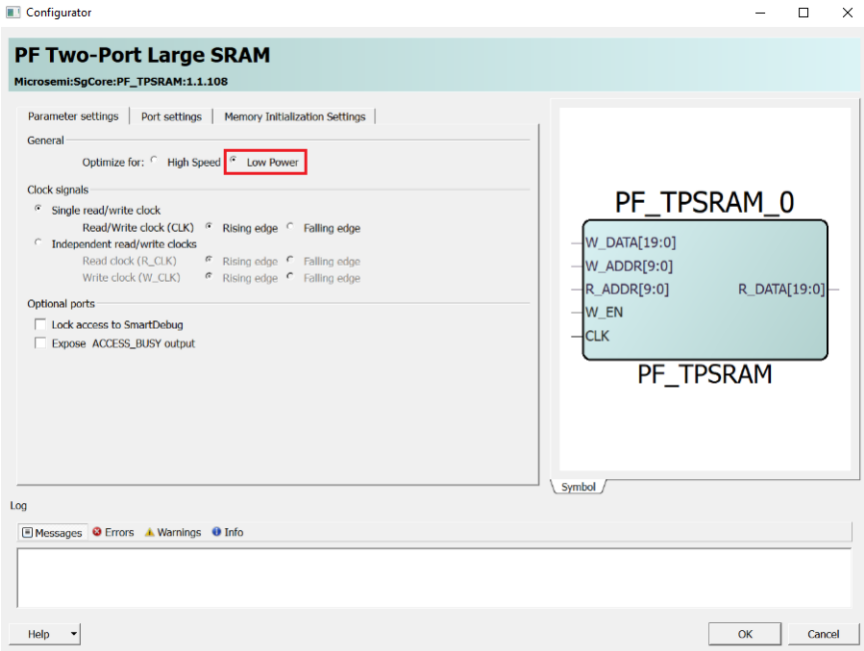
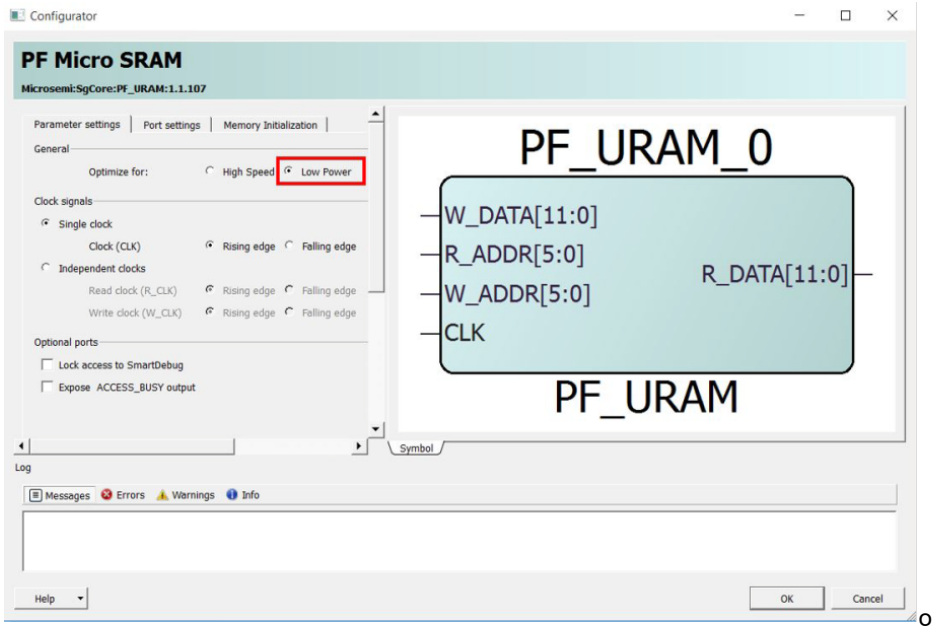


Figure 4 • **Low-Power Setting for Micro SRAM**



2.2 Design Requirements

The following table lists the hardware and software requirements to run the demo.

Table 3 • **Design Requirements**

Requirement	Version
Hardware	
MPF300T-EVAL-KIT	Rev D or later
Host PC	Windows 7, 8.1, or 10
Software	
Libero SoC	**Note:** Refer to the readme.txt file provided in the design files for the software versions used with this reference design.
FlashPro Express	

Note: Libero SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

2.3 Prerequisites

Before you begin:

1. For demo design files download link:
   http://soc.microsemi.com/download/rsc/?f=mpf_ac485_df
2. Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location.
   https://www.microsemi.com/product-directory/design-resources/1750-libero-soc

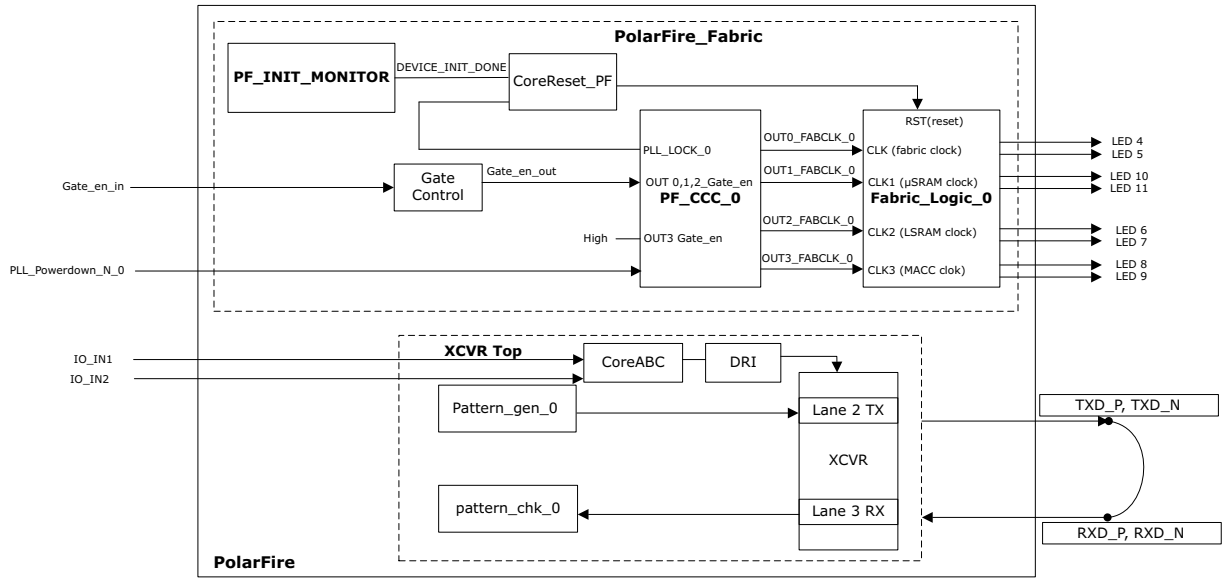
Note: The latest versions of ModelSim and Synplify Pro are included in the Libero SoC installation package.

3. Download the Microsemi PowerMonitor application from the following location:
   http://soc.microsemi.com/download/rsc/?f=polarfire_power_monitor

2.4 Demo Design

The block diagram of the low-power design is illustrated in the following figure.

Figure 5 • **Block Diagram**



The PolarFire_Fabric block instantiates a counter logic along with 500 µSRAM, 500 LSRAM, and 500 Mathblocks, which utilizes 70% of 4 input LUT and DFF.

In the XCVR_Top SmartDesign, transceiver block is instantiated and loop backed internally on PolarFire Evaluation kit from Lane 2 to Lane 3. The Core ABC and DRI block enables the user to Dynamically reconfigure the XCVR registers.

The demo design flow is described as follows:

- The DEVICE_INIT_DONE signal of the PF_INIT_MONITOR block is asserted after the device is initialized.
- CoreReset_PF IP core is used to control reset signal of the Fabric_Logic_0 and XCVR_Top block.
- The PF_CCC_0 block provides the following fabric clocks:
  - CLK: 100 MHz clock for the fabric
  - CLK1: 100 MHz clock for the µSRAM blocks
  - CLK2: 100 MHz clock for the LSRAM blocks
  - CLK3: 100 MHz clock for Mathblocks
- These separate clocks are provided in the design, to gate clocks to each fabric block if required. The transceiver (PF_XVCR) block instantiates the transceiver in 8b10b mode. This block receives clock from the REF_CLK signal of PF_XCVR_REF_CLK_0. The PF_TX_PLL_0 block also derives its reference clock from REF_CLK of PF_XCVR_REF_CLK_0.
- PLL_Powerdown port is used to enable the PLL Powerdown option.
- Gate_en_in signal is fed to Gate Control block and output of the Gate Control Block is connected to OUT0,1, 2_FABCLK_GATED_0_EN.
- OUT3_FABCLK_GATED_0_EN is connected High.
- The TX and RX lanes of the transceiver are looped back using on board PCB loop back.
- The pattern_gen_0 block is implemented to send data to the transceiver block. The pattern_chk_0 block is implemented to check errors in the data received by the transceiver block.
- DRI interface is used to configure the XCVR/TX_PLL in ON and OFF mode.

There are two programming job files provided with this demo.

- Without using low power options (`PF_Demo_Normal.job`) and
- With low power options (`PF_Demo_Low_power.job`).

2.4.1 Low Power Option

This section describes the different low power options used in the demo design.

2.4.1.1 PLL Power Down

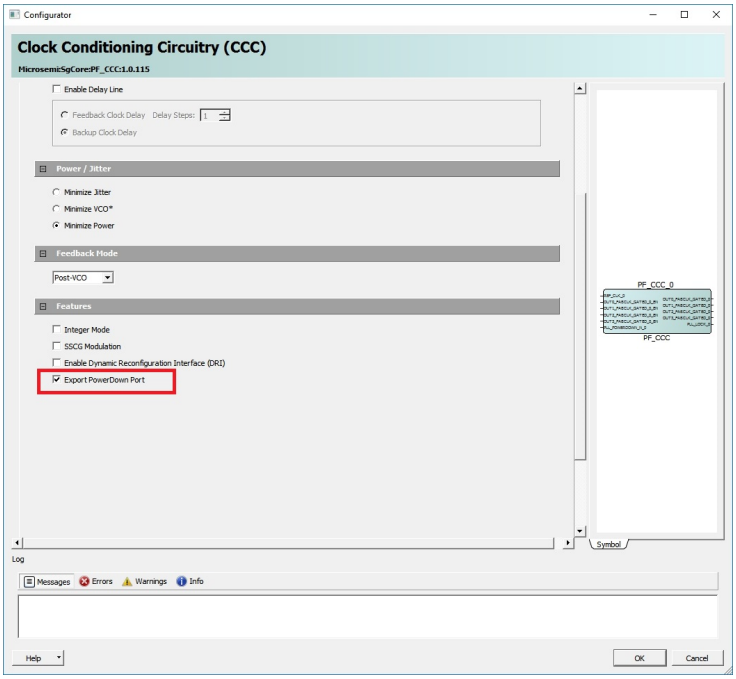
The active-low power-down input (PLL_POWERDOWN_N) can be exposed using CCC configurator. The PLL_POWERDOWN_N is an asynchronous signal, which can be used to reset the PLL from the FPGA fabric, which forces the PLL to its lowest power state and the clock outputs are driven low.

In the design, this port is exposed and connected to DIP1 switch.

- DIP1-0: Power Down Mode
- DIP1-1: Normal Mode

The following figure shows the PF_CCC configurator settings for the demo design.

Figure 6 • **PLL Power Down—CCC Configurator Setting**



2.4.1.2 Clock Gating

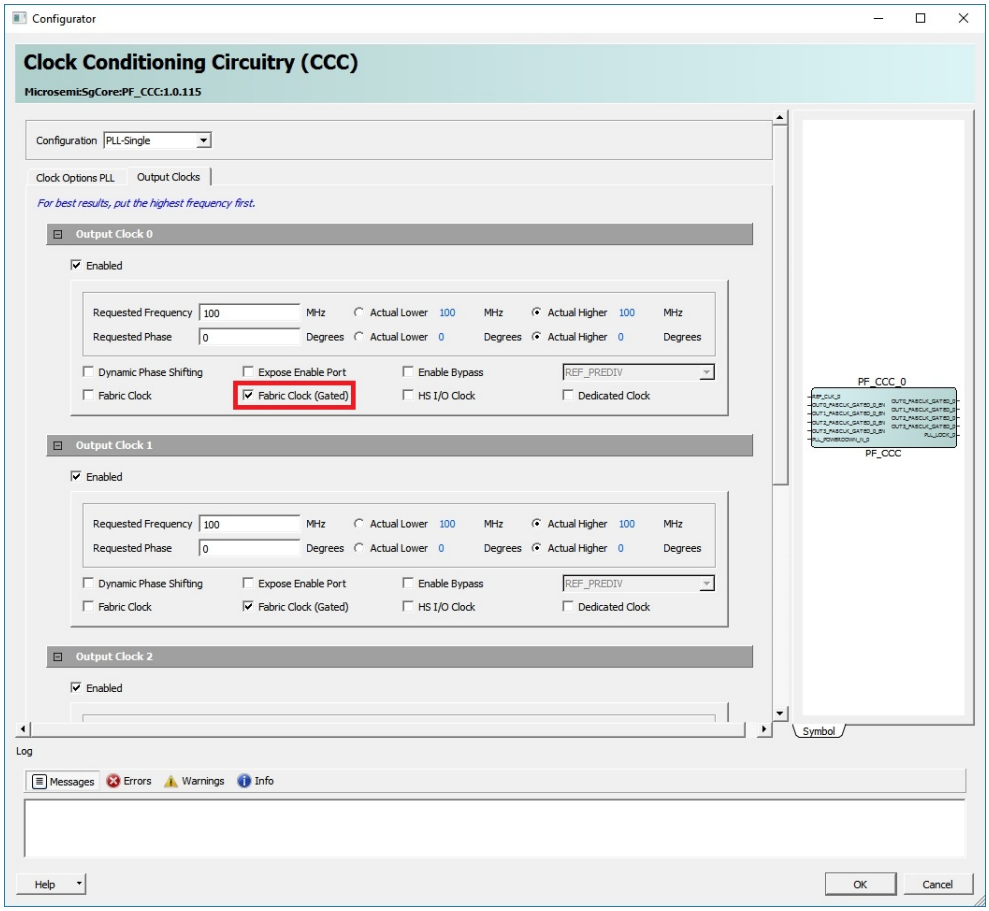
Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Gate enable/disable pins can be exposed by using CCC configurator.

The Design has a clock gating enable /disable switch which is connected to DIP2 for OUTPUT0,1, and 2.

- DIP2-1: Clock Gating Enabled (Clock is available)
- DIP2-0: Clock Gating Disabled (Clock is not available)

The following figure shows the PF_CCC configurator settings for the demo design.

Figure 7 • **Clock Gating—CCC Configurator Settings**

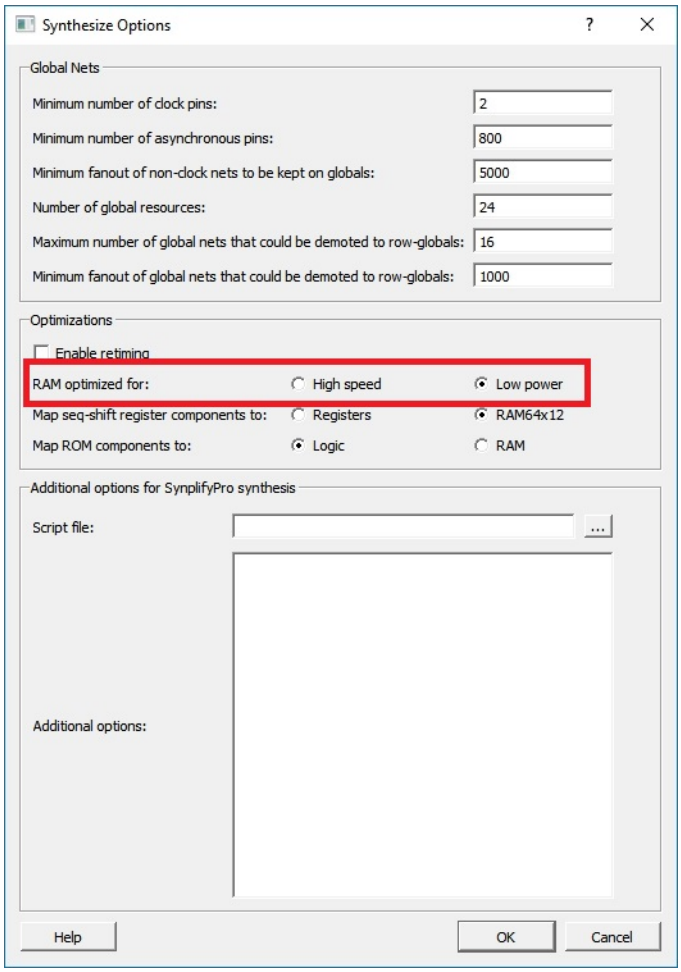


2.4.1.3 Synthesize and, Place and Route

In Libero, Synthesize has RAM optimization option. RAMs can be optimized for the following two modes.

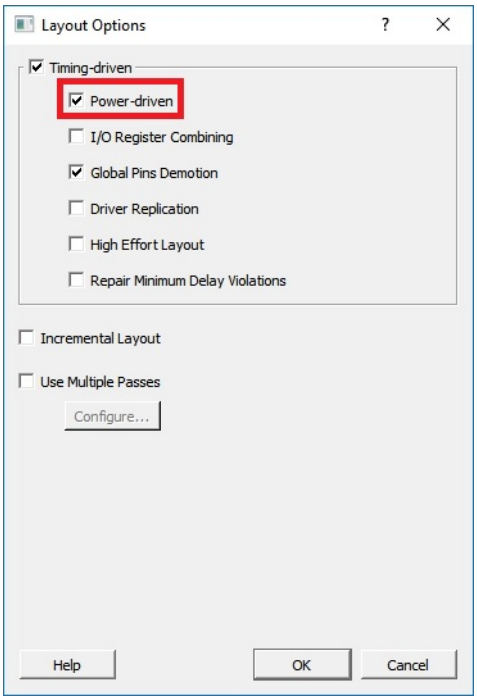
- **High speed** - RAM Optimization is geared towards Speed. The resulting synthesized design achieves better performance (higher speed) at the expense of more FPGA resources.
- **Low power** - RAM Optimization is geared towards Low Power. RAMs are inferred and configured to ensure the lowest power consumption.

Figure 8 • **Synthesize Options**



In Libero, the Place and Route has Power-driven option. Enable this option to run Power-Driven layout. The primary goal of Power-driven layout is to reduce dynamic power while still maintaining timing constraints.

Figure 9 • **Layout Options**



2.4.1.4 Transceiver

In this design, Transceiver can be dynamically switch ON and OFF using DRI interface. DIP-3 and DIP-4 switches are connected to Inputs of CoreABC(IN_IN_0 and I0_IN_1). Based on selection, XCVR related register dynamically reconfigures.

Table 4 • **Power Down/Up XCVR**

Mode	DIP4	DIP3
XCVR OFF	0	1
XCVR ON	1	0

The following figure shows the XCVR register setting for XCVR OFF mode.

Figure 10 • **Transceiver OFF—Register Setting**

```
//-------------------------------------------xcvr off and txpll off
$xcvr_off_txpll_off
// Assert PMA  Reset
    IOWRT 0x011
//SER_RSTPD
    APBWRT DAT 0 0x4078 0x00000007
    APBWRT DAT 0 0x8078 0x00000007
//DES_RSTPD
    APBWRT DAT 0 0x404C 0x0000002F
    APBWRT DAT 0 0x804C 0x0000002F

//LSRT Assert and deassert on Q2_lane2 and Q2_lane3
    IOWRT 0x001
    APBWRT DAT 0 0x4068 0x00000D0D
    APBWRT DAT 0 0x8068 0x00000D0D

//TX PLL Powerdown
    IOWRT 0x011
    APBWRT DAT 1 0x0008 0x0820010
    JUMP $done
```

The following figure shows the XCVR register setting for XCVR ON mode.

Figure 11 • **Transceiver ON Mode Register Setting**

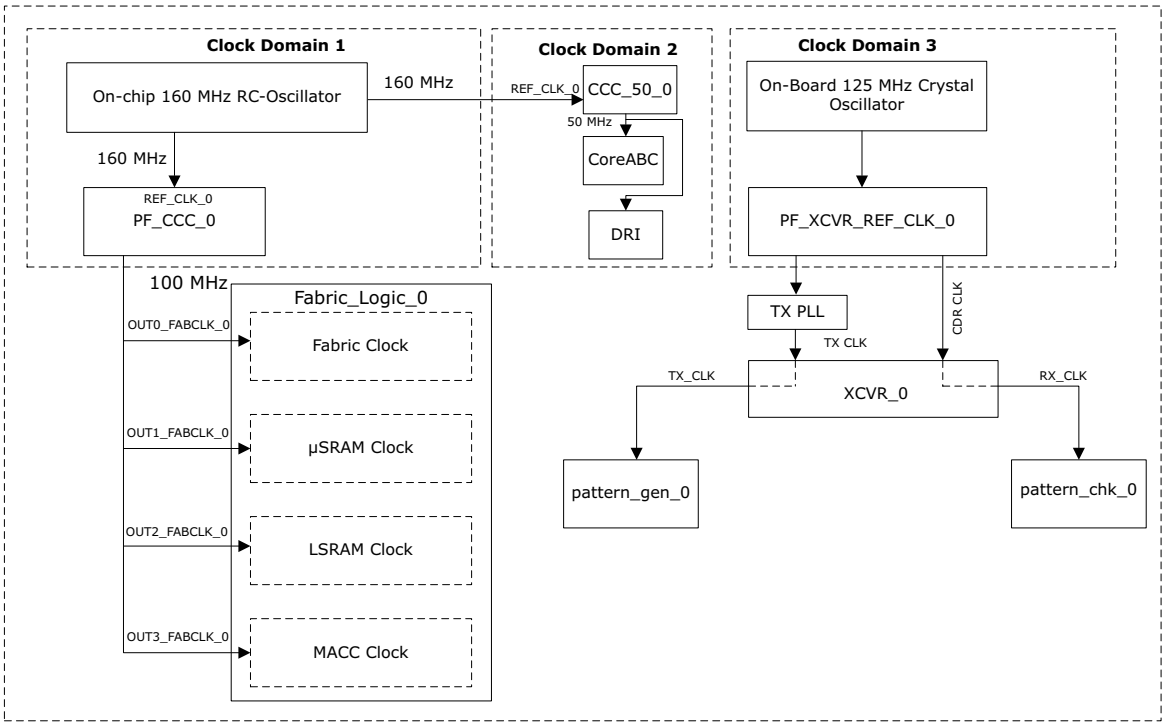
```
//-------------------------------------------xcvr on and txpll on
$xcvr_on_txpll_on
// Assert PMA  Reset
    IOWRT 0x011
//SER_RSTPD
    APBWRT DAT 0 0x4078 0x00000003
    APBWRT DAT 0 0x8078 0x00000003
//DES_RSTPD
    APBWRT DAT 0 0x404C 0x00000032
    APBWRT DAT 0 0x804C 0x00000032
//  Power up XCVR and deassert PMA reset
//SER_RSTPD
    APBWRT DAT 0 0x4078 0x00000001
    APBWRT DAT 0 0x8078 0x00000001
//DES_RSTPD
    APBWRT DAT 0 0x404C 0x0000003C
    APBWRT DAT 0 0x804C 0x0000003C
//LSRT Assert and deassert on Q2_lane2 and Q2_lane3
    IOWRT 0x001
    APBWRT DAT 0 0x4068 0x00000D0D
    APBWRT DAT 0 0x8068 0x00000D0D
    APBWRT DAT 0 0x4068 0x00000404
    APBWRT DAT 0 0x8068 0x00000404
//TX PLL Power on
    IOWRT 0x011
    APBWRT DAT 1 0x0008 0x1800010
    JUMP $done
```

Note: For more information about register configuration, see *AC475: PolarFire FPGA Dynamic Reconfiguration Interface* and *PolarFire Device Register Map*

2.5 Clocking Structure

The following figure shows the clocking structure implemented in the demo design.

Figure 12 • **Clocking Structure**



2.6 Resource Utilization

The following tables list the resource utilization of the low power and normal demo designs after synthesis and place & route. These values may vary slightly for different Libero runs, settings, and seed values.

Table 5 • **Resource Utilization for Low power Demo**

Type	Used	Total	Percentage
4LUT	186382	299544	62.22
DFF	180140	299544	60.14
I/O Register	0	510	0.00
Logic Element	189750	299544	63.35

Table 6 • **Resource Utilization for Normal Demo**

Type	Used	Total	Percentage
4LUT	186182	299544	62.16
DFF	198484	299544	66.26
I/O Register	0	510	0.00
Logic Element	208219	299544	69.51

3 Running the Demo

Prerequisites for the procedure:

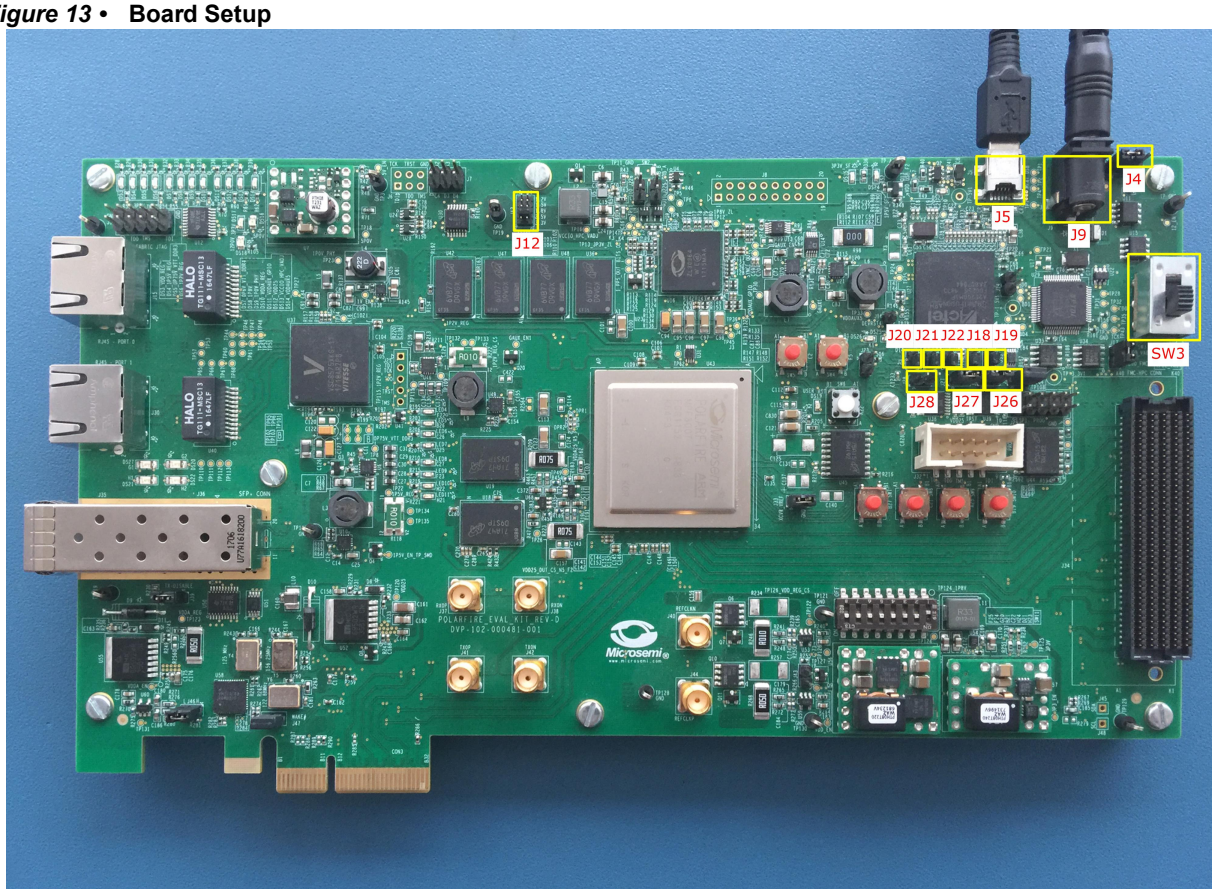
1. On the host PC, download and install the Microsemi PowerMonitor application from the following location:
   http://soc.microsemi.com/download/rsc/?f=polarfire_power_monitor
2. Ensure that the jumper settings on the board are same as listed in the following table

Table 7 • **Jumper Setting**

Jumper	Description
J18, J19, J20,J21, and J22	Close Pins 2 and 3 for Programming PolarFire FPGA through FTDI
J28	Close Pins 1 and 2 for programming through the On board FlashPro5
J4	Close Pins 1 and 2 for manual power switching using switch SW3
J12	Close Pins 3 and 4 for 2.5V

3. Connect the power supply cable to the **J9** connector on the board.
4. Connect the USB cable from the Host PC to the **J5** (FTDI port) on the board.
5. Power on the board using the **SW3** slide switch.

Figure 13 • **Board Setup**



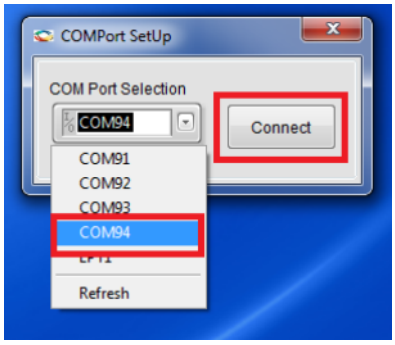
To run the demo, perform the following steps:

1. Ensure **DIP-3** and **DIP-4** are **ON** and **DIP-1** and **DIP-2** are **OFF**.

Note: In Evaluation kit DIP switches are Active Low.

2. To Program the Design without Low power options (`PF_Demo_Normal.job`) using FlashPro Express, see Appendix 1: Programming the Device Using FlashPro Express, page 19.
3. The LEDs {4, 5}, {6, 7}, {8, 9}, and {10,11} blink at different rates. This indicates that the fabric components are in active mode.
4. On the host PC desktop, click **Start** and then select **PowerMonitor**.
5. In the **COMPort** SetUp dialog box, select the highest COM port from the drop-down and click Connect as shown in the following figure.

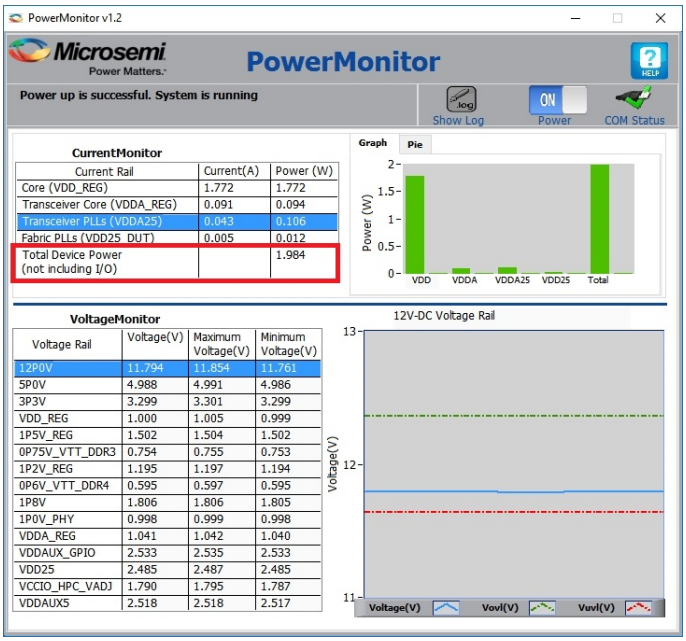
Figure 14 • **COM Port Setup**



The PowerMonitor application successfully connects to the board and starts displaying the Core Fabric (VDD) power, Fabric PLL (VDD25) power, Transceiver Core (VDDA) power, and Transceiver PLL (VDDA25) power

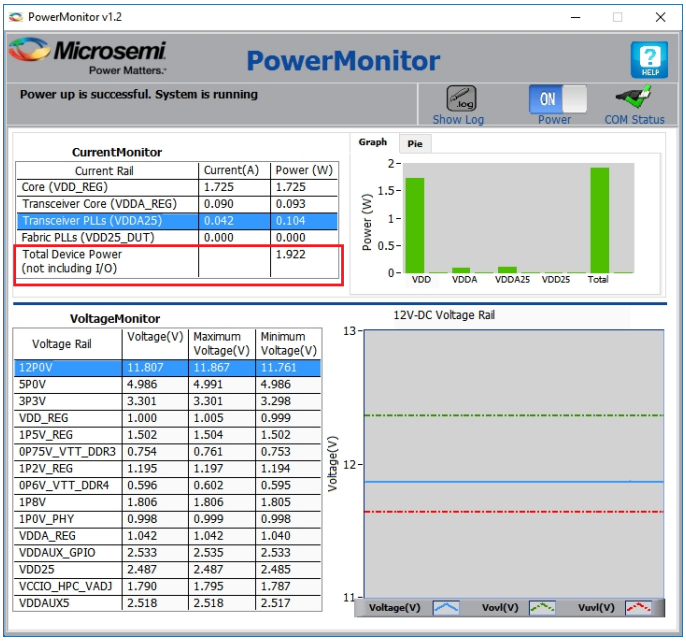
6. The total power consumed by the device is displayed in the Power Monitor GUI, as shown in the following figure.

Figure 15 • **Total Power—PF_Demo_Normal**



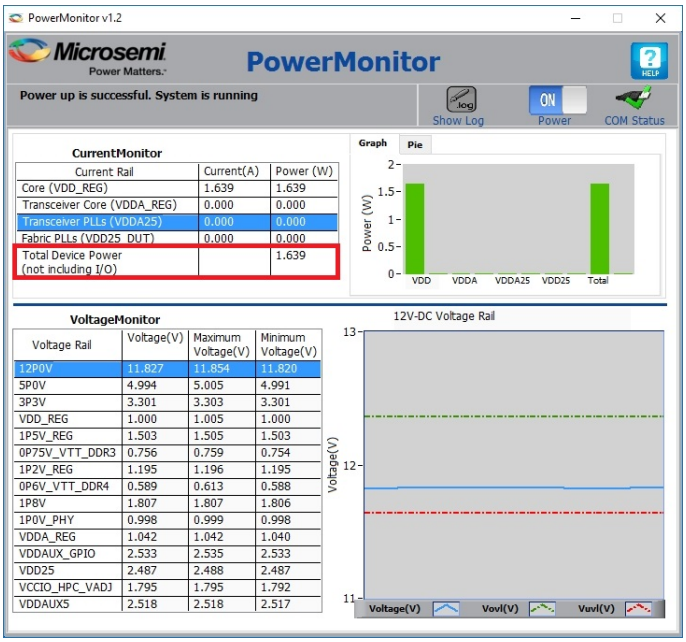
7. To program the design with Low power options (`PF_Demo_Low_power.job`) using FlashPro Express, see, Appendix: FlashPro Express Programming, page 21.
8. The total power consumed by the device is displayed in the Power Monitor GUI.

Figure 16 • **Total Power—PF_Demo_Low_power**



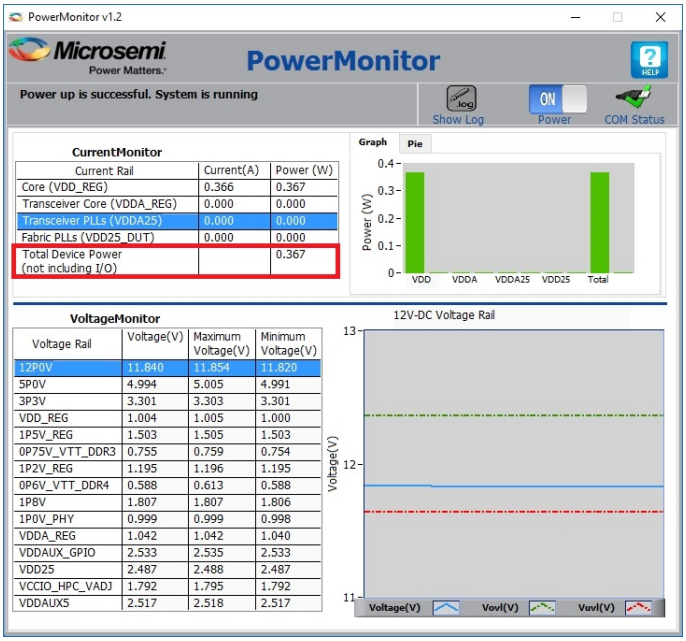
9. Turn off **XCVR** and **TX PLL** by changing **DIP-3 OFF** and measure power.
10. The total power consumed by the device is displayed in the Power Monitor GUI.

Figure 17 • **Total Power XCVR and TX PLL**



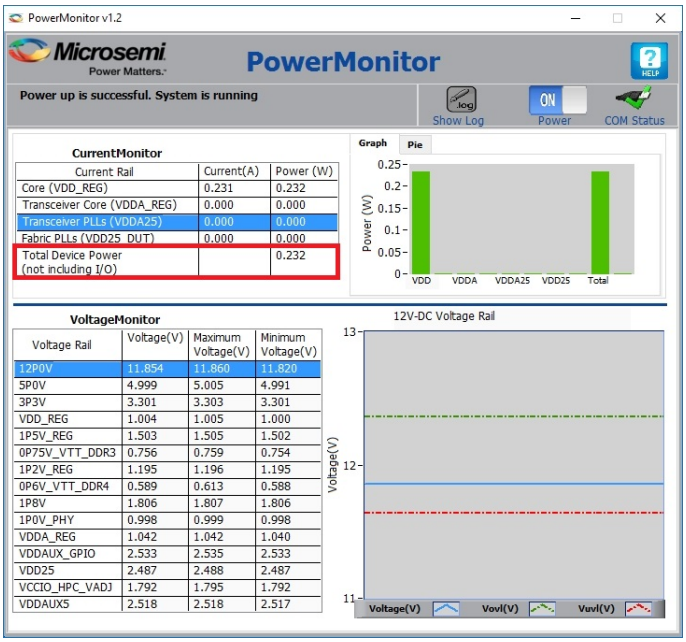
11. Turn on clock gating by changing **DIP-2 ON** and measure power.
12. The LEDs {8, 9}, blinks at different rates as the clock is available. The LEDs {4, 5}, {6, 7}, and {10,11} maintains previous state as the clocks are not available.
13. The total power consumed by the device is displayed in the Power Monitor GUI.

Figure 18 • **Total Power—Clock Gating**



14. Make CCC in power down mode by changing **DIP-1 ON** and measure power.
15. The total power consumed by the device is displayed in the Power Monitor GUI.

Figure 19 • **Total Power—Power Down Mode**



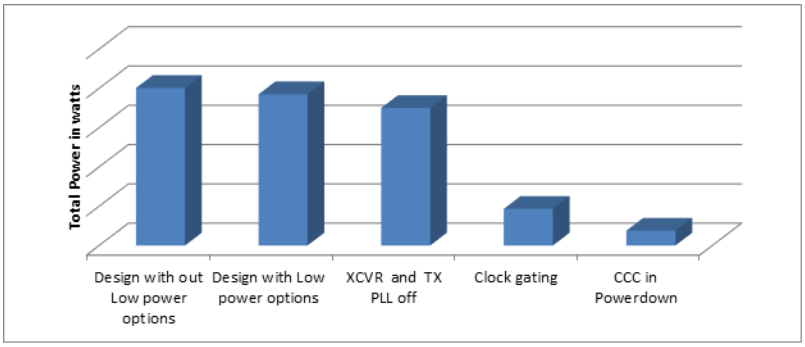
The following table lists the percentage of change after performing the preceding steps.

Table 8 • **Change in Power**

Modes	Percentage of Power Saved After Each Step (Approximately)
Design without Low power options	-
Design with Low power options	5.0
XCVR and TX PLL off	10.0
Clock gating	77.0
CCC in Power down	36.0

The following figure shows the graphical comparison of the power in various modes.

Figure 20 • **Power Comparison**



4 Appendix 1: Programming the Device Using FlashPro Express

This chapter describes how to program the PolarFire device with the Job programming file using a FlashPro programmer. The default location of the Job file is: `mpf_ac485_df\Programming_Job`

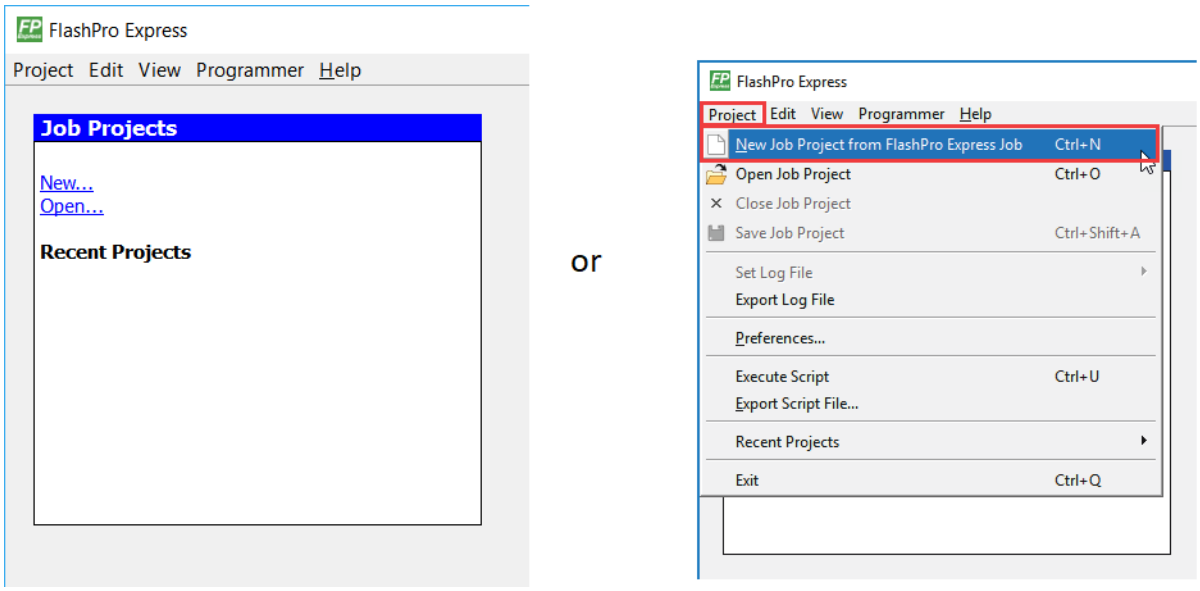
To program the PolarFire device using FlashPro Express, perform the following steps:

1. Ensure that the jumper settings on the board are the same as listed in Table 4, page 25.

Note: The power supply switch must be switched off while making the jumper connections.

2. Connect the power supply cable to the **J9** connector on the board.
3. Connect the USB cable from the Host PC to the **J5** (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.
5. On the host PC, launch the FlashPro Express software.
6. Click **New** or select **New Job Project** from FlashPro Express Job from Project menu to create a new job project, as shown in the following figure.

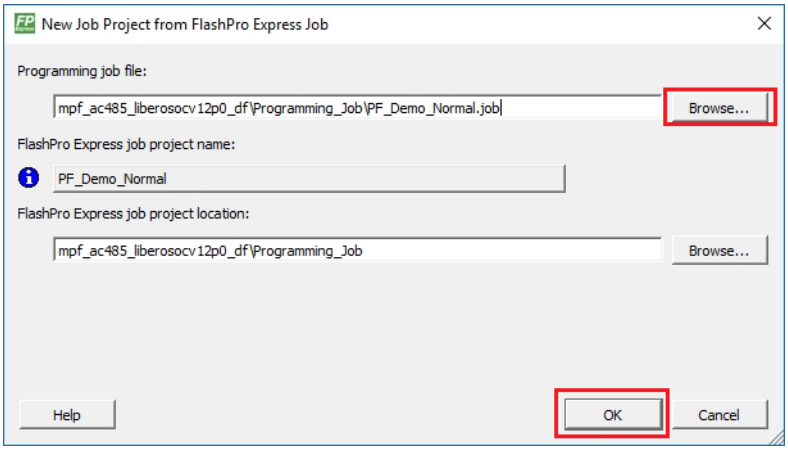
Figure 21 • **FlashPro Express Job Project**



7. Enter the following in the New Job Project from FlashPro Express Job dialog box:

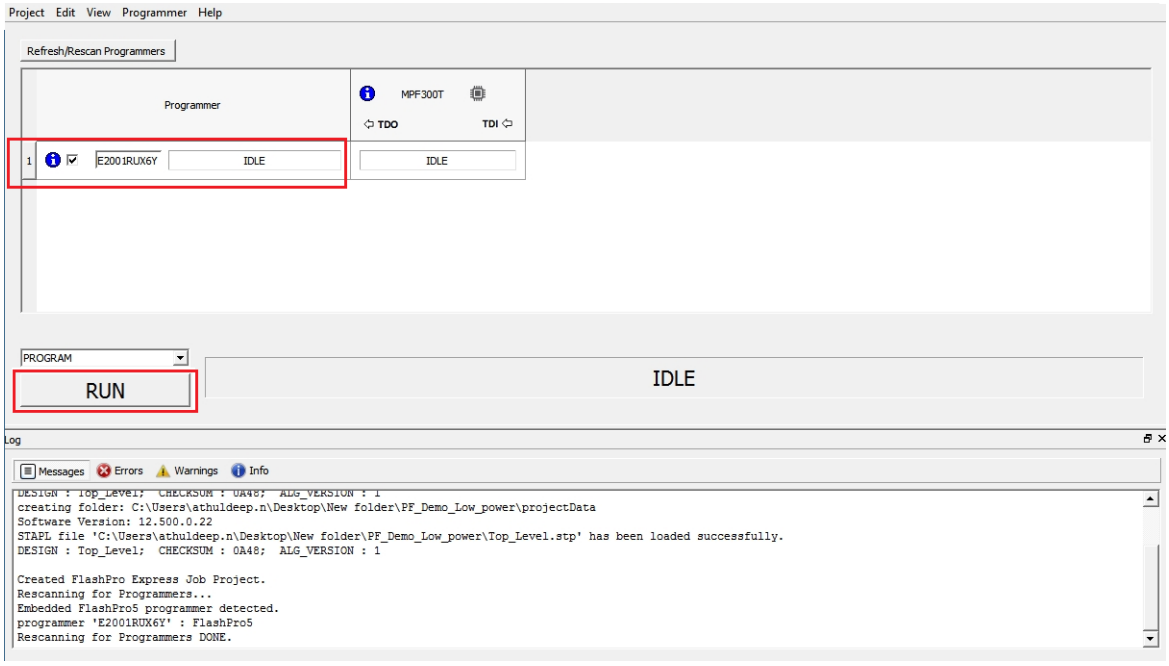
- Programming job file: Click Browse, navigate to the location where the .job file is located, and select the file. The default location is: *<download_folder>\mpf_ac485_df\Programming_Job*.
- FlashPro Express job project location: Click **Browse** and navigate to the location where you want to save the project.

Figure 22 • **New Job Project from FlashPro Express Job**



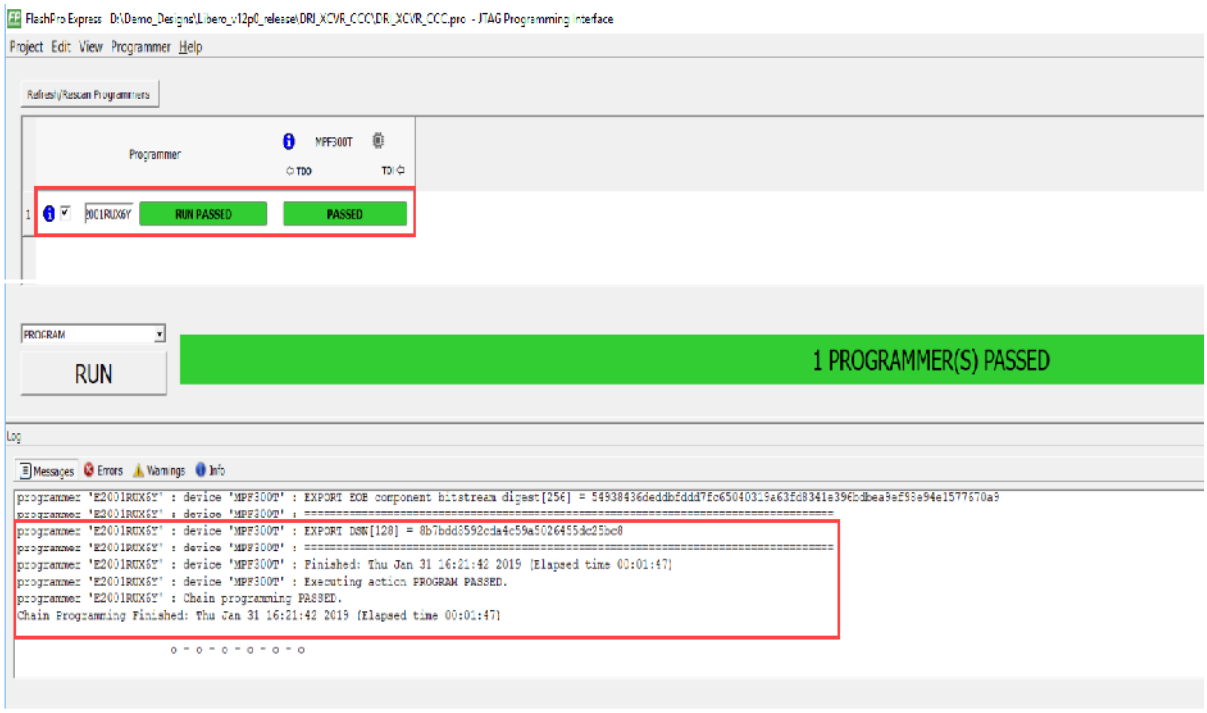
8. Click **OK**. The required programming file is selected and ready to be programmed in the device.
9. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan** Programmers.

Figure 23 • **Programming the Device**



10. Click **RUN** to program the device. When the device is programmed successfully, a RUN PASSED status is displayed as shown in the following figure.

Figure 24 • **FlashPro Express—RUN PASSED**



11. Close **FlashPro Express or** in the **Project tab, click Exit**.

5 Appendix 2: Measuring Power

The following tools are available for power measurement.

- Power Calculator, page 22
- SmartPower, page 22
- Power Monitor, page 22

5.1 Power Calculator

Microsemi Power Estimator (MPE) PolarFire is a spreadsheet-based tool that enables designers to estimate the power consumption of PolarFire FPGAs from design concept to design implementation. It provides thermal analysis, as well as information about the contribution of various factors in the total power consumption of FPGA. Operating frequencies, device resources, clock resources, toggle rates, and other parameters are first entered into the Power Estimator. These parameters are then combined with pre-determined power models based on simulation and characterized device data to estimate power consumption. For more information about the Power Calculator, see *UG0752: PolarFire FPGA Power Estimator User Guide*.

5.2 SmartPower

SmartPower provides a detailed and accurate way to analyze designs for Microsemi SoC FPGAs from top-level summaries to deep down specific functions within the design, such as gates, nets, IOs, memories, clock domains, blocks, and power supply rails. You can analyze the hierarchy of block instances and specific instances within a hierarchy, and each can be broken down in different ways to show the respective power consumption of the component pieces.For more information about the SmartPower, see *SmartPower User Guide Libero SoC PolarFire.*

5.3 Power Monitor

The SmartFusion A2F 200 device on the PolarFire Board, monitors the voltage and current on different PolarFire power rails. It measures the current for different components and displays the power on the Microsemi PowerMonitor application. PowerMonitor is a Graphical User Interface (GUI) application that runs on the host PC. The power monitoring program on the SmartFusion device measures the total device power without any manual measurements. For more information about the Powermonitor, see *UG0747: PolarFire FPGA Evaluation Kit User Guide* Or *UG0786: PolarFire FPGA Splash Kit User Guide.*

6 Appendix 3: Recommendations

This section provides the information about the recommended settings to achieve lower power.

- Transceiver Power Reduction Recommendations, page 23
- LSRAM/uSRAM Power Reduction Recommendations, page 24
- Mathblock Power Reduction Recommendations, page 24

6.1 Transceiver Power Reduction Recommendations

There are options in PolarFire that can be used to reduce the power of the Transceiver PMA and the associated DFE calibration block. The following options are available to reduce the power consumption of the transceiver PMA as well as the DFE calibration block within the PCIESS and transceiver PCS blocks.

- Disabling DFE and EM blocks when CDR mode is used during normal operation
- Disabling EM block (PDEM = 1'b0) when DFE mode is used during normal operation
- Disabling the Calibration clock (DFE_CAL_CEN = 1'b0) when either PDDFE = 1'b1 or PDEM = 1'b1

Note: These settings must be restored before any DFE/CDR calibration or eye monitor functions can be performed.

- Modifying the CTLE Drive settings from the default of 0x2:
  - For setting 0x1, the estimate is that this will reduce the power by 1.5 mW.
  - For setting 0x3 (only for Rev.F), the estimate is that this will increase the power by 3.75 mW (3.93 mW when used with VDDA = 1.05V).
  - For PDDFE=1'b1 and PDEM = 1'b1, the Transceiver PMA power can be reduced further by setting CSENT[3:1]_DFEEM = 0x0.
- Reduce the Tx amplitude:
  - The Tx amplitude should only be large enough to transmit the required data and withstand cross-talk from other lanes as much as possible. Additional amplitude beyond this optimal limit only increases power, noise and cross-talk in the system.
  - De-emphasis should be used to improve the performance of the system by removing high frequency content that must be transferred across the backplane. Modifying de-emphasis parameters has essentially no effect on the overall Transceiver power.
  - Examples of power reduction from the base of 88 mW at 6.875 Gb/s for 1000 mv pk-pk amplitude settings are:

Table 9 • **Example Setting**

S.No	TX Amplitude (mV)	pk-pk (mW)
1	1000	88
2	800	81
3	600	74
4	400	67
5	200	60

- Disable the TxPLL auxiliary clock:
  - If the auxiliary clock from the PLL is not needed it should be disabled by setting TXPLL_AUXDIVPD/EXTPLL_AUXDIVPD = 1'b1. This setting saves the significant power on VDD rail.
  - Some functions within the Serial sub-system require the auxiliary clock output to be enabled. The main function known to require this function to be enabled is the jitter attenuator function.

6.2 LSRAM/uSRAM Power Reduction Recommendations

Following are the LSRAM/uSRAM power reduction recommended settings:

- Disabling the LSRAM read enable signal retains their previous output value and there will be no dynamic read power consumed.
- Use the Block enable signal for read and write address enable logic to avoid the continuous toggling and thereby consumes the power only during read /write operation. During idle disabling the block enable signal saves the power.
- Cascading memory blocks in deep saves the power. For example, two blocks of 1024x20 combined to create 2048x20.

6.3 Mathblock Power Reduction Recommendations

Enabling the input and output pipeline registers in Mathblock avoids the glitches in combinational logic between I/O ports, this reduces the sudden power fluctuations. Also pipelining the IO ports reaches the high performance, but increases the total power due to additional pipeline registers. If the design needs moderate performance with not many glitches, it is recommended to use the non- pipelining to reduce the power consumption in Mathblocks.

7 Appendix 4: Running the TCL Script

TCL scripts are provided in the design files folder under directory TCL_Scripts. If required, the design flow can be reproduced from Design Implementation till generation of job file.

To run the TCL, follow the steps below:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click Browse and select `script.tcl` from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within TCL_Scripts directory.

For more information about TCL scripts, refer to **mpf_ac485_df/TCL_Scripts/readme.txt.**

Refer to *Libero® SoC TCL Command Reference Guide* for more details on TCL commands. Contact Technical Support for any queries encountered when running the TCL script.