Core Deep Learning

ASIC Design Services

A deep learning FPGA platform optimized for implementation on Microsemi FPGAs

Core Deep Learning (CDL) from ASIC Design Services is a scalable and flexible Convolutional Neural Network (CNN) solution for FPGAs. CDL accelerates a wide range of layers typically associated with CNNs . The configurable nature, small real-estate, and low-power properties of FPGAs allow for computationally expensive CNNs to be moved to the node. CDL is the product of a scalable framework that offers the opportunity to stipulate the desired performance, platform specifications, and resource constraints for an application and platform-specific optimized solution. CDL can fit into any FPGA design by scaling to unique customer requirements.

Caffe

CNN design and training with tools from community

Specification
↓
Feasibility Study
↓
CNN Model and Training

Trained CNN model

Core Deep Learning

CNN to RTL with CDL flow

CNN Quantization and Finetuning
↓
Core Optimization

Optimized RTL

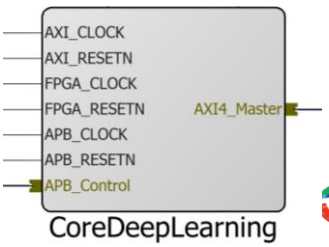
Libero System-on-Chip

RTL to bitstream with Libero flow

Core Implementation
↓
FPGA bitstream

Versatile Network Support

Simple Interface



Device Compatibility

Microsemi Power Matters. PolarFire FPGA

Microsemi Power Matters. SmartFusion2 SoC FPGA

Microsemi Power Matters.

Comprehensive Layer Support

- Convolution
- Depthwise separable
- Concatenation
- Pooling
- Activation
- Fully connected
- Batch normalization

8-Bit Dynamic Fixed-Point data Representation

- Low bandwidth
- Smart quantization
- Negligible accuracy loss
- Efficient hardware usage

Key Features

- FPGA CNN solution
- Hardware only
- Scalable
- Network specific
- Platform optimized
- Low power

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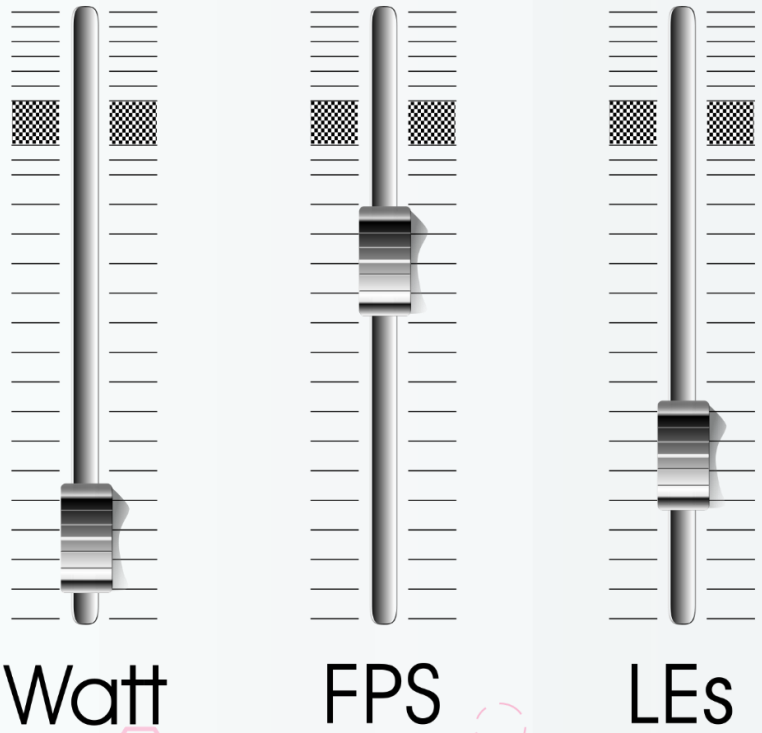
Core Deep Learning

Ultimate User Flexibility



Optimal FPGA Implementation

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