Microsemi Corporation: CN19002

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Customer Notification No: CN19002

Customer Advisory Notification (CAN)

Change Classification: Minor

Subject
RTG4 Family Customer Notifications

Summary
This document describes five customer advisory notices (CANs) for all RTG4 devices. The following table lists a summary of each CAN and the action required by the customer.

Notification	Description	Action Required
CAN 19002.1	Clock Source Latency Calculation	Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP2 or later
CAN 19002.2	ECC Flag for Deeply Cascaded SRAM	Regenerate the RAM using Libero SoC v11.9 SP2 or later
CAN 19002.3	Missing Timing Arc in IP Interface Logic Timing Model	Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP2 or later
CAN 19002.4	Incorrect Net Delay for Hardwired INBUF to GRESET	Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP2 or later
CAN 19002.5	Transient Current During Power-Down	Follow recommended power-down sequences to avoid transient on VDD and I/O glitch

CAN 19002.1 Clock Source Latency Calculation

Reason for Change

When RTG4 input jitter specifications were updated per PCN18009.3, designers were asked to evaluate whether their design could meet the required timing performance with the added clock jitter by specifying clock source latency constraints in SmartTime. Jitter is typically applied to the Max Delay Analysis in SmartTime to perform the worst-case calculation where the launching clock edge arrives late and the capture clock edge arrives early.

However, due to an error introduced in Libero SoC v11.7.SP1, an additional delay (equal to late-early) was incorrectly added to the clock net driven by the clock source in the required time calculation. As a result, the launch to capture window to account for clock jitter did not happen as expected with the clock source latency constraints.

Description of Change

Libero SoC v11.9 SP2 and later remove the extra jitter value that was double counted in SmartTime's data required time calculation. This issue was also addressed in Libero SoC v12.0. The respective software release notes also include a reference to this change. Furthermore, starting with Libero SoC v12.0, clock uncertainty constraints can also be applied within a single clock domain. Previous versions of Libero only applied clock uncertainty constraints between clock domains.

Application Impact

With the clock source latency constraint in place, SmartTime in Libero SoC from v11.7 SP1 to v11.9 SP1 could have shown no violation after accounting for clock jitter because the constraint was effectively nullified by the double-counting of the late-early latency value. There is no issue for cases where the max delay path slack is greater than the total jitter window (late-to-early value). However, if the resulting max delay path slack was less than the jitter window, there could have been a timing violation that was not highlighted in the affected SmartTime versions.

Action Required

Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP2 or later.

Products Affected by this Change

Appendix A lists the products affected. (see page 9)

CAN 19002.2 ECC Flag for Deeply Cascaded SRAM

Reason for Change

Libero SoC v11.9 introduced features in the dual-port LSRAM, two-port LSRAM, and uSRAM configurators to generate logic that gates-off the ECC flags for inactive RAM blocks. The gating logic was correctly generated up to the RAM cascading depths listed as follows, depending on the optimization option selected between high speed or low power:

- Two-port LSRAM low-power 4K x 36
- Dual-port LSRAM 8K x 18
- uSRAM 256 x 18

However, due to the depth limits on the RAM configurators, any RAM components built with a cascading depth greater than eight blocks deep did not include sufficient logic to ensure the correct RAM block's ECC flags reached the component-level flag output ports.

Description of Change

Libero SoC v11.9 SP2 and later lift the depth limits on the RAM configurator, enabling the dual-port LSRAM, two-port LSRAM, and uSRAM configurators to correctly generate logic that gates-off the ECC flags of inactive RAM blocks for all cascade depths.

Application Impact

In pre-synthesis simulation, the ECC flags from the active RAM blocks beyond the above depth limits would be unknown ('X') even during a valid read data out cycle. In post-synthesis simulation, post-layout simulation, and hardware testing, depending on the read address, the ECC flags would remain LOW because the wrong RAM block's ECC flags would be output, meaning that a flag assertion could be missed.

Furthermore, synthesis with Synplify Pro would generate warnings such as the following:

```
@W: CG360 :"C:\...\ TPLSRAM_10213x72_0_RTG4TPSRAM.v":334:8:334:21|Removing wire BLKY2_pipe[2], as
there is no assignment to it.
@W: CL156 :"C:\...\ TPLSRAM_10213x72_0_RTG4TPSRAM.v":334:8:334:21|*Input BLKY2_pipe[2] to
expression [instance] has undriven bits; assigning undriven bits to 0. Simulation mismatch
possible. Assign all bits of the input.
```

The number of blocks cascaded depth-wise can be used to determine whether the particular RAM component uses more than eight RAM blocks deep. RAM components with a cascade depth greater than eight blocks deep must be regenerated using Libero SoC v11.9 SP2 or later.

Action Required

Each RAM component generated by the dual-port LSRAM, two-port LSRAM, and uSRAM configurators includes a log file within the Libero project's sub-folder:

```
/component/work/<component_name>/<instance_name>/
```

The log file lists the RAM cascade configuration as shown in the following example.

```
Cascade Configuration
     Write Port configuration    : 1024x18
     Read Port configuration     : 1024x18
     Number of blocks depth wise : 10
     Number of blocks width wise : 4
```

The number of blocks cascaded depth-wise can be used to determine whether the particular RAM component uses more than eight RAM blocks deep. RAM components with a cascade depth greater than eight blocks deep must be regenerated using Libero SoC v11.9 SP2 or later.

Products Affected by this Change

Appendix A lists the products affected. (see page 9)

CAN 19002.3 Missing Timing Arc in IP Interface Logic Timing Model

Reason for Change

In the specific scenario of a flip-flop directly driving the D input pin of a neighboring IP interface logic's LUT-4 combinatorial cell, including an inversion of a signal, the timing model of the IP interface logic's LUT-4 cell was missing the timing arc from the D pin to the Y pin. As a result, SmartTime did not account for the paths that went through this connection when checking for timing violations.

Description of Change

Libero SoC v11.9 SP2 and later add the missing timing arc.

Application Impact

The missing timing arc was a rare issue that was only observed in less than 1% of our test cases.

An example scenario affected by this issue is the following: A reset synchronizer is used to create an async-assert, sync-deassert reset net for an RTG4 design. This path is expected to be in the "Register-to-Asynchronous" timing set in SmartTime. Depending on the reset polarity of the downstream logic, an inversion is inserted between the output of the synchronizer flip-flop and the GRESET macro. Furthermore, for this issue to affect the design, both the flip-flop and the inverter are placed in an IP interface logic flip-flop and LUT-4 combinatorial cell. Due to the missing timing arc, the path with the inversion is not shown in SmartTime.

Action Required

Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP2 or later.

Products Affected by this Change

Appendix A lists the products affected. (see page 9)

CAN 19002.4 Incorrect Net Delay for Hardwired INBUF to GRESET

Reason for Change

The hardwired input path through an INBUF macro to a GRESET global resource at four specific GRESET input pin locations has zero net delay due to a pin name mismatch. Consequently, the insertion delay calculation for this GRESET path in SmartTime is underestimated.

When running Layout in Libero SoC software, the following messages are printed to notify designers of the incorrect net delay:

```
Error during net delay calculation of net <name> from <INBUF>/U0/U_IOPAD:Y_HW to INBUF>/U0
/U_IOIN_greset:A. Delay set to 0.
Error during net delay calculation of net <name> from <INBUF>/U0/U_IOPAD:Y_HW to <INBUF>/U0
/U_IOIN_greset:A. Delay set to 0.
ERROR: PTOLEMI EXCEPTION: in file: /<internal_path>/ptolemi/src/timnet/hardwiredtimnetmodel.cxx at
line: 612
Error: Cant find hardwired track p2gb_s_7_IOUT_HW_P_greset_loc
```

Description of Change

Libero SoC v11.9 SP2 and later have the correct net delay for hardwired INBUF to GRESET path.

Application Impact

The incorrect net delay for the hardwired INBUF to GRESET path could result in inaccurate timing reporting and timing violation that was not identified by SmartTime.

Action Required

Re-run static timing analysis with SmartTime using Libero SoC v11.9 SP2 or later.

Products Affected by this Change

Appendix A lists the products affected. (see page 9)

CAN 19002.5 Transient Current During Power-Down

Reason for Change

During RTG4 power-down, specific voltage supply power-off sequences can trigger a transient current on the 1.2 V VDD supply. The magnitude of the transient current is dependent on the specific board decoupling capacitance and the transient response of the 1.2 V voltage regulator.

Description of Change

If the 3.3 V VPP supply is ramped down before the 1.2 V VDD supply, and DEVRST_N is tied to VPP, a transient current on VDD will be observed as VPP and DEVRST_N reach about 1 V.

Transient current does not occur if VPP is powered down last, which is also the datasheet recommendation to avoid I/O glitches during power-down.

Application Impact

The transient current on the VDD supply distributes across the entire FPGA fabric and is not localized to a specific area.

Due to the distributed nature of the current and the short duration, there is no reliability concern with this current. Application Note AC439 will be updated to provide an upper boundary on the transient VDD current the RTG4 device can tolerate during this power-down event without causing a reliability concern.

As a best design practice, follow the datasheet recommendation to avoid the transient current.

Action Required

Follow these recommended power-down sequences to avoid transient on VDD and I/O glitch. Application Note AC439 will be updated with these recommendations.

Table 1 • Recommended Power-Down Sequence

						Power-Down Behavior	
Default Output State	**VDD (1.2 V)**	**VDDIx (<3.3 V)**	**VDDIx (3.3 V)**	**VPP (3.3 V)**	**DEVRST_N**	**I/O Glitch**	**Transient Current**
I/O Driving Low or Tri-Stated	Ramp down in any order before VPP			Ramp down last	Tied to VPP	No	No
	Ramp down in any order		Ramp down last[1]		Tied to VPP	No	No
I/O Driving High	Ramp down in any order before VPP			Ramp down last	Tied to VPP	No[2]	No
	Ramp down in any order		Ramp down last[1]		Tied to VPP	No[3]	No

1. Both VDDIx (3.3 V) and VPP must be on the same power rail with a simultaneous power-down profile.
2. No output glitch observed as long as there is no external pull-up resistor on the I/O connected to a power supply that remains powered when VPP ramps down. An external pull-up resistor should connect to a rail which powers-down simultaneously with VDDIx bank voltage.
3. Only applies to MSIO banks powered at 3.3 V that ramp down per footnote 1. Critical I/Os that are pulled-high externally during power-down and cannot tolerate a LOW glitch during power-down should be put on the 3.3 V MSIO banks when following this power-down sequence.

Note: DEVRST_N PAD must not be pulled above the VPP voltage.

Products Affected by this Change

Appendix A lists the products affected. (see page 9)

Appendix A

The following table lists the affected RTG4 devices.

Microsemi Part Number	DLA SMD Number
RT4G150-CB1657PROTO	
RT4G150-CG1657B	5962-1620801QXF
RT4G150-CG1657E	5962-1620805QXF
RT4G150-CG1657EV	
RT4G150-CG1657V	5962-1620809VXF
RT4G150-CG1657PROTO	
RT4G150-CQ352B	
RT4G150-CQ352E	
RT4G150-CQ352EV	
RT4G150-CQ352PROTO	
RT4G150-LG1657B	5962-1620803QZC
RT4G150-LG1657E	5962-1620807QZC
RT4G150-LG1657EV	
RT4G150-LG1657V	5962-1620811VZC
RT4G150-LG1657PROTO	
RT4G150-1CB1657PROTO	
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-1CG1657EV	
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-1CG1657PROTO	
RT4G150-1CQ352B	
RT4G150-1CQ352E	
RT4G150-1CQ352EV	
RT4G150-1CQ352PROTO	
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-1LG1657EV	
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-1LG1657PROTO	

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