RTG4 – MSIO
SEE Testing Report
Tested at LBNL, April 19th 2016

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I. Testing Objectives

Single Event Effects testing was performed on Microsemi's RTG4 FPGA. The objective of this test was to capture Single Event Transients on the MSIOs.

1. Sample preparation

A single sample was used to capture SETs on the MSIOs.
The RTG4 PROTO FPGA tested is identical in design and silicon fabrication to production RTG4 flight model FPGAs.

Table 1 – RTG4 Samples & Configurations

Part Number	Depth Estimate	Revision	Focus
RTG4_Proto29	60um	C	IO SET

2. Testing Conditions

The 16MeV cocktail beam was used at Lawrence Berkeley National Laboratory's Cyclotron facility. The sample was tested at room temperature and at nominal bias on all supplies except VDDI = 2.5V. The irradiation is also performed in vacuum < 1mTorr.

Table 2 below lists all Heavy Ion species used to test the MSIOs on the device and their adjusted effective LET's accounting for tilting and silicon thickness mentioned above in table 1.

Table 2 – Testing Beam Parameters

Species	**Adjusted LET Range (MeV-cm²/mg)**	**Tilting (degrees)**
N	1.23	0
Ne	2.61	0
Si	4.8-5.54	0, 30 & -30
Ar	8.17	0
V	12.5	0
Cu	19.32	0
Kr	30.16	0

II. Summary

1. RTG4 MSIO SET Capture Design

To test the upsets on the FPGA's IOs, 40 IOs were chained in a daisy chain configuration. The last stage IO buffer was then fed into a SET capture circuit which was then reported to the data collection mechanism off chip.

The configuration for the Bi directional input buffer used for daisy chaining the 40 IOs is shown in Figure 1.

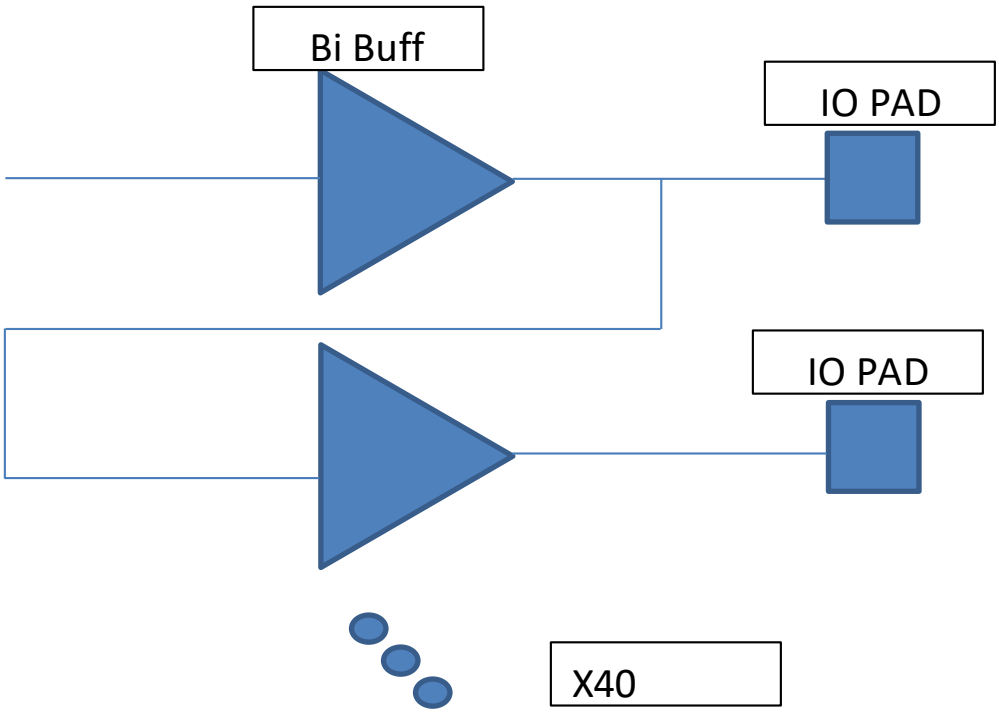

Figure 1: Bidirectional Buffer Configuration for IO SET Test

The SET Capture Circuit consists of 3 Flip Flops configured as shown in Figure 2.

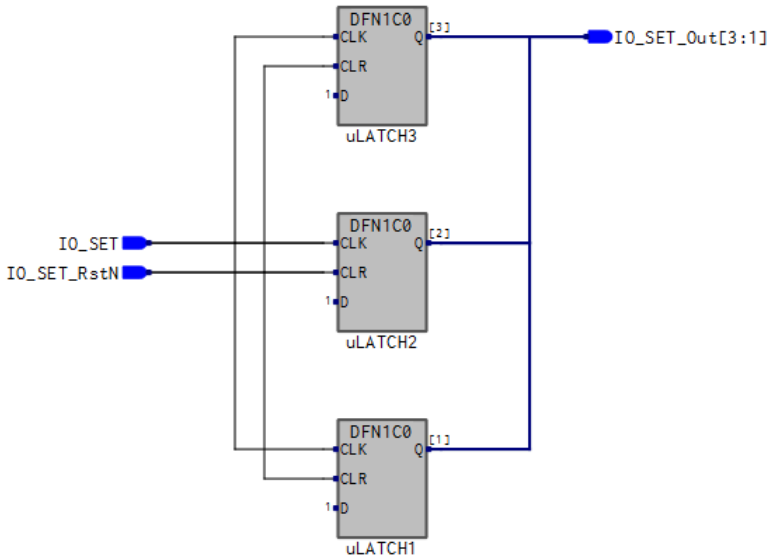

Figure 2: SET Capture Circuit

The Signal IO_SET comes from the last chain of the 40 stages of bi directional buffers and IO Pads as shown in the figure above. Note that the DFN1C0 block is positive edge triggered Flip Flop. If there is a glitch on the clock signal, the Flip Flop will latch in the 1'b1 tied to the D input. The triplication is used to ensure that the glitch comes from the common clock between the 3 Flip Flops which comes from the IO Pads in series.

2. MSIO SET Observations

The triplication of the IO buffers on the pads is enabled (default setting). Table 3 shows the number of errors vs LET. The MSIO SET cross section is shown below in Figure 3, and the Weibull parameters are shown in Table 4. The data shows that the IO buffers are sensitive as low as an LET of 4.8.

LET	Number of Errors	Fluence (ion/cm^2)
1.23	0	9.78E+7
2.61	0	2E+7
4.8	1	2.06E+7
5.54	0	2E+7
8.17	0	2E+7
12.5	2	2E+7
19.32	3	2E+7
30.16	3	2E+7

Table 3: MSIO SET Errors

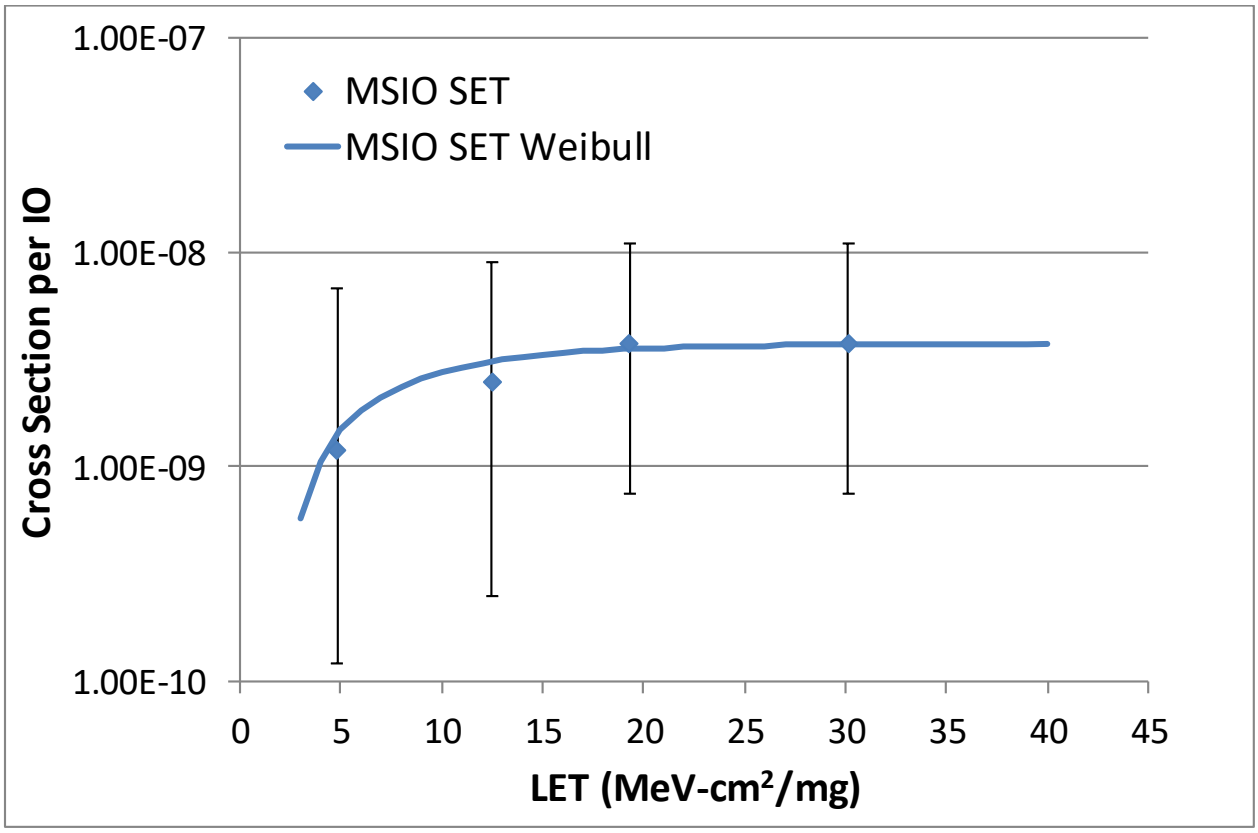

Figure 3: MSIO SET cross section and Weibull Plot.

L0 (MeV·cm²/mg)	W (MeV·cm²/mg)	S	A0 (cm²)
2	6	1.5	4E-09

Table 4: MSIO SET Weibull Parameters

Orbital Upset Rates

From the data presented above, the following is the orbital upset rates calculated using crème 96

MSIO SET	1.03E-08 upset/MSIO/day

Conclusion

A sample size of 40 IOs was used for this MSIO test. The large Error bars are due to the low number of upsets observed since the MSIOs are hardened. The test has identified that glitches on the IOs are observed as low as an LET of 4.8.

Revision History

Date	Comments
7/27/2018	Initial version
9/3/2019	Revised version, removed cross section with SET filter disabled, SET Filter has no impact on the MSIO SET results and only one cross section should be shown.