

Libero SoC v12.0

Release Notes

4/2019



a  **MICROCHIP** company

**Microsemi Corporate Headquarters**

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Fax: +1 (949) 215-4996

Email: sales.support@microsemi.com

www.microsemi.com

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51300213-1/4.19

Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.10

Revision 1.10 includes the following update (04/03/2019):

- Added known issue in section 4.16.1.
- Removed known issue in section 4.16.4.
- Added known issues in section 4.17.1.
- Added known issue in section 4.18.2.
- Updated link in section 5.

Revision 1.9

Revision 1.9 includes the following update:

- Updated section 2.2.

Revision 1.8

Revision 1.8 includes the following updates:

- Updated workaround for second known issue in section 4.18.6.
- Updated description in second bulleted item, section 1.4.3.
- Updated section 4.2.
- Added section 4.4.
- Added known issue in section 4.16.8.

Revision 1.7

Revision 1.7 includes the following updates:

- Added known issue in section 4.17.1.
- Added document link in section 1.1.2.

Revision 1.6

Revision 1.6 includes the following updates:

- Updated section 1.1.4.
- Updated section 1.4.3.
- Updated section 1.4.4.
- Added section 4.2.

Revision 1.5

Revision 1.5 includes the following updates:

- Updated section 1.1.4.
- Added sections 2.2, 2.3, 2.4.

- Added section 4.2.
- Added section 4.5.4.
- Added section 4.10.2.
- Added known issue in section 4.17.1.
- Revised section 4.17.5.
- Added known issue in section 4.18.2.
- Added license daemon note in section 6.

Revision 1.4

Revision 1.4 includes the following updates:

- Added section 2.1.6.
- Added section 4.17.5.
- Added section 4.18.4.
- Added limitation in section 4.18.5.

Revision 1.3

Revision 1.3 includes the following updates:

- Added instructions in section 2.1.4.
- Added known issue in section 4.18.5.
- Added known issue sections 4.2, 4.4.
- Minor text edits and clarifications.

Revision 1.2

Revision 1.2 includes the following updates:

- Added known issue sections 4.21.7, 4.21.8.

Revision 1.1

Revision 1.1 includes the following updates:

- Updated instructions in section 2.1.3.
- Added resolved issue to table in section 3.1.
- Added known issue in section 4.17.1.
- Added known issue in section 4.21.6.
- Updated requirements for CentOS in section 5.

Revision 1.0

Revision 1.0 was the first publication of this document.

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1 Libero SoC v12.0 Software Release Notes

The Libero® system on chip (SoC) v12.0 unified design suite is Microchip's flagship FPGA software, for designing with Microsemi's latest power efficient flash [FPGAs](#), [SoC FPGAs](#), and [rad-tolerant FPGAs](#). The suite integrates industry standard Synopsys [Synplify Pro](#)® synthesis and Mentor Graphics [ModelSim](#)® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.0 for designing with Microsemi's [RTG4](#) Rad-Tolerant FPGAs, [SmartFusion® 2](#) and [IGLOO® 2](#) SoC FPGAs, and [PolarFire](#) FPGAs.

To design with Microsemi's older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. [Development Kits & Boards](#) are listed in the **Design Resources** tab.

1.1 Important Software and Silicon Support Changes

1.1.1 Removal of 130nm Flash-based FPGA support

Libero SoC v12.0 does not support the following 130nm Flash-based FPGA and SoC device families:

- ProASIC3 (including RT ProASIC3)
- ProASIC3E
- ProASIC3L
- IGLOO
- IGLOOe
- IGLOO +
- Fusion
- SmartFusion

Note: Libero SoC v11.9 service packs will continue to support all the above 130nm Flash-based FPGA and SoC device families, as well as IGLOO2, SmartFusion2, and RTG4 (both Classic and Enhanced Constraint Flows). However, the Libero SoC v11.9 software branch is in maintenance mode, and only critical bug fixes will be made going forward.

1.1.2 Removal of Libero SoC Classic Constraint Flow

Libero SoC v12.0 removes support for the Classic Constraint Flow. New projects created with this release will use the Enhanced Constraint Flow, which was introduced with Libero SoC v11.7 for IGLOO2, SmartFusion2, and RTG4 families. IGLOO2, SmartFusion2 and RTG4 projects using the 'Classic' flow cannot be opened in this release. See [Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow](#) for details about how to migrate Classic Constraint Flow projects to the Enhanced Constraint Flow.

1.1.3 Removal of FlashPro Programming Software

Starting with Libero SoC v12.0, the FlashPro software will no longer be included in the Libero design software nor will it be available in standalone mode. Microsemi will be supporting the FlashPro Express v12.0 programming software, which replaces the FlashPro programming software. The last versions of Libero that include FlashPro are Libero SoC v11.9 and Libero SoC PolarFire v2.3.

Users working with Libero SoC v12.0 who would like to use FlashPro standalone programming software can export a STAPL file from Libero SoC v12.0 and program the FPGA using standalone versions of FlashPro v11.9 or FlashPro PolarFire v2.3.

1.1.4 Floating License Server upgrade required

The FlexLM library installed with Libero SoC v12.0 has been updated to v11.16.1. Floating license servers must have the lmgrd and actlmgrd daemons upgraded to v11.16.1 for Libero SoC v12.0 to be able to obtain a floating license. The updated daemons are available for download from the Microsemi website under [Licensing – Downloads](#) and once installed, are backward compatible with earlier Libero SoC releases.

License Server Daemons

License manager daemons are required for server-based (Floating) licenses. They are bundled independently for download to allow users to host their Libero license on their preferred server platform.

Note: The latest actlmgrd v11.16.1.0 version on Windows requires VC++ 2015 Redistributable 32-bit library “vc_redist.x86.exe”. This program can be directly downloaded from Microsoft website at: <https://www.microsoft.com/en-us/download/details.aspx?id=48145>.

For Linux daemons version v11.16.1.0, the following 32-bit system packages are required: redhat-lsb.i686 and glibc.i686.

Complete installation instructions can be found in the [Libero Software Installation and Licensing Guide](#).

1.2 New Device Support

Libero SoC v12.0 includes the following enhancements for PolarFire devices:

- Production timing and power support for the MPF300T/S/TS (1.0V, -1 speed grade) devices
- Preliminary timing and power support for all other production PolarFire devices

Libero SoC v12.0 introduces support for the following devices:

| Family | Die | Pin/Package | Speed Grade | Core Voltage | Temperature |
|--------------|----------|---------------|-------------|--------------|-------------|
| SmartFusion2 | M2S150T | 484 FCV | -1 | 1.2 V | MIL |
| SmartFusion2 | M2S150TS | 484 FCV | -1 | 1.2 V | MIL |
| RTG4 | RT4G150L | 352 CQFP | STD | 1.2 V | MIL |
| RTG4 | RT4G150L | 1657 CCGA/LGA | STD | 1.2 V | MIL |

RT4G150L is the low-power version of the RT4G150 device, featuring 25% static power reduction.

1.3 Design Performance and Runtime Improvements

Libero SoC v12.0 includes runtime enhancements:

- 25% runtime reduction in Place and Route for all families
- 60% runtime reduction in Timing analysis for all families
- 20% runtime reduction in Power analysis for all families
- Peak memory reduction by 50% in high effort Place and Route for PolarFire

Libero SoC v12.0 also includes the following design performance improvements.

- Average Fmax improvement of 4% for all families
- An additional average Fmax improvement of 6% for PolarFire MPF300T/S/TS devices (1.0V, -1 speed grade)
- Up to 30% Fmax improvement for the PolarFire DDR cores

1.4 New Software Features and Enhancements

1.4.1 Project Manager – Design Entry

Libero SoC v12.0 includes major enhancements to the Design Entry step, focusing on ease of use, as well as support for advanced use cases. Many of these enhancements were already available in the Libero PolarFire releases, and are being extended to the SmartFusion2, IGLOO2 and RTG4 device families for the first time in v12.0.

- HDL Language Support has been overhauled, and many enhancements have been made to add support for advanced VHDL-2008 constructs. One of the major enhancement is the support of VHDL configurations.
- Design Hierarchy enhancements:
 - As of Libero SoC v12.0, the Design Hierarchy is not rebuilt on every design change; it is just marked as out-of-date. Users can rebuild the design hierarchy any time by clicking the “Build Hierarchy” button located above the hierarchy frame. Note that the Design Hierarchy is automatically rebuilt, if needed, when invoking the Synthesis or Simulation tools.
 - HDL Generics are now fully elaborated, and used to build a complete Design Hierarchy. These elaborated generics can be viewed in the Design Hierarchy view.
 - Note that you must insert the “*build_design_hierarchy*” command into an existing Tcl script after importing all source files before setting the design root.

For details, see the [Libero SoC Design Flow User Guide](#) and the [PolarFire FPGA Design Flow User Guide](#).

- New SmartDesign Canvas:
 - The redesigned SmartDesign canvas has much more effective symbol placement and connection routing algorithms, enabling a cleaner, more intuitive graphical view of complex designs.
 - The new canvas places all components in columns, with the nets vertically routed in the space between columns. Top-level input ports are placed in the leftmost column. Top-level output ports and inout ports are placed in the rightmost column.
 - The new “highlight” feature works on nets, instances, pins, ports and identifies modified modules.
 - In-place hierarchical expansion of sub-SmartDesign components enables users to quickly drill into sub-hierarchies without changing views.

For details, see the [SmartDesign User Guide](#).

- **Component-Based Instantiation:** This is a change to how IP cores are configured and instantiated into a SmartDesign.
 - IP cores must be configured first before they can be instantiated into a SmartDesign. Configured IP cores are components; they are listed under the new 'Components' node in the Design Hierarchy window.
 - The component-based methodology significantly improves the overall responsiveness of Libero during the design creation phase, minimizing SmartDesign regeneration time when instantiated Components undergo incremental changes.
- This release includes major upgrades to Tcl-based flow and design automation. Tcl-based design entry for SmartDesign, HDL+, and Core Configuration is now supported, including the export of Tcl scripts from a GUI-based design entry session for scripted execution and replay of the design entry phase.

For details, refer to the [Libero SoC v12.0 Tcl Command Reference Guide](#) or the [PolarFire FPGA Tcl Command Reference Guide](#).

1.4.2 Other Project Manager Enhancements

- New in Libero SoC v12.0 is support for the Microsemi Design Separation Methodology (for security and safety critical applications) using the Enhanced Constraints Flow. In previous releases, this methodology required the Classic Constraints Flow.
Note: Only SmartFusion2 and IGLOO2 support the Microsemi Design Separation Methodology.
- Libero SoC v12.0 implements an important customer-requested enhancement to vault handling. Users running Libero no longer need to have write access permissions to the Libero vault.
- Libero SoC v12.0 on Linux no longer requires an X-Server display when run in batch mode.

1.4.3 Synthesis

SynplifyPro N201803MSP1-1 is the OEM Synthesis tool integrated with Libero SoC v12.0. This version of SynplifyPro provides key enhancements and bug fixes.

- **SynplifyPro Synthesis tool .vm netlist generation**

In Libero SoC v12.0 and later releases, for PolarFire, the SynplifyPro Synthesis tool will always generate a Verilog gate level netlist (.vm) instead of an EDIF netlist. For SmartFusion2, IGLOO2, and RTG4, an EDIF netlist is generated, as before.

- **RTG4 Defeature Read-before-write for inferred LSRAM**

Read-before-write mode is not supported for the RTG4 LSRAM per Product Change Notification 18011. By default, when Read/Write Check insertion is OFF, the RAM1K18_RT LSRAM primitive is inferred in the Simple-write mode (in which Read-data port holds the previous value). When Read/Write Check insertion is ON, single-port RAM in Read-before-write mode is inferred as uSRAM RAM64x18_RT and fabric logic, but true dual-port RAM in Read-before-write mode is no longer supported. Synthesis will fail with the below error when the "rw_check" directive is enabled:

```
Cannot map <memory[MSB:0]> due to multiple write clocks
```

- **Packing of registers with Asynchronous assertion and Synchronous de-assertion into FF, LSRAM and URAM blocks**

SynplifyPro now supports the packing of both asynchronous and synchronous reset signals into FF, LSRAM and uSRAM blocks for PolarFire, RTG4, SmartFusion2 and IGLOO2 families.

- **Warning against suboptimal priority between Enable and Synchronous reset signals on FF, LSRAM, uSRAM and MATH blocks**

SynplifyPro will issue a warning when it detects suboptimal priority (Synchronous reset having precedence over Enable) between Enable and Synchronous reset signals on FF, LSRAM, uSRAM and MATH blocks for PolarFire, RTG4, SmartFusion2 and IGLOO2 families.

- **Message browser**

Libero SoC v12.0 will extract all design specific messages from the synthesis log (*.srr) and display them into the hierarchical message window for ease of browsing and filtering.

- **Synthesis implementation**

Libero SoC v12.0 will now show the name of the current synthesis implementation folder below the root module in the Design flow window.

- **PolarFire Automatic Compile Points**

Libero SoC v12.0 adds an option in the synthesis configurations dialog to enable Automatic Compile Points. When enabled, execution of synthesis iterations will be faster based on how many such Compile points remain unchanged from the last iteration.

- **PolarFire Symmetric FIR Filter Packing into MATH blocks**

SynplifyPro now supports the packing of Symmetric FIR filters through the inference of MATH blocks with shift chain.

- **PolarFire Packing of Asynchronous Reset and Dynamic Offset in Sequential shifts**

SynplifyPro now supports the packing of Asynchronous reset and Dynamic offset logic in sequential shifts through the inference of uSRAM blocks for PolarFire.

- **PolarFire Dual Port ROM Support**

SynplifyPro now supports Dual port ROM inference using RAM1K20 macros for PolarFire.

- **PolarFire RAM Report generation for inferred LSRAM and uSRAM**

A detailed report is generated in the <libero_project>/synthesis/{implname}_ram_rpt.txt file with details of the LSRAM and uSRAMs inferred for a design.

1.4.4 Timing Constraints

Libero SoC v12.0 adds a set of new timing constraints commands that expand the set of scenarios that can be analyzed by SmartTime:

- The new '*-add_delay*' option for the *set_input_delay* and *set_output_delay* SDC command enables you to specify a second max (or min) input/output delay constraint on the same port. This option is commonly used to constrain an input/output port relative to more than one clock edge (for example, in a DDR Interface).
- The new '*-add*' option for the *create_clock* and *create_generated_clock* commands enables you to apply multiple clocks constraint to the same clock port. You can define as many constraints as appropriate for your design by specifying the *-add* option for all clocks after the first.
- A *simple uncertainty* option for the *set_clock_uncertainty* command enables you to specify the clock uncertainty on a single clock.
- The new '*-edges*' option for the *create_generated_clock* command enables you to specify how a generated clock transforms the reference clock waveform by referencing the edges instead of a division factor. The frequency of the generated clock can also be specified using this option.
- The new '*-edge_shift*' option for the *create_generated_clock* command enables you to specify a shift between the reference edge and the generated edge.

For details about the options above, refer to [UG0679: Timing Constraints Editor User Guide](#).

In Libero SoC v12.0, the Place and Route tool for RTG4, SmartFusion2 and IGLOO2 has been enhanced to interpret timing exception constraints such as *get_nets*, *get_clocks*, *max_delay*, *multicycle*, *-from {*}*, *-to {*}*.

1.4.5 SmartDebug

FPGA Hardware Breakpoint Enhancements

Libero SoC v12.0 adds FPGA Hardware Breakpoint Auto Instantiation (FHB) support for the RTG4 and PolarFire FPGA families.

In addition, for all supported families, the following enhancement to FHB have been added:

- The number of clock cycles supported for VCD capture has been increased to a maximum of 1,000

PolarFire Silicon Debug Enhancements

Continuing the work to provide a state-of-the-art on-chip FPGA debug tool, this release of SmartDebug includes the following enhancements targeting the PolarFire device family:

- PCIe Debug: The PCIe Debug page shows the following content of the PCIe link used in the design
 - LTSSM state of the PCIe link
 - PCIe lane status and lane link error status
 - PCIe configuration space
- Transceiver Eye Monitor enhancements
 - Three eye plot modes are now supported in Libero SoC v12.0: Normal mode (single eye plot), Infinite Persistence mode (eye plot over a period of time until halted by user), and Design initiated eye plot

For details about SmartDebug, see the following documents:

[UG0638: SmartDebug User Guide \(SmartFusion2, IGLOO2, RTG4\)](#)

[UG0773 SmartDebug User Guide \(PolarFire\)](#)

1.4.6 Programming

SmartFusion2 and IGLOO2 SPI-Slave Programming

FlashPro Express v12.0 supports SPI-Slave Programming for SmartFusion2 and IGLOO2 families.

Note: PolarFire SPI-Slave programming will be supported in a future release. SPI-Slave programming is not supported for RTG4 devices.

Export Pass Keys in Plaintext

Users can explicitly select to include plaintext pass keys, if desired. By default, all exported bitstream files will not include plaintext pass keys.

Bitstream files which include plaintext pass keys should only be used in trusted environments. FlashLock/Pass keys are needed if the bitstream file is targeted to update a feature that is FlashLock/Passkey protected.

Note: Prior to the Libero SoC v12.0 release, exported *_master* bitstream files and exported *_uek1/_uek2* bitstream files with protected sNVM /Fabric pass keys or locked Program, Authenticate, and Verify actions included plaintext pass keys.

Secure Production Programming Support (SPPS)

Libero SoC v12.0 adds Secure Production Programming Support for PolarFire.

1.5 New Silicon Features and Enhancements

1.5.1 PolarFire Transceiver Solution

Transceiver Enhanced Receiver Management Solution

- Libero SoC v12.0 replaces the existing PolarFire transceivers solution with the Enhanced Received Management (ERM) solution. Refer to [UG0677: PolarFire FPGA Transceiver User Guide](#) for details on when and how to use / implement this enhanced solution.
- All projects containing Transceivers must be upgraded to use the Enhanced Received Management solution, including using latest Transceiver cores versions and the latest PolarFire Transceiver Interface core (PF_XCVR_ERM). For more details, refer to the “Migrating Designs to Libero SoC v12.0” section.

Transceiver Reference Clock

- Libero SoC v12.0 adds support for all Transceiver Reference Clock input standards.

TxPLL Jitter Attenuation

- Libero SoC v12.0 adds Jitter Attenuation support for CPRI rates 1 to 6 and SDI SD/HD/HD3G use models.

SDI Support

- Libero SoC v12.0 adds a new CDR lock mode ‘Lock to data with 2x gain’ in the PolarFire Transceiver Interface core (PF_XCVR_ERM) to support SDI use models. Refer to [UG0677: PolarFire FPGA Transceiver User Guide](#) for details on how to implement SDI use models.

1.5.2 PolarFire IOD Interfaces

- Libero SoC v12.0 adds the capability of doing external timing checks on IOD interfaces using SmartTime.

1.5.3 PolarFire IO's

- **Enhanced Pin Report:** Libero SoC v12.0 introduces an enhanced pin report. The enhanced report shows detailed information for all pins – used and unused - of the targeted device package.
- **Mixed voltage receiver mode:** Libero SoC v12.0 adds mixed voltage receiver mode support for GPIOs and HSIOs for the PolarFire family.
- **External Hold Repair:** If a design has external hold time violations, turn on Repair Minimum Delay Violations (which is off by default in Libero SoC v12.0) and it will attempt to fix the violations automatically by adjusting programmable delays through both input or output I/Os. See the report `<root>_mindelay_repair_report.rpt` in the `<project>/designer/<root>/` directory, which lists all paths that were considered.

1.5.4 PolarFire Multiple UJTAG

PolarFire designs in Libero SoC v12.0 can now contain multiple UJTAG cells from various user sources including Synopsys Identify and external IP. Post-synthesis optimization will merge the multiple UJTAG cells into one where each input signal is combined appropriately (either union or intersection).

1.5.5 RTG4 LSRAM Write Byte Enables

RTG4 Two-port and Dual-port LSRAM configurators in Libero SoC v12.0 expose Write Byte Enable control signals (WBYTE_EN for Two-port LSRAM and A_WBYTE_EN, B_WBYTE_EN for Dual-port LSRAM). You can apply these signals to design a handshake circuit for accessing LSRAM data through SmartDebug.

For more information, refer to [CN19001 RTG4 LSRAM Data Errors When Accessing SmartDebug](#).

1.5.6 RTG4 UPROM File Formats

RTG4 UPROM configurator in Libero SoC v12.0 adds support for the following memory file formats in addition to the Microsemi-Binary format (*.mem):

- Intel-Hex (*.hex, *.ihx)
- Motorola-S (*.s)
- Simple-Hex (*.shx)

1.5.7 SmartFusion2, IGLOO2 and RTG4 I/Os

With Libero SoC v12.0, Automatic I/O Register Combining is available as an option. It can be selected in the Place and Route configurations dialog. The default setting is ON for RTG4, SmartFusion2 and IGLOO2 designs. Enable this option to combine any register directly connected to an I/O when it has a timing Constraint.

2 Migrating Designs to Libero SoC v12.0

2.1 Notes on Design Migration

2.1.1 General Notes for SmartFusion2, IGLOO2, and RTG4

SmartFusion2, IGLOO2, and RTG4 support only the Enhanced Constraint Flow in Libero SoC v12.0. Only designs created with the Enhanced Constraint Flow in Libero SoC v11.9 SP2 and earlier versions can be opened with Libero SoC v12.0. You must manually port designs created with the Classic Constraint Flow to the Enhanced Constraint Flow with Libero SoC v12.0.

Note: A document that describes how to migrate Classic Constraint Flow to Enhanced Constraint Flow will soon be published on the Microsemi website.

2.1.2 PolarFire Tool Invalidation

Libero SoC v12.0 is a major release milestone in the Microsemi® PolarFire FPGA product life cycle. Bug fixes and enhancements to some silicon features may require upgrading cores and re-running design flow steps for users migrating from Libero SoC PolarFire v2.3.

For all PolarFire devices, after opening your project in this release, the Place and Route tool will be invalidated, and must be re-run.

2.1.3 PolarFire Core Invalidation

Designs containing the following cores will be invalidated upon migrating Libero SoC PolarFire v2.3 projects to Libero SoC v12.0:

- CoreSmartBERT (CORESMARTBERT)
- PolarFire PCI Express (PF_PCIE)
- PolarFire QDR (PF_QDR)
- PolarFire IOD Generic Receive Interfaces (PF_IOD_GENERIC_RX)
- PolarFire Transceiver Interface (PF_XCVR)
- PolarFire Transceiver Interface (PF_TX_PLL)

For the above cores, you must do the following:

1. Download the latest version of the core into your vault.
2. For all cores except PF_XCVR, upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting 'Replace Component Version...'.
3. To upgrade the PolarFire Transceiver Interface (PF_XCVR), see the important migration notes below.
4. Regenerate the design.
5. Rerun the Derive Constraints step.
6. Rerun the tool flow.

Important Migration Notes:

- When migrating to the latest PolarFire PCI Express core version, note that the PCIE_WAKE_N signal is no longer exposed by default. You must correct the design accordingly.
- When migrating existing PolarFire Transceiver Interface (PF_XCVR) components, you must configure a new transceiver interface component as per the new guidelines described in [UG0677: PolarFire FPGA Transceiver User Guide](#). You also must follow the below steps:
 - Keep a screenshot of the transceiver interface configuration using the Libero PolarFire v2.3 software.

- Close all SmartDesign components in which the PolarFire Transceiver Interface (PF_XCVR) component is instantiated.
- Delete the existing PF_XCVR configured core component from the Design Hierarchy.
- Create a new transceiver component using the new PolarFire Transceiver Interface (PF_XCVR_ERM) core as per your required previous component configuration and the new guidelines in [UG0677: PolarFire FPGA Transceiver User Guide](#). The new component should have the same name as the one that was removed in the previous step.
- Open all SmartDesign components in which the transceiver component was instantiated previously and see if there are any port-list changes on the transceiver component with the new core and configuration. If there are any port-list changes, right-click on the transceiver component's instances in each SmartDesign and choose the option 'Update Component' to update the port-list.
- All existing pin connections for transceiver components in the SmartDesign will be intact. You only need to take care of the new port-list changes if there are any.
- Repeat the steps above for all PolarFire Transceiver Interface (PF_XCVR) components in the design.

2.1.4 PolarFire Core Upgrade

If a Libero SoC PolarFire v2.3 created project contains the following cores, and the cores have been generated, they do not need to be upgraded upon migrating the project to Libero SoC v12.0. However, if the core needs to be generated again for any reason (for example, change in parameters), the latest version from the Catalog must be downloaded and used.

- PolarFire DDR3
- PolarFire DDR4
- PolarFire LPDDR3
- PolarFire SRAM (AHBLite and AXI)
- PolarFire Crypto
- PolarFire System Services
- PolarFire IOD CDR

For the above cores, you must do the following:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting 'Replace Component Version...'.
 3. Regenerate the design.
 4. Rerun the Derive Constraints step.
 5. Rerun the tool flow.

2.1.5 PolarFire Physical Design Constraints (PDC) required changes

When migrating an existing PolarFire design to Libero SoC v12.0, PDC constraints must be changed for the following cases:

IO PDC update:

- The RX_CDR_AUTO_CAL (CDR auto-calibration) transceiver Signal Integrity port attribute has been removed as part of the Enhanced Received Management (ERM) solution. You must remove this attribute from any PDC file if it is present.
- The set of IN_DELAY (Input delay) port attribute legal values has changed. You must fix this attribute from any PDC file if the value that was used is now illegal. Legal values are [0-127, 128, 130, 132, ..., 254].
- For true differential I/Os, the VICM_RANGE (Vcm Input Range) port attribute has the following restrictions. One cannot have true differential I/Os in the same GPIO bank that have a mix of MID and LOW values.

FP PDC update:

- When migrating a transceiver design to the Enhanced Received Management (ERM) solution, the internal hierarchical names of Transceiver Interface components will change. For example, in Libero SoC PolarFire v2.3, when a Transceiver Interface instance is placed with the I/O Editor, a line similar to the following is seen in the FP PDC file:

```
set_location -inst_name xcvr_0/xcvr_0/LANE0 -fixed true -x 1596 -y 44
```

When migrating this design to Libero SoC PolarFire v12.0, the above line should be deleted.

2.1.6 PolarFire Synopsys Design Constraints (SDC) Update

When a XCVR macro is updated, user SDC's must also be updated to include the new hierarchical name.

2.2 PolarFire Devices' Timing and Power Data State in Libero SoC PolarFire v12.0

In this release, the timing and power data states for the MPF300T/TS (1.0V, -1 speed grade) have been upgraded to "Production". All other PolarFire devices now have Preliminary timing and power data. The table below summarizes timing and power data state for all PolarFire devices as of Libero SoC PolarFire v12.0.

| Device | Timing Data State | Power Data State |
|---|-------------------|------------------|
| MPF100T/TS/TL/TLS | Preliminary | Preliminary |
| MPF200T/TS/TL/TLS | Preliminary | Preliminary |
| MPF300TES/TS_ES | Preliminary | Preliminary |
| MPF300XT | Production | Production |
| MPF300T/TS/TL/TLS (1.05V: all speed grades; 1.0V STD speed grade) | Preliminary | Preliminary |
| MPF300T/TS/TL/TLS (1.0V: -1 speed grade) | Production | Production |
| MPF500T/TS/TL/TLS | Preliminary | Preliminary |

2.3 Cores in Production status in Libero SoC v12.0

| Display Name | Libero SoC v12.0 | Changes from Libero SoC PolarFire v2.3 |
|---------------------------------------|------------------|--|
| PF Clock Conditioning Circuitry (CCC) | 1.0.115 | None |
| PF Clock divider | 1.0.103 | None |
| PF CoreSmartBERT | 2.3.102 | No functional changes Uses the latest Transceiver Interface core version |
| PF Crypto | 1.0.106 | No functional changes Updated the Embedded DLL Jitter label/options for clarity |
| PolarFire QDR | 1.3.200 | No functional changes Improved the generated constraints for better constraint coverage |

| | | |
|---|---------|--|
| | | Added fast simulation (BFM) option |
| PF Glitchless clock mux | 1.0.101 | None |
| PF PCI Express | 2.0.100 | <p>No functional changes</p> <p>Updated the Embedded DLL Jitter label/options for clarity</p> <p>The PCIE_WAKE port is not exposed by default</p> <p>Improved the generated netlist for better constraint coverage off the AXI interface</p> |
| PF Dual-Port Large SRAM | 1.1.110 | None |
| PF Micro SRAM | 1.1.107 | None |
| PF Two-Port Large SRAM | 1.1.108 | None |
| PF uPROM | 1.1.108 | None |
| PolarFire Dynamic Reconfiguration Interface | 1.0.101 | None |
| PolarFire IOD Generic Receive Interfaces | 1.1.111 | <p>No functional changes</p> <p>Improved the generated constraints for better constraint coverage</p> |
| PolarFire IOD Generic Transmit Interfaces | 1.1.106 | None |
| PolarFire Initialization Monitor | 2.0.103 | None |
| PolarFire RC Oscillators | 1.0.102 | None |
| PolarFire RGMII TO GMII | 1.1.105 | None |
| PolarFire SRAM (AHBLite and AXI) | 1.1.127 | <p>No functional changes</p> <p>Added help link</p> |
| PF Tamper | 1.0.107 | None |
| PF Temperature and Voltage Sensor Interface | 1.0.106 | None |
| PF Transceiver Reference Clock | 1.0.103 | None |
| PF Transmit PLL | 2.0.002 | <p>Added Low/High Bandwidth selection (default is low)</p> <p>Added CPRI 1-6 / SDI-SD/HD/HD-3G Jitter cleaner support</p> |
| RTG4 Two-port Large SRAM | 1.1.109 | Option to expose Write Byte Enables. The BUSY output from v1.1.107 is no longer available. |

| | | |
|---------------------------|---------|---|
| RTG4 Dual-port Large SRAM | 1.1.106 | Option to expose Write Byte Enables. The “DOUT on write” (Read-before-write) option is no longer available. |
|---------------------------|---------|---|

2.4 Cores in Pre-production status in Libero SoC v12.0

| Display Name | Libero SoC v12.0 | Changes from Libero SoC PolarFire v2.3 |
|---------------------------------|------------------|--|
| PolarFire DDR3 | 2.3.200 | No functional changes Improved the generated constraints for better constraint coverage |
| PolarFire DDR4 | 2.3.200 | No functional changes Improved the generated constraints for better constraint coverage |
| PolaFire LPDDR3 | 2.2.200 | No functional changes Improved the generated constraints for better constraint coverage |
| PolarFire IOD CDR | 1.1.200 | No functional changes |
| PolarFire Transceiver Interface | 2.0.201 | New core See details in section 1.3.1 |
| PF CoreSmartBERT | 2.3.102 | No functional changes Uses the latest Transceiver Interface core version |
| PolarFire System Services | 2.2.201 | No functional changes Added help link |

3 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC v12.0. Resolution of previously reported "Known Issues and Limitations" is also noted in this table.

3.1 List of Resolved Issues

| Case Number | Description |
|-------------------|---|
| 493642-2559621344 | TPSRAMX36 mode with write and read clocks are different: RTG4 Two Port Memory ECC Error Flags going 'x' in Libero v11.9SP2 |
| 493642-2514901135 | RTG4TPSRAM v1.1.107 pre-synth simulation issue with ECC flags |
| 493642-2521157111 | Program action should detect MPF300ES or XT devices |
| 493642-2527865326 | Libero batch mode error - cannot connect to X server |
| 493642-2523233678 | SmartFusion2, IGLOO2 and RTG4: The delay value 8ns (late-early, 4-(-4)= 8 ns) is getting added to the clock net delay FCCC_0/GLO_net value in the required time calculations when we apply the latency clock constraints. |
| 493642-2521895093 | SmartTime crashes in Libero Linux v11.8/v11.9, hangs in Windows |
| 493642-2517658133 | Link for user guide of PolarFire System Services shows error |
| 493642-2474396566 | Documentation: Remove FlashLock/UPK1 protection option of eNVM bitstream programming/verify and read (from lock spreadsheet) |
| 493642-2474396566 | Remove FlashLock/UPK1 protection option of eNVM bitstream programming/verify and read |
| | Device Status - if user security is programmed, eNVM protection by UEK1/2 should be displayed regardless of the lock setting |
| | SmartFusion2/IGLOO2 Engine: Remove FlashLock/UPK1 protection option of eNVM bitstream programming/verify and read |
| 493642-2476865426 | The JTAG voltage for IGLOO2 060 device is 3.3V |
| 493642-2471364031 | Synplify does not add CLKINT after INBUF_DIFF driving PLL and 41 FFs |
| 493642-2539809132 | AXI4 interconnect core in a VHDL project fails synthesis |
| 493642-2535535133 | Error: No solution was found which could accommodate the global nets (and their drivers) |
| 493642-2527824479 | Libero fails with "tao.exe has stopped working" message |
| 493642-2277021577 | Place and Route tool should generate a single Pin Report which contains all information |
| 493642-1025009105 | Support for pin-out report from Designer in CSV format |
| 493642-2448596660 | Support for mentioning "open drain" output pin/s in IO report |
| 493642-2520262281 | M2GL050TS incorrect I/O count in power calculator v10d |
| 493642-2520212891 | SmartDebug does not show logical memory blocks |
| 493642-2517557174 | PolarFire: Placer to enforce only 1 RGB per source on each quarter-row |
| 493642-2511149470 | PolarFire PCIE: Add AXI Clock Frequency range option |
| 493642-2505472685 | SmartTime crashes after reopening it |
| 493642-2508234396 | PolarFire: Placer to allow at most 4 locally routed RGB per half-row |
| 493642-2505472685 | Crash at Synthesis stage |
| 493642-2505472685 | SmartTime crashes after reopening it |

| | |
|---|--|
| 493642-2504689177 | Constraint checker should issue a warning when input-delay and external check overlap |
| 493642-2474502908 | PolarFire IO's: Vref voltage for VDDI1.2 is mentioned as 0.75V |
| 493642-2456664732 | I/O Bank Assignment: No solution was found which could accommodate the global nets and drivers |
| 493642-2349601283, 493642-2396162779, 493642-2450968851 | Batch Mode: Remove X-Server Dependency for Libero |
| 493642-2430404453 | Place and Route fails due to Verify Timing errors but SmartTime shows no timing errors |
| 493642-2492873587 | The pin report does not include ODT values for Transceiver Interface or Reference Clock pins |
| 493642-2464509920 | Addition of Mixed Voltage Receiver mode support for PolarFire GPIOs and HSIOs |
| 493642-2384627802 | Libero help file should have the VHDL language version support info |
| 493642-2383176414 | verifichdlsynchk.exe crashes and after that Libero crashes |
| 493642-2357669988 | Reg SmartTime Datasheet report is incorrect in calculations |
| 493642-2349889033 | M2S encrypted flow causes minimum delay violations |
| 493642-2353437944 | Libero cannot handle VHDL generics properly |
| 493642-2340538903 | Tcl to support core configuration, generate core |
| 493642-2498053109 | FEC design crashes on verifc |
| 493642-2273111580, 493642-2343409381 | VHDL Configuration clause synthesis issue |
| 493642-2498053109 | Polarfire: tao.exe crashes for attached design |
| 493642-2224710682 | Tcl: Importing/recreating Libero designs with components that contain BIFs |
| 493642-2223893253 | Tcl support for Generate Design in Canvas |
| 493642-2456678571 | Need support for SPI Slave programming in standalone environment (outside Libero) |
| 493642-2045251567 | Need a Tcl command to 'generate' a component for SmartDesign |
| 493642-1626502288 | Tcl commands in the Export Script file |
| 493642-2422045030 | Request to document TCL commands for SmartDesign |
| 493642-2567607057 | SmartTime "Verify timing" has a bug in fast corner |

4 Known Issues and Limitations

4.1 Catalog Cores

4.1.1 Core Generation Language

With Libero SoC v12.0, some cores generate only Verilog files, regardless of the preferred HDL language selected in the Libero project. All PolarFire cores listed in section 2.3 above.

VHDL users desiring to simulate designs containing affected cores must use mixed-language simulation (available with ModelSim ME Pro, which is bundled with this release, and requires a Gold, Platinum, or Eval license).

4.1.2 Linux: Core generation fails in batch mode when the DISPLAY variable is not set

The following Direct Cores cannot be generated in Libero in batch mode via Tcl when the DISPLAY variable is not set on a Linux machine.

- CoreAXI4SRAM
- CoreCIC
- CoreCordic
- CoreABC
- CoreEDAC
- CoreDDS
- CoreFIFO
- CoreFFT
- CoreFIR_PF
- CoreRSDEC
- CoreRENC

4.2 Tcl Support Limitation

Parameters for SgCore and System Builder components are not documented. To configure such cores using Tcl, do the following:

1. Use the GUI to configure the core as desired.
2. Export the core configuration Tcl description by selecting the “Export Component Description (Tcl)” action on the right-click menu of the component in the Design Hierarchy.
3. Use the exported Tcl command to create the configured core in a regular Tcl script.

Note: The below set of cores cannot be configured using Tcl; the Export Component Description (Tcl) option is thus not supported:

- SmartFusion2/IGLOO2 MSS/HPMS component
- SmartFusion2/IGLOO2 System Builder component.
- RTG4 DDR memory controller with initialization (RTG4FDDRC_INIT)
- RTG4 High Speed Serial Interface 2 – EPCS and XAUI – with Initialization (NPSS_SERDES_IF_INIT)
- PolarFire SRAM (AHBLite and AXI) (PF_SRAM_AHBL_AXI)

4.3 Migration

While migrating a design from Libero SoC PolarFire v2.3 to Libero SoC v12.0, you may see warning messages about the availability of newer versions for PF_IOD and PF_LANECTRL cores. These warning messages can be ignored.

4.4 Simulation

When a core is configured using Tcl, if the value of the parameter FAMILY is not in sync with the family of the current project, incorrect files may be passed to simulation, resulting in simulation failures. This issue may occur if you export the Tcl description for a configured core in a project created with one family, and then use the same exported Tcl description to configure the core in Tcl in a project created with another family. This issue will be fixed in the upcoming Libero SoC 12.1 release, where the parameter FAMILY will no longer be exported to the exported Tcl description files of cores, and the Tcl will error out if a wrong value is specified for the parameter FAMILY.

4.5 SmartDesign

4.5.1 Modify Memory Map feature should not be used

The Modify Memory Map action used to connect peripherals to buses in the SmartDesign canvas should not be used in the Libero SoC v12.0 release. If used, Libero may crash or produce an incorrect/incomplete memory map.

4.6 Synthesis

4.6.1 MPF500T/TS/TL/TLS: encrypted blocks are limited to one top level module

To avoid Synthesis failures for Libero projects targeting the MPF500T device, ensure that each encrypted block in the design has exactly one top module. This issue also affects designs containing the Cortex-M1 IP core.

4.6.2 SynplifyPro mapping of sequential-shift to uSRAM does not support initial values

PolarFire devices do not support initial values on registers for Sequential-shift constructs mapped to uSRAMs. If an initial value is specified for a register in RTL, Synplify will ignore the value and issue a warning.

4.6.3 SynplifyPro version checking returns an error message on RHEL/CentOS 7.4

Checking the SynplifyPro version with the following command returns an error message:

```
synplify_pro -version -batch
```

```
Error creating '"Internal Error: unsupported format used in message: '
```

```
Error creating '"Internal Error: unsupported format used in message: '
```

```
N-2017.09M-SP1-1
```

Note: In Libero SoC, the dialog box where a Synthesis profile is added will display the same error message.

This error message can be safely ignored – these operating systems are supported by Libero SoC v12.0.

4.6.4 Standalone Synthesis Flow

Libero SoC v12.0 users may synthesize their design outside the Libero SoC software by using Synopsys SynplifyPro directly. When using this flow, the following additional steps are necessary to successfully synthesize and implement a design:

- Ensure that the <install location>/Designer/data/aPA5M/polarfire_syn_comps.v is passed to SynplifyPro. This file contains module declarations with timing information for PolarFire primitives not known to Synopsys.
- Many configured cores generate timing constraints. You must ensure that these constraint files are passed to synthesis for optimal results. These constraint files must also be imported into Libero along with the synthesis gate level netlist to get optimal place and route and timing analysis results. Core generate constraint files must be modified so that constraints are expressed using the proper hierarchical name of the configured cores in the top-level design

4.7 Netlist Viewer

Opening two or more views (for example, Hierarchical RTL View and Flattened Post-Compile View) in Netlist Viewer may result in a crash due to memory usage. Avoid opening multiple views for large designs.

4.8 PolarFire Block Flow

Libero SoC v12.0 supports Block Flow. The limitation is that only Fabric components (LUT, SLE, RAM, MATH) may be instantiated in a Block. All other components (CCC, DDR, etc.) must be part of the top level design, and cannot be instantiated in Blocks.

4.9 PolarFire Place and Route

- The Router will fail on designs which hit the architecture limit on locally routed row-globals.
Workaround: Eliminate the occurrence of locally routed row- globals by rerunning Synthesis/Compile with the option "Number of global nets that could be demoted to row-globals" set to '0'.
- The Router will fail on designs which reach the architecture limit on multiple gated locally routed row-globals (RGCLKINT) from the same source clock.
Workaround: Modify the RGCLKINT instances to chip-level GCLKINT instances in the source design.

4.10 SmartTime

4.10.1 Timing Data State for PolarFire Devices

For the Libero SoC v12.0 release, SmartTime and Timing Reports for all MPF300T/TS/TL/TLS devices show the Timing Data State as "Production". This is incorrect. Timing Data State is only "Production" for the MPF300T/TS-1 devices, at a nominal voltage of 1.0V. The Timing Data State for all other MPF300T/TS/TL/TLS devices is "Preliminary".

4.10.2 Timing Data State for RTG4 Device

For the Libero SoC v12.0 release, SmartTime and Timing Reports for the 1657 CG package, RTG4150L device show the Timing Data State as "Advanced." This is incorrect. The Timing Data State is "Production".

4.10.3 Incorrect slack for edge-shifted generated clocks

When an edge shift is specified on a generated clock, common clock period calculation for inter-clock domains with that clock may fail. In such cases, slack calculated for these inter-clock domains will be incorrect in the Max Timing Analysis Report.

4.11 IBIS Models

For PolarFire devices, the LVDS IBIS models have undesired swing in common model voltage, but the differential voltage is correct.

4.12 PolarFire SmartPower

4.12.1 Incorrect Power for PLL macros

Power for PLL macros is incorrectly displayed as zero in the Analysis Tab, even though the correct value is included in the total power calculation.

4.13 SSN Analyzer

For all PolarFire MPF300T/TS/TL/TLS -FCG1152 devices, SSN Analyzer simulated data deviates from the Silicon measured data. This deviation can be between 20%-60%.

4.14 Post-layout simulation fails in secure IP flow designs

SmartFusion2, IGLOO2, and RTG4 post-layout simulation fails due to incorrect _ba.v file generation.

4.15 Post-layout simulation is not supported for PolarFire

Post-layout simulation is not supported for PolarFire devices in the Libero SoC v12.0 release.

4.16 PolarFire Silicon Support Limitations

4.16.1 DDR3, DDR4, LPDDR3 and QDR Memories

- The Constraints Coverage report indicates some missing constraints; this can be ignored.
- Some designs containing DDR3, DDR4, or QDR memories may show timing violations on paths terminating at the HS_IO_CLK_PAUSE pin of the LANCTRL macro. If timing violations for this pin are seen, edit the SDC file to add a false path.
e.g.: `set_false_path -to [get_pins
PF_DDR3_0/DDRPHY_BLK_0/LANCTRL_ADDR_CMD_0/I_LANCTRL*/HS_IO_CLK_PAUSE]`
This issue will be resolved in future releases.
- The option "READ DBI enable" should be off for DDR4 and will be removed in future releases.
- The evaluation kit preset in DDR4 configurator does not update the value of the RTT_Nom parameter to the recommended setting. This will lead to failure on silicon. To avoid this, change the value of "ODT RTT Nominal Value" in the "Memory Initialization" tab of the DDR4 configurator to the recommended value, which is "RZQ/4".
- When exporting DDR configurations using the MSS External Memory DDR Controller Configurator (SmartFusion2 and IGLOO2 designs), the program attempting to export the configuration crashes.

4.16.2 DLL

- **Secondary Phase Restrictions Missing:** Although the user can specify values for Primary and Secondary phase with no restrictions, the Secondary Phase value cannot be lower than the Primary Phase value.
Workaround: Do not set the Secondary Phase value lower than the Primary Phase value.
- In DLL Phase Generation Mode, the secondary output clocks are not producing the correct phase in pre-synth HDL simulations.
Workaround: There is no workaround at this time.

4.16.3 PLL

- Only the post-VCO feedback mode is available in this release.
- Bypass option on output clocks is not available in this release.

4.16.4 PCIe

- During BFM simulation of the PCIe AXI interface (master or slave), the simulator may print warning messages about AHB signals, such as "HRESP". The warning message can be ignored.
- When the PCI Express Interface is configured in single lane mode (X1), the GUI incorrectly exposes the RXD and TXD ports for two lanes. The ports for the extra lane can be ignored.

4.16.5 Transceiver

- For the MPF300XT, MPF300TES, and MPF300TSES devices, the TX_ELEC_IDLE and TX_BYPASS_DATA signals are nonfunctional and must always be tied-off to "GND".

4.16.6 Transceiver Reference Clock

- Enabling on-die-termination, differential resistance and external VREF on the Transceiver Interface Reference Clock I/O is not supported in the I/O editor. However, these options can be set in the I/O PDC file.
- The connection from the Transceiver Interface Reference Clock I/O to the South-East PLL for all the reference clocks associated with Transceiver Interface Quad 0,2 and 4 lanes is missing in the software. Place and Route will fail if this connection is attempted.

4.16.7 IOD Generic Interfaces

- General Limitation: The IOD Generic Interface has only been characterized for the MPF300/T/TS device.
- The number of independent IOD interfaces that can be placed per edge is limited to 2. Users can place 3 IOD interfaces per edge, if at least two of the interfaces run at the same frequency. To accomplish this, in the IOD Generic Configurator, enable the option "Global clock from shared PLL" to share the HS_IO_CLK/RX_CLK_G signals from the PLL with the three interfaces.

4.16.8 IOD CDR

- The interface signals shown in the PolarFire IOD CDR configurator GUI are inconsistent with the signals shown in the SmartDesign component. The correct signals are those shown in the SmartDesign component. This issue will be fixed in the upcoming Libero SoC v12.1 release.
- You may see a crash on designs with PF_IOD_CDR instances, if the lane in which the CDR instance is placed has some unbounded IOs. This issue will be fixed in Libero SoC v12.1 release.

4.16.9 I/O's: SSTL15 On-Die Termination values are incorrectly programmed

For the MPF300XT/TES/TSES devices, when the ODT value for an SSTL15 I/O is selected as 20 Ohm or 30 Ohm, an incorrect setting is programmed

Workaround: Do not use the 20 or 30 Ohm on-die termination values for the affected devices.

4.17 Programming

4.17.1 Libero Programming

- The following error message is displayed when an sNVM client is not selected for programming:
"Exit -22 Bitstream or data is corrupted or noisy"

Workaround: Enable all sNVM clients for programming.

- The following error message is displayed when an authenticated/encrypted sNVM client is programmed in Libero:

"Exit -22: Bitstream or data is corrupted or noisy"

Workaround: Export a bitstream file or Export FlashPro Express Job and program the device outside of Libero using FlashPro Express, DirectC, or Auto Programming

- Updating the security or sNVM with a security-only bitstream or sNVM-only bitstream on a device that has the Fabric programmed will disable the Fabric.

If the Fabric has been disabled, you must reprogram the Fabric to enable it.

Workaround:

- sNVM only bitstreams: Field update bitstream files should always program the Fabric with sNVM.
 - Security only bitstreams: Security only bitstream should be used on a blank device only.
- When a device is programmed with a blank Silicon Signature field, it will not get erased.

Workaround:

- Specify a Silicon Signature that is not blank and program the device to change value.
 - Perform Erase program action to erase it.
- If the USERCODE which is part of the security segment is unspecified and the security is not programmed, the previous value of USERCODE will be retained. This issue will be fixed in the upcoming Libero SoC v12.1 release.
 - Programming Libero SoC v12.0 via SPI-Slave instead of JTAG is currently not supported. Support for this use model will be added in a future release.
 - Serialization is not working for SmartFusion2 and IGLOO2 in Libero SoC v12.0.

Serialization of the eNVM client is not working for Libero SoC v12.0.

Workaround: Use Libero SoC v11.9.

- FlashPro Express does not support SPI-Flash only programming in a JTAG chain with SmartFusion2/IGLOO2 and PolarFire devices.
- FlashPro5 programmer sometimes fails to be detected in FlashPro Express software on Linux machines.

Refer to [Microsemi SoftConsole v6.0 Release Notes](#) for more information and a workaround.

- The Configure Permanent Security setting crashes Libero when executed from TCL script (PolarFire).

Workaround: Use the GUI to set Configure Permanent Security.

- Serialization using PPD is not supported for SmartFusion2 and IGLOO2 devices.

Workaround: To use serialization, select the STAPL option when generating a job file for FlashPro Express.

4.17.2 SPI Flash Programming

This release includes the following limitations:

- Only the Micron SPI Flash is currently supported with the Evaluation Kit.
- This tool erases the SPI Flash prior to programming. It is recommended to program the SPI Flash with Libero SoC v12.0 prior to programming other data on the SPI Flash using non-Libero programming solutions.
- Partial update of the SPI Flash is currently not supported.
- It is not recommended to have huge gaps between clients in the SPI Flash, since gaps are currently programmed with 1's and will increase programming times.

The following table lists the ERASE, PROGRAM, and VERIFY/READ times for different client sizes. All times are in hh:mm:ss.

Note: Depending on the SPI-Flash memory silicon version, you may observe a shorter erase time.

| SPI Size | ERASE | PROGRAM | VERIFY/READ | TCK | Programmer |
|----------|----------|----------|-------------|-------|------------|
| 1 MB | 00:03:55 | 00:00:45 | 00:10:46 | 4MHz | FP5 |
| 1 MB | 00:03:55 | 00:00:28 | 00:10:05 | 15MHz | FP5 |
| 9 MB | 00:03:55 | 00:06:38 | 01:19:15 | 4MHz | FP5 |
| 9 MB | 00:03:55 | 00:04:26 | 01:08:49 | 10MHz | FP5 |
| 18 MB | 00:03:55 | 00:09:04 | 02:32:43 | 10MHz | FP5 |
| 128 MB | 00:03:55 | 00:58:38 | 22:07:55 | 15MHz | FP5 |

4.17.3 sNVM write fails due to ROM client created by previous design

In the scenario where a PolarFire device is first programmed with a design with an sNVM client, and then reprogrammed with a (different) design without an sNVM client, upon completion of programming with the second design, the sNVM client will not be erased. In such a case, if there are sNVM pages that are locked, writes to those pages will fail.

There is no programming action to erase the sNVM completely.

Workaround: Create a dummy sNVM client (filled with 0's) in the second design.

4.17.4 Zeroization Security warnings for MPF300XT/TES/TSES devices

For Libero SoC v12.0 projects targeting the MPF300XT/TES/TSES devices, while running the Export Bitstream or Export FlashPro Express Job step, unexpected zeroization security warnings are shown, even though zeroization is not supported on these devices. These warnings can be ignored and will be removed in the upcoming Libero SoC v12.1 release.

4.17.5 Polarfire VERIFY_DIGEST action may fail in certain cases

The VERIFY_DIGEST step in FlashPro Express for a PolarFire device in Libero SoC v12.0 release will fail in cases where the digest check is run for segments that are not programmed.

Workaround:

Using FlashPro v2.3 (part of Libero SoC PolarFire v2.3 or Programming and Debug Tools PolarFire v2.3), load the STAPL file into FlashPro, and deselect the digest checks for segments not programmed.

4.18 SmartDebug

4.18.1 General SmartDebug Limitations

- Initializing RAM blocks with random values in the Design Initialization Data and Memory tool will result in SmartDebug displaying incorrect values for zeroed memory blocks.
- The logical view cannot be reconstructed for:
 - LSRAM/uSRAM for port widths of x1 inferred through RTL.
 - LSRAM/uSRAM configurations when a single net of an output bus is used and others are unused. i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM. In this scenario, the memories can be read/write using physical view.
 - LSRAM/uSRAM configurations inferred using CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
 - HDL modules inferring RAM blocks that are instantiated in SmartDesign.

Workaround: There are no workarounds for the issues above at this time.

- Running Probe insertion from SmartDebug on an MPF500T device results in a tool crash. This issue will be fixed in the upcoming Libero SoC v12.1 release.

4.18.2 PolarFire Transceiver Support Limitations

- Optimize receiver on a Transceiver lane is disabled in SmartDebug. Receiver calibration (DFE) through SmartDebug is not supported in this release. The following Receiver calibration use cases are affected:
 - Transceiver lanes configured in DFE mode with XCVR universal workaround solution disabled
 - SmartBERT lanes configured to use DFE
 - Receiver change from CDR to DFE by modifying signal integrity parameters in SmartDebug

The PolarFire MPF100T/TS/TLS, MPF200T/TS/TLS, MPF300T/TS/TLS devices are affected by this issue.

- For PMA Native Mode: 12500 Mbps DFE, Optimize Receiver works as expected only on the third consecutive run when FlashPro4 is used. The following shows the behavior on each Optimize Receiver run:
 1. First Optimize Receiver run after UWA calibration request (IDCode verify failed in SmartDebug)
After this step, RxReady and RxValid went low.
 2. Second Optimize Receiver run (RxReady & RxValid unexpected output)
 3. Third Optimize Receiver run (expected RxReady and RxValid outputs)

On the third step, the User Calibration Request and Optimize Receiver works as expected in any sequence triggered one after another on completion.

- Plot Eye introduces a burst of errors in data traffic on Transceiver Interface lanes when started. This will be fixed in an upcoming Libero SoC PolarFire release.
Workaround: Enable Eye Monitor using the Power On Eye Monitor option before starting the traffic. This will power on the DFE and EM receivers in CDR mode and no spurious errors will be seen during eye plot.
- The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.
Workaround: Perform the following steps to obtain the expected eye output:
 1. Assert PCS RX RESET
 2. Optimize DFE
 3. Plot Eye
 4. De-Assert PCS RX RESET
- The SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- SmartBERT IP PRBS tests take more time to start/stop/inject error on RHEL 7.x and Cent OS 7.x platforms as compared to RHEL 6.x and Windows OS. This issue is seen only with PRBS patterns from the SmartBERT IP, and will be fixed in upcoming Libero SoC release.
- During the Static Pattern Transmit operation, the Receiver PLL (RX PLL) does not lock to the max run length pattern when looped back from TX to RX.
- SmartBERT IP PRBS tests do not work when the first Transceiver lane uses an internal pattern (PRBS from XCVR PMA) and the following lane uses a SmartBERT pattern (PRBS from SmartBERT IP).
- When multiple lanes are specified for DFE Calibration through SmartDebug, the optimize_receiver Tcl command will fail if RX_CTLE (from read back flow) is not found for any of the lanes. This will result in incomplete calibration of other lanes.
- The Power ON eye monitor Tcl command (eye_monitor_power) does not work correctly in Libero SoC v12.0. The Receive PLL does not lock to the incoming data after this Tcl command is run. This will be fixed in an upcoming Libero SoC release.
Workaround: There are no workarounds for the issues above at this time.
- If Start Plot Eye is started on a lane when data is coming from an external source, clicking Stop Plot Eye will result in a SmartDebug crash.

4.18.3 PolarFire Signal Integrity Support Limitations

- The RX Polarity Signal Integrity parameter (Polarity P/N reversal) has no effect when a PDC file is imported using the Import option in SmartDebug. This flow works without errors in GUI mode. This will be fixed in an upcoming Libero SoC release.
- When the TX amplitude and RX CTLE parameters are changed in the SmartDebug Signal Integrity tab, BMR (Burst Mode Receiver) designs will fail to work.

4.18.4 PolarFire FPGA Hardware Breakpoint (FHB) Limitations

- FHB is not supported when a Transceiver Interface with the Enhanced Receiver Management Solution enabled is used in a design.

4.18.5 RTG4 FPGA Hardware Breakpoint (FHB) Limitations

- For designs that instantiate certain macros in HDL, Synthesis fails during FHB auto-instantiation. For example, Synthesis fails for FHB auto-instantiation flow for designs where FCCC modules are instantiated in RTL files.
- Live Probe channel assignment using a static signal (connected to GND) halts the DUT. If this occurs, initiate the Soft Reset operation using the FHB UI to restart the DUT.

- Halting a clock domain driven by a CCC will also halt all clock domains that are driven by all the CCCs in the design. This is silicon limitation.
- FHB is not supported for cascaded CCC's (CCC's that rely on other CCC outputs to source the reference/feedback clocks)

4.18.6 Standalone SmartDebug Limitations

- Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug. In addition, the ID code of Microsemi devices cannot be read in this scenario.
Workaround: Use SmartDebug through the Libero flow to perform these operations.
- Programming fails for RTG4 devices when a standalone SmartDebug project is created using the "Construct Chain Automatically" option, and a DDC file is imported in the Programming Connectivity and Interface dialog.

Workaround:

1. Close and reopen the Programming Connectivity and Interface UI and then click **Run Program Action**.
2. Create a project by importing the DDC file (without Auto-construct).

4.19 Secure Production Programming Solution

4.19.1 SPPS: New JDC file need to be generated if eNVM is set to be protected by passkey, using pre-v12.0 Libero SoC

eNVM update protection with FlashLock is not supported. eNVM update is protected by User Encryption Keys (UEK1, UEK2 or UEK3).

Regenerate the JDC file without eNVM FlashLock Protection enable.

4.19.2 SPPS: Job Manager crashes when opening an existing Job Manager project from v11.9

Job Manager v12.0 does not support Job Manager project files created with releases prior to v12.0.

4.19.3 SPPS: Job Manager does not support PolarFire DAT export

PolarFire DAT file bitstream export from Job Manager is not supported in Libero SoC v12.0.

4.19.4 SPPS: SmartFusion2/IGLOO2: eNVM update protection with FlashLock is no longer supported

Due to a silicon limitation, eNVM update protection with FlashLock has been defeatured. If a JDC file generated with a pre-12.0 version of Libero SoC had the eNVM set to be protected by passkey, it must be regenerated with Libero SoC v12.0 without eNVM FlashLock Protection enabled. eNVM update protection continues to be provided by User Encryption Keys (UEK1, UEK2 or UEK3).

4.19.5 ERASE Action failure for FlashPro Express Job

If a HSM FlashPro Express job has tickets for PROGRAM and ERASE actions, without a ticket for the VERIFY action, the ERASE action will fail. To successfully run the ERASE action, ensure that a ticket for the VERIFY action is included. This issue will be fixed in the upcoming Libero SoC v12.1 release.

4.20 Identify Instrumentor may hang on some Windows 10 machines

When the Identify Instrumentor is opened in Integrated mode on certain machines, the tool opens, but, upon interaction, it freezes. This is an isolated issue, and happens on rare Windows 10 OS configurations.

Workaround: Use the Standalone Identify Instrumentor.

4.21 Installation and System Limitations

4.21.1 Libero does not run on 8TB File Systems

Libero is currently only supported for partitions 2TB or smaller. If either the Libero install or the Libero project is located on a partition that is larger than 2TB, file access errors or tool crashes may occur. Support for larger partitions is expected to be added in an upcoming release.

4.21.2 4K and 8K screens are not supported

4K and 8K screens are not supported in the Libero SoC v12.0 release.

4.21.3 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

4.21.4 Visual C++ Redistributable Installation Error

On some machines, the installer may display a message stating:

“The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?”

The above error message is benign. If it is seen, click Yes and Libero SoC v12.0 will be installed successfully.

4.21.5 Installation on Windows 7

During Libero SoC v12.0 installation on Windows 7 machines, you may see pop-up warning messages about shortcuts toward the end of installation process.

These messages can be safely ignored. Click OK to close the pop-up windows and the installation will proceed and complete as expected. All Windows shortcuts will appear correctly.

4.21.6 Installation fails when there is insufficient space

In Libero SoC v12.0, the web installer quits without any user notification or error message when there is insufficient space for the installation. In addition, the estimated space for the installation is incorrect – it reads as approximately 236MB required. Ensure that there is at least 20GB free space on the target hard drive before invoking the installer.

The DVD installer will also not proceed if there is insufficient space.

4.21.7 Windows Standalone Installer: Spaces in Extraction Path

During installation of the standalone (DVD) version, the folder to which the zip file is extracted must not contain spaces. If spaces are present, invocation of the installer will fail with the error *"Windows cannot find '<truncated path to extracted folder>'". Make sure you typed the name correctly, and then try again"*. Rename and/or move the extracted folder to one without spaces (in the entire path).

4.21.8 Linux Package Note

In Libero SoC v12.0, the script `bin/check_linux_req/check_linux_req.sh` incorrectly reports that the Linux package `xz.i686` is required for RHEL/CentOS 7.x. Package `xz.i686` is not required. The correct required packages are `xz-libs.x86_64` and `xz-libs.i686`.

4.21.9 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC PolarFire successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC v12.0, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

5 System Requirements

The Libero SoC v12.0 release has the following system requirements:

- 64-bit OS
 - Windows 7, Windows 8.1, or Windows 10 OS
 - RHEL 6.6 or later, RHEL 7, CentOS 6.6 or later, or CentOS 7.0-7.5
- A minimum of 16 GB RAM

Note: Setup instructions for using Libero SoC v12.0 on Red Hat Enterprise Linux OS or CentOS are available [here](#). As noted in that document, installation now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

6 Download Libero SoC v12.0 Software

The following are available for download:

- [Libero SoC v12.0 for Linux](#)
- [Libero SoC v12.0 for Windows](#)
- [Libero SoC v12.0 MegaVault](#)

Note: Installation requires administrative privileges.

After successful installation, clicking **Help-> About Libero** will show Version: 12.500.0.22