RTG4 Fabric DDR Controller Testing Report

LBNL Oct 3rd 2018

Nadia Rezzak, J.J. Wang, Paco Mok, Marco Cheung

November 15th, 2018

SUMMARY

The report presents the testing results of Heavy Ion induced failures on the FDDR Controller block on Microsemi's RTG4 FPGA.

The design exhibited a lock up behavior or SEFI where the FDDRC was unable to recover normal functionality without a reset being issued to the FDDRC and the respective FSMs controlling the transactions. The second error mechanism identified was a single read data error which is flagged when the return (read data) is not equal to the expected data. Finally, the third error mechanism identified was a single write data error which is flagged when the write is not equal to the expected data.

I. TEST OBJECTIVE

The objective of this test is to obtain Heavy Ion induced SEE data on the Fabric DDR Controller (FDDRC) on Microsemi's RTG4 FPGA.

II. DEVICE UNDER TEST

The test was performed at the Berkley National Laboratory. Table 1 lists facility and Device under test (DUT) parameters.

Table 1. Heavy Ion Testing Parameters

Condition	**Setting**
Beam Energy	10 MeV/Nucleon
Temperature	Room Temperature
Bias	1.2V, 2.5V & 3.3V
Sample Preparation	Reworked RTG4 evaluation board with a back grinded RTG4 Rev C unit (production version).

III. TEST METHODS

This test generally follows the guidelines of two SEE testing standards: ASTM standard F1192M-95, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation on Semiconductor Devices," and JEDEC standard JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

A. Irradiation

The test was performed at the Berkley National Laboratory. Table II lists the Ions tested and their respective LETs.

Table 2. Species Tested & Adjusted LETs

Species & Tilt	**LET**
O – (0)	2.19
Si – (0)	6.09
V – (0)	14.59
Cu – (0)	21.17
Kr – (0)	30.86

B. DUT Design

The design instantiates the FDDR controller provided in the RTG4 Microsemi Catalog (with initialization). The transactions to and from the FDDR controller are handled through the AXI interface (refer to Microsemi Demo Guide dg0625 https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/rtg4-development-kit#documents)

The circuits under test include the following. Refer to dg0625 for more details

1. FDDRC_With_INIT
2. AXI_IF
3. FSMs responsible for Data Comparison (User Defined)

The demo design is modified to isolate the circuits under test mentioned above. Additional logic blocks were moved to the master FPGA to facilitate remote user interaction and data collection.

C. Experimental Setup and Procedure

Figure 1 below shows the FDDR controller testing hardware setup block schematic.

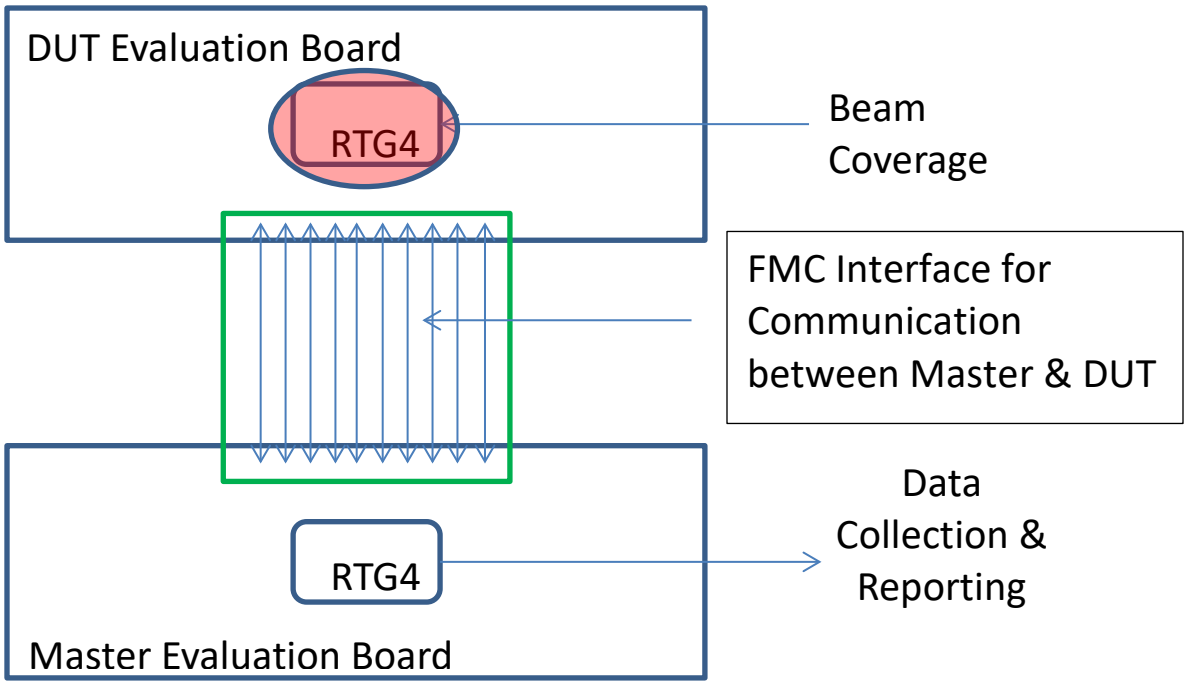

Figure. 1. Hardware block level schematic

FDDR Controller Test Flow:

The Master FSMs will write the entire memory space, followed by reading and comparing. If a single event error is detected, the FSM will log the error and rewrite the entire memory.

If a SEFI event occurs, we will stop the beam and issue resets to recover the controller. In the event that the reset does not work, a power recycle will be applied. In this test no power cycle was required, as all SEFI events were fixed with issuing resets.

The following is a test flow for testing the FDDR controller:

1. Master controller fills DRAM with DATA = ADDRESS
2. Master controller reads and compares data with the address in sequence through the entire memory space.
3. Once the reading and writing is in progress the radiation beam is turned on.
4. If an error is detected the counter increments and the state machine reverts back to the fill state. This type of error is registered when the return value of the read data does not equal the address (bad/corrupt data)
5. Each memory address is read 3 times, the following determines what type of error:
    a. All 3 reads expected – pass
    b. All 3 reads different from expected but the readback values are all same – write error
    c. Any of the 3 reads different from expected but not the same with each other – read error
6. If the operation locks up at any point, the beam will be stopped and resets will be issued by the user to reinitialize the test.
    a. When a lock up (SEFI) behavior is observed, the beam will be stopped immediately and a SEFI event will be recorded.

A testing flow chart is provided in Figure 2.

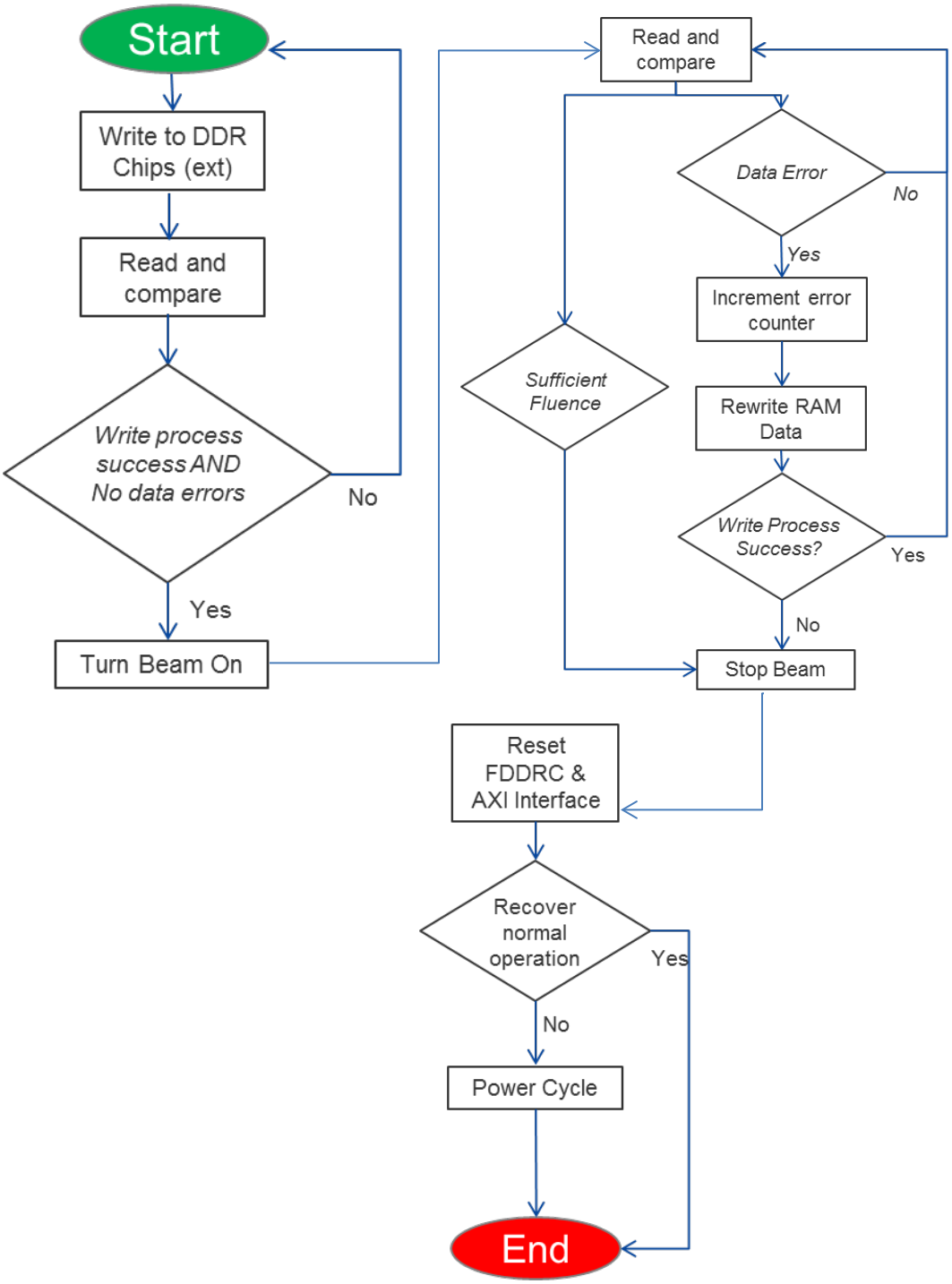

Figure. 2. FDDRC Testing flow chart

IV. Results and Discussions

The design exhibited lock up behavior at all LET's tested. Figure 3 shows the LET vs. cross section curve of this SEFI. Single data errors were also observed when the design did not lock up. The cross section is displayed in Figure 3 below. Single data errors refer to the error signature when the return data is not equal to the expected data for both Read and Write operations. Note that the DDR memory chips are not irradiated, therefore this data corruption/mismatch is expected to be an error in the read or write operation performed by the controller.

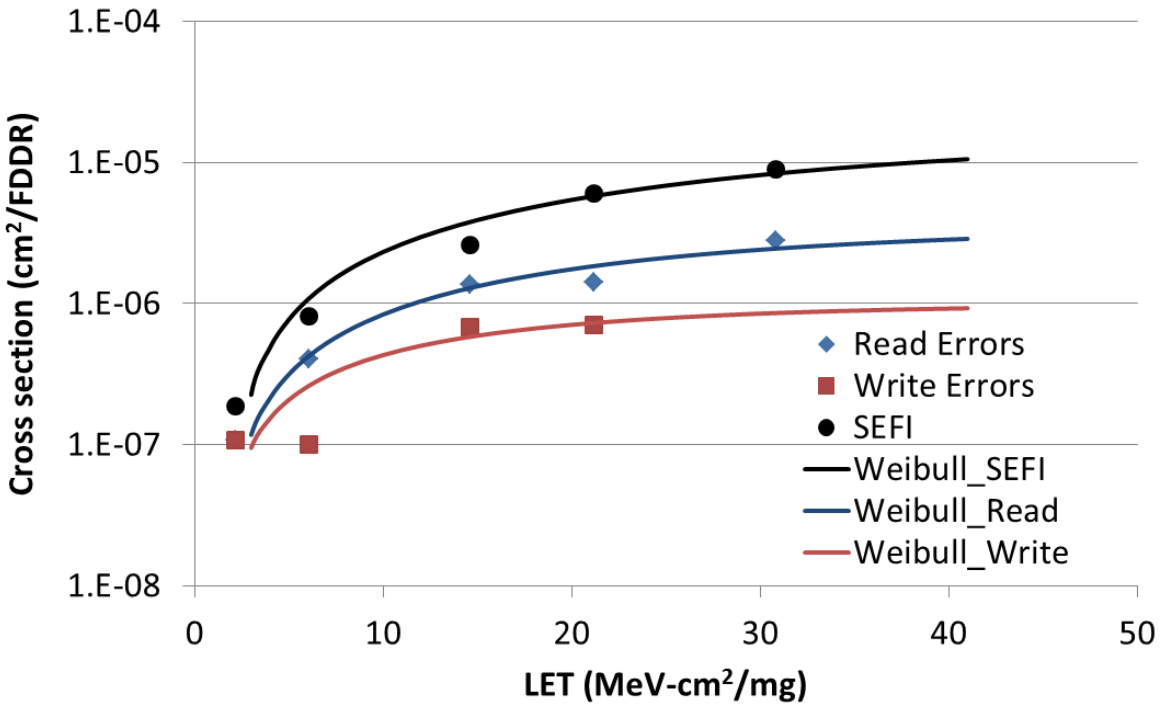

Figure. 3. FDDRC SEFI, Read and Write error cross sections and Weibull fit

Table 3. SEFI Weibull Parameters

L0	W	S	A0
0.9	40	1.2	1.70E-05

Table 4. Read Errors Weibull Parameters

L0	W	S	A0
0.5	25	1.2	3.5E-06

Table 5. Write Errors Weibull Parameters

L0	W	S	A0
0.5	15	1	1.00E-06

Table 6 below summarizes the fluence tested at each LET and the number of errors observed for each failure mode (read errors, write errors and SEFI).

Table 6. Error summary and cross section (XS)

LET	Fluence	Read Errors	Write Errors	SEFI	Read XS	Write XS	SEFI
2.9	3.73E+07	4	4	7	1.07E-07	1.07E-07	1.88E-07
6.09	9.9E+06	4	1	8	4.04E-07	1.01E-07	8.08E-07
14.59	8.82E+06	12	6	23	1.36E-06	6.80E-07	2.61E-06
21.17	2.83E+06	4	2	17	1.41E-06	7.06E-07	6.00E-06
30.86	1.79E+06	5	0	16	2.80E-06	0.00E+00	8.95E-06

V. ORBITAL UPSET RATE

The Weibull fit parameters in Tables 3, 4 and 5 are used to calculate the orbital upset rates in GEO synchronous orbit solar min, 100 Mil aluminum shielding.

Table 7. Orbital Upset Rates

Error Mode	**GEO Solar Min Orbital Upset Rate**
Read Errors	3.41E-5 upset/bit-day
Write Errors	2.29E-5 upset/bit-day
SEFI	7.85E-5 upset/device-day