A Fault Tolerant PMAD System Using Radiation Hardened Highly Integrated AFE Circuits
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Agenda

- PMAD topology
- Fault Tolerant Power Stage
- LX7720 as analog front-end for DC/DC conversion
- LX7712 as power line protection for PMAD
- Control aspects
PMAD Topology
Power Management and Distribution

- Optimally transfers power from input sources, manages transmission of power to loads

- Consists of DC/DC converters, protection circuits, power transfer and fault management

- Inputs assumed as PV strings with fast MPPT control to track
  - Varying angle
  - Shading
  - Temperature per spring
PMAD Topology
Sensing, Drive and Control

- Voltages on input and output nodes and currents in each converter are sensed

- Loop control if done digitally
  - AFE converts to digital all sense lines + drives MOSFETs from PWM inputs
  - FPGA implements
    - DC/DC loop
    - MPPT
    - Power and safety management

- Power Distribution and Bus Protection implemented
## Power stage

- DC/DC units implemented using
  - 2 High-Side NMOS in series
  - 2 Low-Side NMOS in series
    - + Allows for FET short protection
    - - Efficiency penalty

- Regular switching Mid FETs – M22 M23

- Health Monitoring by exercising upper and Lower FETs – M21 and M24

- Shoot through current or inductor current detect to signal Fault

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**Upper – Lower FETs Health Monitor**

**Shoot-Through, Inductor current sense By AFE**

**Mid FET – PWM Switching by AFE**

**Power stage from Another PV string**
Power stage fault simulation

- Fault detect waveforms with 5 Ohms faults
  - on M14/M24
  - on M11/M21
- Criteria in this case:
  “If the change in average current during the test switching cycle is higher than 0.5A then tested device is developing a short.”

Note: Inductor current is almost unaffected (same for output and input voltages)
For Synchronous Boost in CCM: if \( dt_1 \) and \( dt_2 \) are too large they impact efficiency so \( dt_1,2 \) should be minimized.

If \( dt_1 \) and \( dt_2 \) are negative then a large shoot through current will reduce efficiency.

There is a maximum efficiency point.
Dead time simple model cont.

- For $dt > 0$ degradation is sub percent for 100V output.
- Efficiency degrades most when $dt$ is negative (there is shoot through current).

$$
\eta \approx 1 - \frac{V_{out}^2}{R_{short}} \frac{|dt|}{V_{out}^2} \frac{R_{load}}{R_{short}} = 1 - \frac{|dt|}{T} \times \frac{R_{load}}{R_{short}}
$$

For example for $dt=-1$ns, $T=10$us, $R_{load}=300\Omega$, $R_{short}=0.3\Omega \Rightarrow 1-\eta=10\%$

- Traditional design: dead time is insured based on margining worst case delays + jitter between driver chain for each MOSFET
- Our topology can sense the effect of dead time drift due to temperature, aging or radiation so it can continuously optimize efficiency and keep $dt$ minimum
LX7720 Power Driver with Current Sensing Highlights and Applications

- Space System Manager – Motor Control – Power Management
- Motor driver Servo Control
- Linear actuator servo control
- Stepper, BLDC, PMSM motor driver
- DC/DC
- Power drivers up to 150V
- In-line Current Sense with embedded converters
- 132-lead ceramic Quad Flat Pack package - 24mmx24mm
LX7720 Power Driver with Current Sensing Features

- Four Half-Bridge Nch MOSFET drivers
- Four floating differential current sensors with ΣΔmodulated processed outputs to FPGA
- Pulse density modulated resolver exciter
- Three differential resolver sensors with ΣΔmodulated processed outputs to FPGA
- Six threshold configurable logic inputs
- Ground isolation signal-to-motor
- Six bi-level logic inputs
- Fault detection
- Radiation Tolerant
  - SEL free – 87MeV-cm²/mg
  - 100krad TID
  - ELDRS tested up to 50krads
LX7720 Power Drivers

- There are 4 half bridge drivers
- Upper driver is floating N ch MOSFET
- Supports power rails up to 150V
- Switching frequency to 200kHz
- Supports 100% duty cycle for upper or lower switches.
- Bootstrap option for powering upper driver also supported
- Long term shoot through prevention
LX7720 Floating Current Sense

- Capable of sensing current at the switch pin; this gives a true indication of coil current.
- Senses a +/-250mV differential analog signal. Rejects a common mode signal of 150Vpk changing at a rate of 15KV/us.
- Single line sigma delta data stream output to FPGA
- 2nd order sigma delta modulator at 32MHz
- Provides OC fault detection for levels exceeding 300mV
LX7720 Radiation testing schedule

- Preliminary 100krad test performed at DMEA in May 2018
- Final 100krad test under way. Data will be presented at NSREC
- 100krad test of qual lot to be completed in November 2018
- 50krad ELDRS to be completed in February 2019
- SEE testing scheduled for end of June, data will be presented at RADECS
Preliminary 100krad results:

- No significant shifts observed on the following parameters:
  - Current consumption
  - Reference voltage
  - Fault thresholds
  - Bi-level inputs and logic I/O parameters
  - ADC gain
- Small increase, 5-10%, in the MOSFET and DMOD drivers impedance
- Small degradation of ADC offset (<0.15%FSR)
LX7712 Power Line Protector Device Highlights and Applications

- Used for power control and distribution
- Provides a protected integrated switch
- Turns on and off DC load with current of up to 5A
- Latch-able current limit protection
- Fold-back current limit protection
- Can be paralleled for higher currents
- 48-lead hermetic HTF flatpack package - 19mmx19mm

- ESA Standards:
  - ECSS-E-HB-20-20A: Electrical design and interface requirements for power supply
  - ECSS-E-ST-20-20C: Guidelines for electrical design and interface requirements for power supply
LX7712 Power Line Protector Device Features

- Internal 5A PMOS switch and catch diode
- 120V rated
- LCL or FCL configurable
- ON, OFF, and STATUS pins
- Programmable UVLO and current levels
- Current monitor output
- Current slew rate control: on and off
- Programmable timer
- Optional hiccup restart mode
- Temperature shutdown - optional
- Radiation Tolerant
  - SEL free – 87Mev-cm2/mg
  - 100krad TID
  - ELDRS tested up to 50krads
LX7712 Power Line Protector Device Classification as LCL, HLCL & RLCL

Maximum Safe Operating Curve

- **RLCL 2B**: (38V, 2.2-2.8A, 10-20ms)
- **RLCL 2**: (52V, 2.2-2.8A, 4-8ms)
- **LCL 4**: (38V, 4.4-5.6A, 6-12ms)
- **LCL 4B**: (52V, 4.4-5.6A, 4-8ms)
- **HLCL 4**: (38V, 4.4-5.6A, 0.5-2ms)
- **HLCL 4**: (52V, 4.4-5.6A, 0.5-2ms)

Note: for LCL and HLCL classification the max current limit needs to be set between 4.4-5A for LX7712
DC/DC control

- Fast loop / slow loop approach
  - Fast loop implements a PID controller for each of the two boost DC/DC converters served by each LX7720
    - PID controller at switching frequency regulates voltage across the input PV string to a target voltage by controlling the duty cycle, bandwidth 5-10x switching frequency.
    - Power stage SOA sensing can overwrite the target
  - Slow loop is an integral controller updating the target voltage of the fast loop in order to optimize the input power (MPPT), bandwidth 100x switching frequency (1kHz)
    - Simple “perturb and observe” or more complex (see paper references)
Dead time control

- Dead time (dt) optimization (and redundant fault monitoring) is running at a much slower pace than slow loop (e.g. 1Hz)
- Optimization based on perturb and observe method using the fact that the only observable degradation is at negative dt.

1. Start from A and test B and C
   - If C >> A ≈ B stay in A
   - If C >> A >> B move to B
   - If C ≈ A ≈ B move to C
   - If C < A or A < B error, set conservative dt

2. Repeat 1.
Dead time loop modeling

- Modeled dead time adjustment control and a delay mismatch temperature model to verify operation.

- Simulation: response to thermal cycles.

  - Dead time adjustments are done at the level of the PWMs driving the higher and lower MOSFETs
  - PWM delay resolution is 5ns
  - Dead time adjust is the extra delay added to the nominal rising edge of the upper MOSFET gate driver.
  - Dead time error is the difference between ideal dead time adjust and current dead time
  - Initial safe dead time adjustment is 125ns
Experimental data

- LX7720 motor control evaluation

- Modification to evaluate the new power stage

Two half bridge circuits reconnected

4MOSFETs to emulate new power stage
In a conservative design to margin for TID and temperature variation of the 7720 and MOSFETs dt is set to 1.2us.

If we want duty cycle up to 10% then dt margin is maximum 5% => Tsw = 24us

If we use dt control with a step of 5ns then dt becomes negligible

the new limiting factor will be the gate driver minimum pulse width (~500ns) and Tsw=5us.

=> 5x higher switching frequency possible with dt control.
Conclusions and future work

In this presentation we have shown:

- A new PMAD topology
- A 4-MOSFET Fault Tolerant Power Stage
- How to use LX7720 as analog front-end for DC/DC conversion using the fault tolerant power stage
- How to apply LX7712 as power line protection for this particular PMAD
- Details of the system control aspects:
  - How to detect faults and switch to redundant system
  - How to constantly optimize deadtime and be tolerant to parametric shift of MOSFET control delay
Conclusions and future work

- Future integration in an application/evaluation board once the LX7712 is available.
- System verification:
  - Emulate
    - loads and load faults using programmable loads
    - sources by using a PV simulator
  - Use an NI box to control the sources and loads and measure performance, behavior and fault tolerance
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