UG0845
User Guide
Median Filter v4.1

a MICROCHIP company

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 (Published in November 2018) is the first publication of this document.

2 Introduction

The median filter is a nonlinear digital filtering technique, often used to remove glitches from an analog signal.

2.1 Key Features

The median filter IP block supports the following features:

- Finds the median of a set of input samples
- Variable window size (5,7,9)

2.2 Supported Families

The median filter IP block supports the following families:

- SmartFusion®2
- IGLOO®2
- RTG4™

2.3 Theory of Operation

The median filter is used to remove the noise from a signal. It forms a window of N (this IP supports N=5, 7, and 9) adjacent samples and finds the median of these samples.

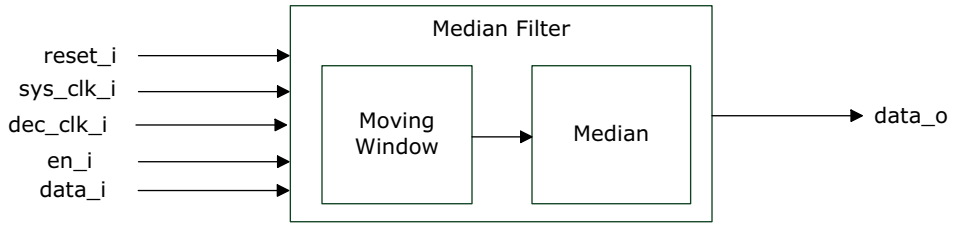
Examples:

- If N = 9 and {15,13,25,18,35,46,61,26,9} is a set of input samples, then median will be 25
- If N = 7 and {12,11,27,19,9,6,3} is a set of input samples, then median will be 11
- If N = 5 and {15,15,12,11,10} is a set of input samples, then median will be 12

3 Hardware Implementation

The following figure shows the block diagram of the median filter.

Figure 1 • **System-Level Block Diagram of Hardware Implementation**



3.1 Submodules

The median filter IP has two submodules.

3.1.1 Moving Window

The input data is sampled at every rising edge of dec_clk_i. This submodule takes the input samples and creates windows of fixed length (5 or 7 or 9 samples each). The window size depends on the configuration parameter g_WINDOW_SIZE. If we consider g_WINDOW_SIZE as 7, then {1st, 2nd, 3rd, 4th, 5th, 6th, 7th} samples will form a window, {2nd, 3rd, 4th, 5th, 6th, 7th, 8th} samples will form the next window and so on. These windows are connected as the input to median submodule.

After the reset signal is de-asserted, the window will have all zeros. The input data_i is sampled at rising edge of dec_clk_i.

3.1.2 Median

The median submodule finds the median value of each window and gives it as the output. At every rising edge of dec_clk_i the median output is updated.

3.2 Inputs and Outputs

The following table describes the input and output ports of the median filter block.

Table 1 • **Inputs and Outputs of Median Filter Block**

Signal Name	Direction	Width	Description
reset_i	Input	1 bit	Active low asynchronous reset signal to design
sys_clk_i	Input	1 bit	System clock
dec_clk_i	Input	1 bit	Decimated clock input - data is sampled at the rising edge of this signal
en_i	Input	1 bit	Enable signal
data_i	Input	g_DATA_WIDTH bits	Data input
data_o	Output	g_DATA_WIDTH bits	Median data output

3.3 Configuration Parameters

The following table describes the configuration parameters used in the hardware implementation of the median filter. These are generic parameters and can be varied as per the application requirements.

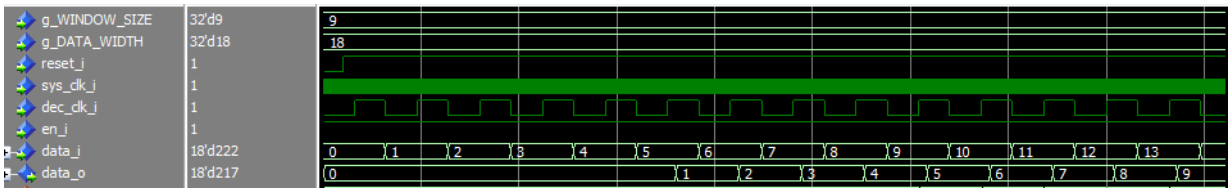
Table 2 • **Configuration Parameters**

Name	Range	Description
g_WINDOW_SIZE	5, 7, 9	Describes the size of the window
g_DATA_WIDTH		Describes the input and output data width

3.4 Timing Diagram

The following figure shows the timing diagram of the median filter block. The timing diagram represents a typical use case of the median filter block.

Figure 2 • **Timing Diagram**



After the reset signal is de-asserted, the window will have all zeros. The first input sample will enter the window at the first rising edge of dec_clk_i, the second sample will enter the window at the second rising edge of dec_clk_i and so on.

For the timing diagram shown in the above-mentioned figure, after the reset signal is de-asserted, the window will be {0,0,0,0,0,0,0,0,0}

At first rising edge of dec_clk_i , data_i is 0, the window will be{0,0,0,0,0,0,0,0,0}

At second rising edge of dec_clk_i,data_i is 1,the window will be{0,0,0,0,0,0,0,0,1}

At third rising edge of dec_clk_i,data_i is 2,the window will be{0,0,0,0,0,0,0,1,2}

and so on.

3.5 Resource Utilization

The following table lists the resource utilization of the median filter block after synthesis.

Table 3 • **Resource Utilization for g_WINDOW_SIZE = 5 and g_DATA_WIDTH = 18**

Resource	Count
LUTs	640
DFF	240
MACC	0
RAM1kx18	0
RAM64x18	0

Table 4 • **Resource Utilization for g_WINDOW_SIZE = 7 and g_DATA_WIDTH = 18**

Resource	Count
LUTs	1130
DFF	320
MACC	0
RAM1kx18	0
RAM64x18	

Table 5 • **Resource Utilization for g_WINDOW_SIZE = 9 and g_DATA_WIDTH = 18**

Resource	Count
LUTs	1480
DFF	390
MACC	0
RAM1kx18	0
RAM64x18	0