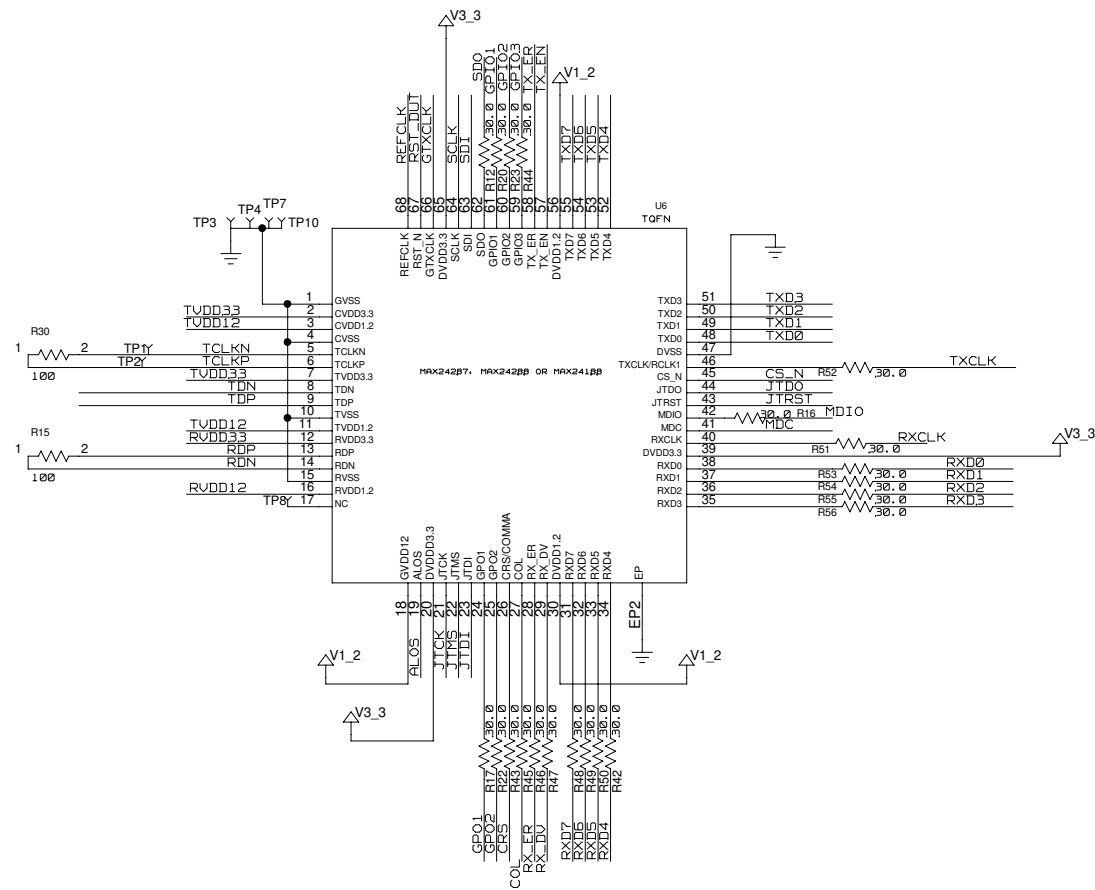


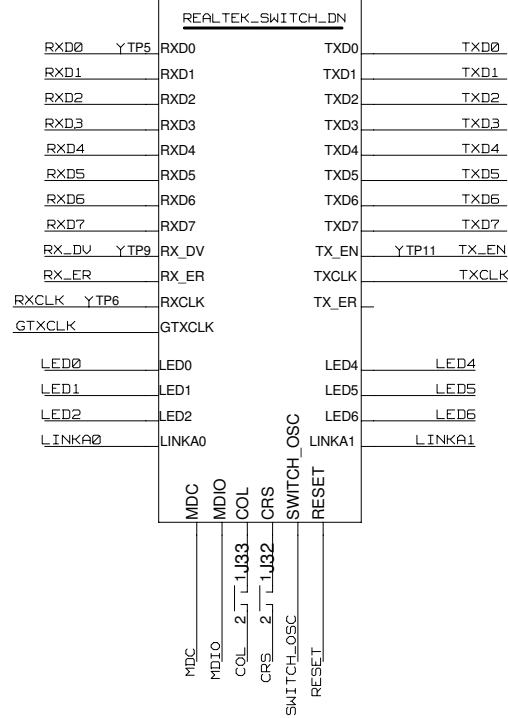
# MAX24287 EVKIT Rev\_B



Top level Hierarchy block

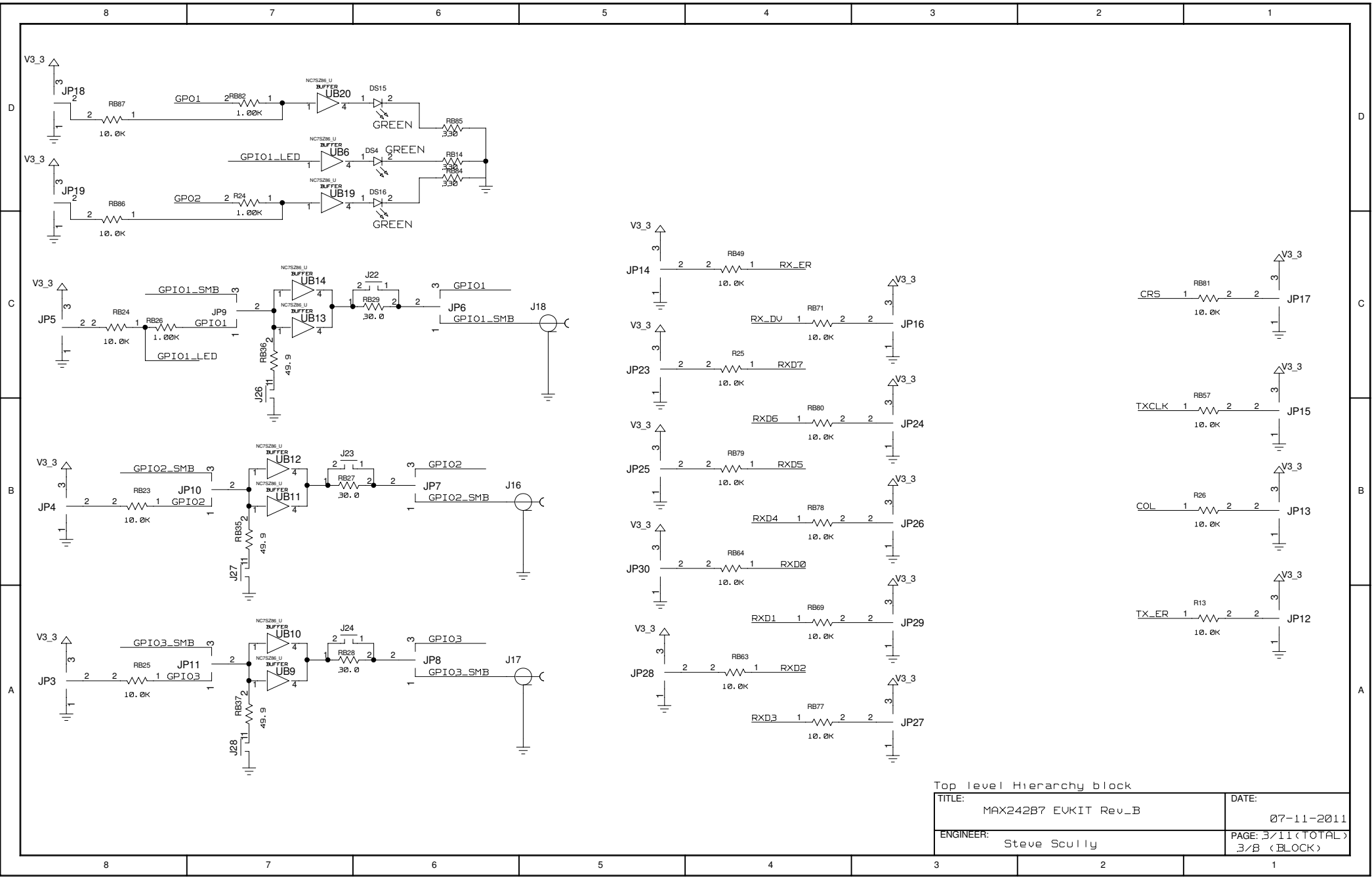
TITLE: MAX24287 EVKIT Rev_B	DATE: 07-11-2011
ENGINEER: Steve Scully	PAGE: 1/1 (TOTAL) 1/B (BLOCK)

Switch Hierarchy block.  
 Contents on page 9



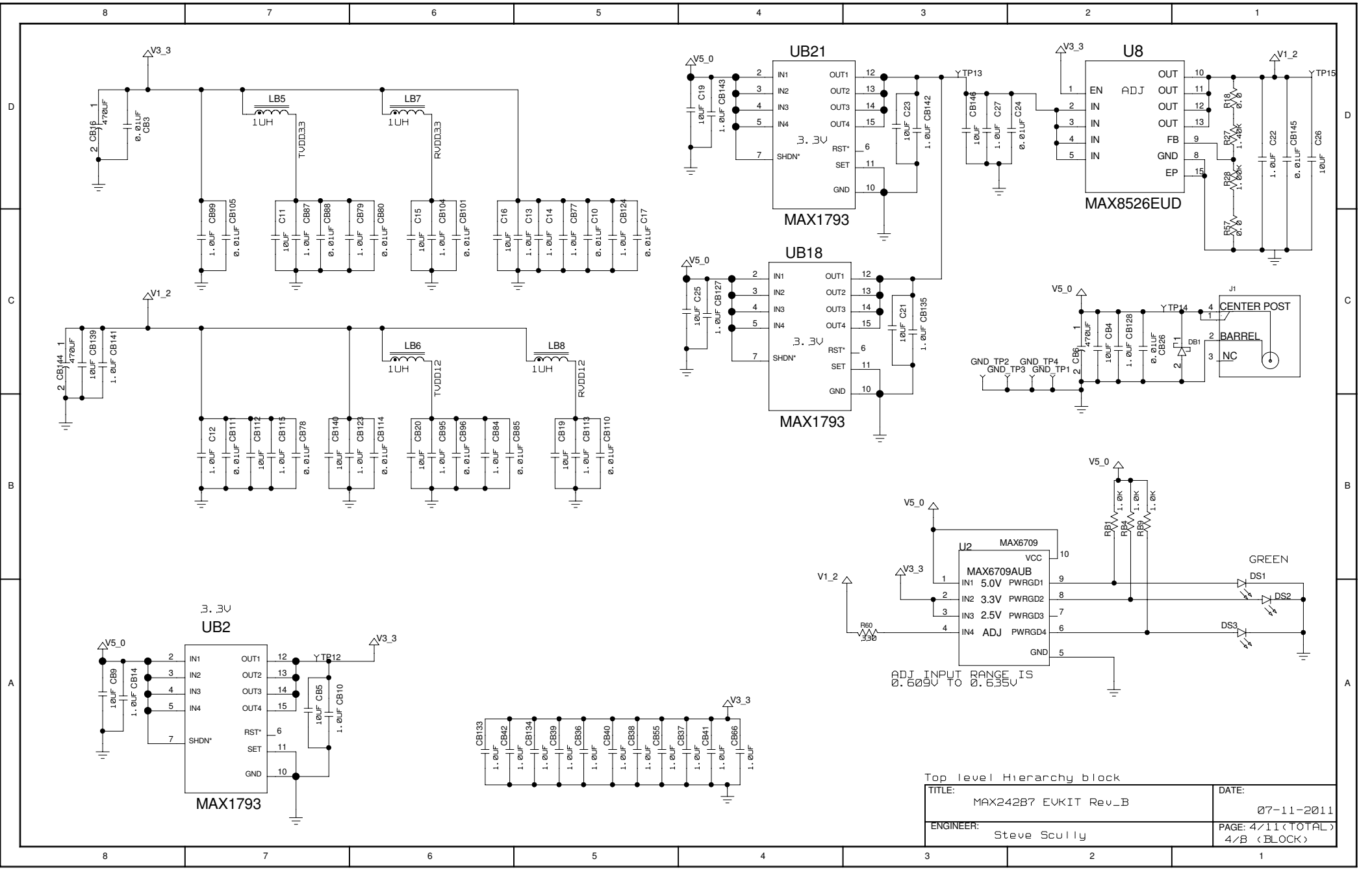
Top level Hierarchy block

TITLE: MAX24287 EVKIT Rev_B		DATE: 07-11-2011
ENGINEER: Steve Scully		PAGE: 2/11 (TOTAL) 2/B (BLOCK)



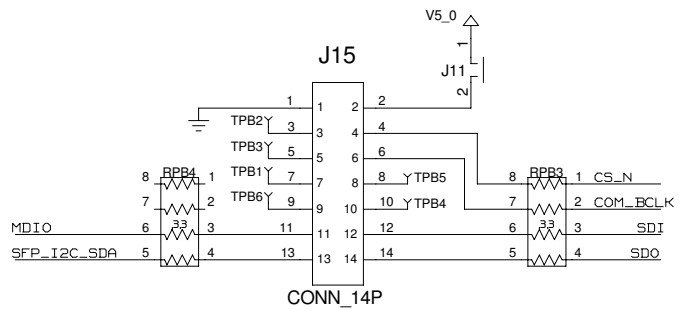
Top level Hierarchy block

TITLE: MAX24287 EVKIT Rev_B	DATE: 07-11-2011
ENGINEER: Steve Scully	PAGE: 3/11 (TOTAL) 3/B (BLOCK)

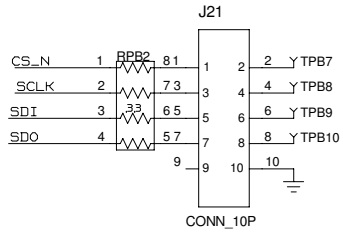


Top level Hierarchy block

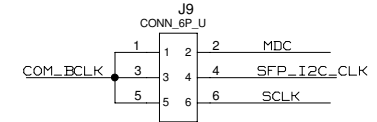
TITLE:	MAX24287 EVKIT Rev_B	DATE:	07-11-2011
ENGINEER:	Steve Scully	PAGE:	4/11 (TOTAL) 4/B (BLOCK)



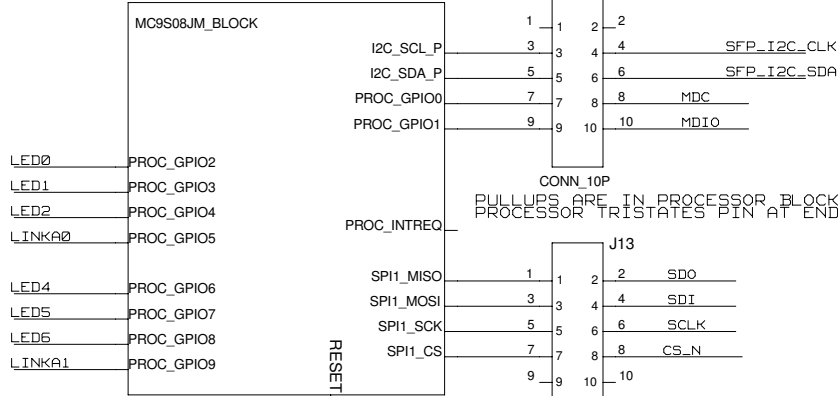
EXTERNAL SBC CONNECTOR



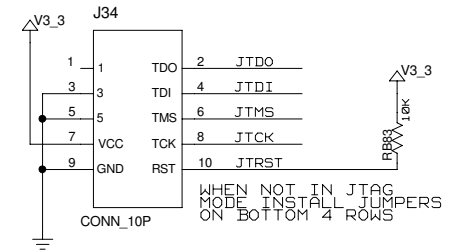
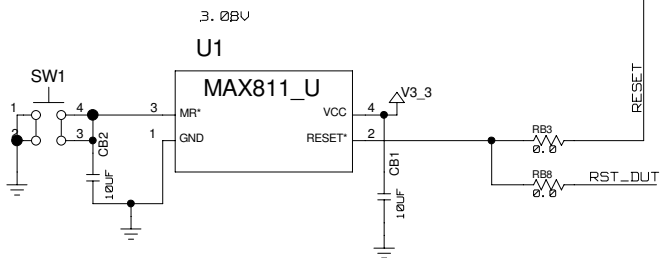
DS31400DK CONNECTOR



Processor Hierarchy block.  
Contents on page B



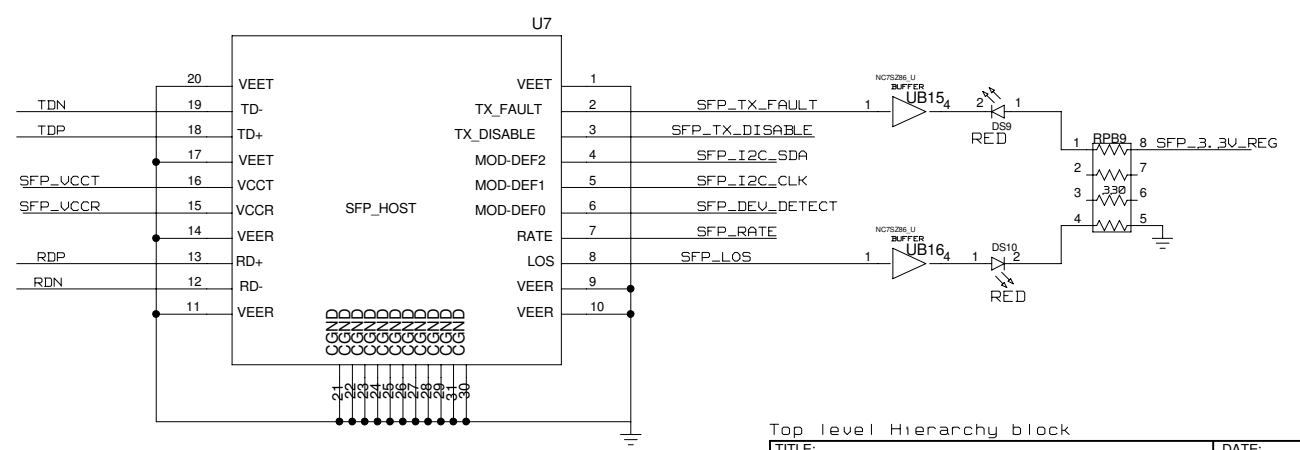
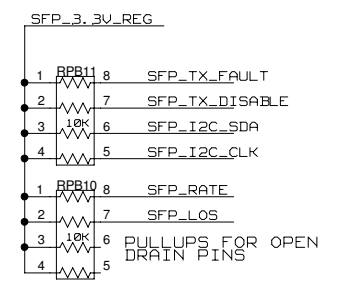
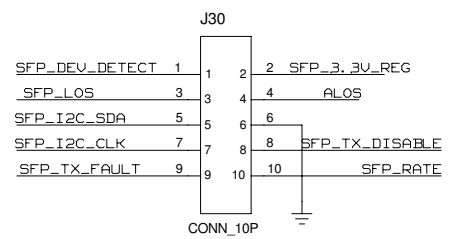
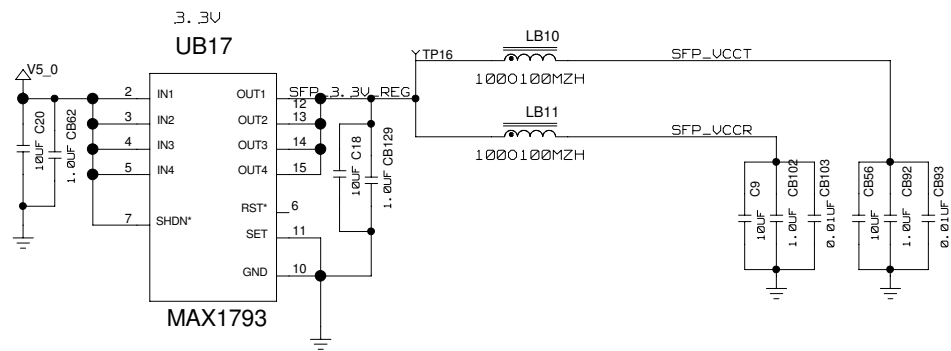
PULLUPS ARE IN PROCESSOR BLOCK  
PROCESSOR TRISTATES PIN AT END OF CYCLE



WHEN NOT IN JTAG  
MODE INSTALL JUMPERS  
ON BOTTOM 4 ROWS

Top level Hierarchy block

TITLE: MAX24287 EVKIT Rev_B	DATE: 07-11-2011
ENGINEER: Steve Scully	PAGE: 5/11 (TOTAL) 5/B (BLOCK)



Top level Hierarchy block

TITLE: MAX242B7 EVKIT Rev_B	DATE: 07-11-2011
ENGINEER: Steve Scully	PAGE: 6/11 (TOTAL) 6/B (BLOCK)

D

C

B

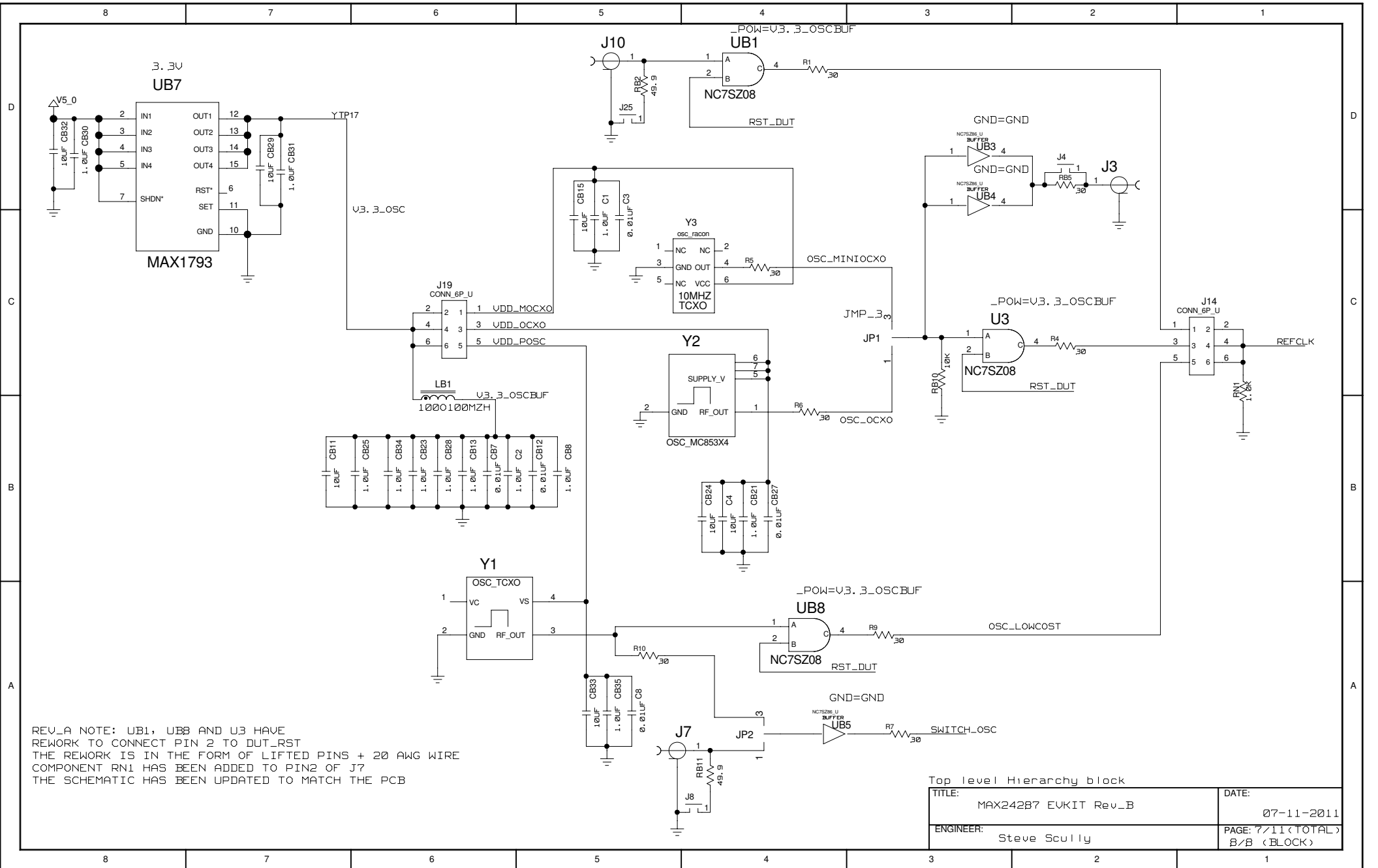
A

D

C

B

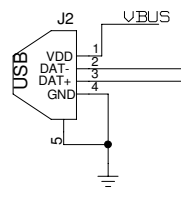
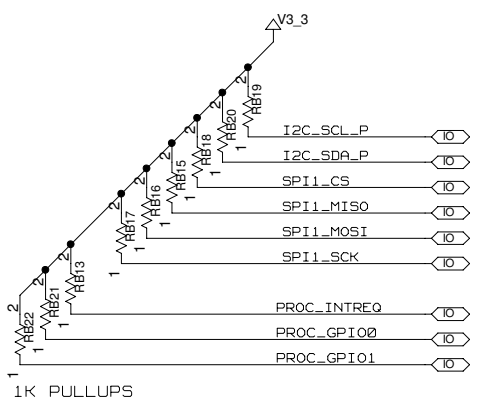
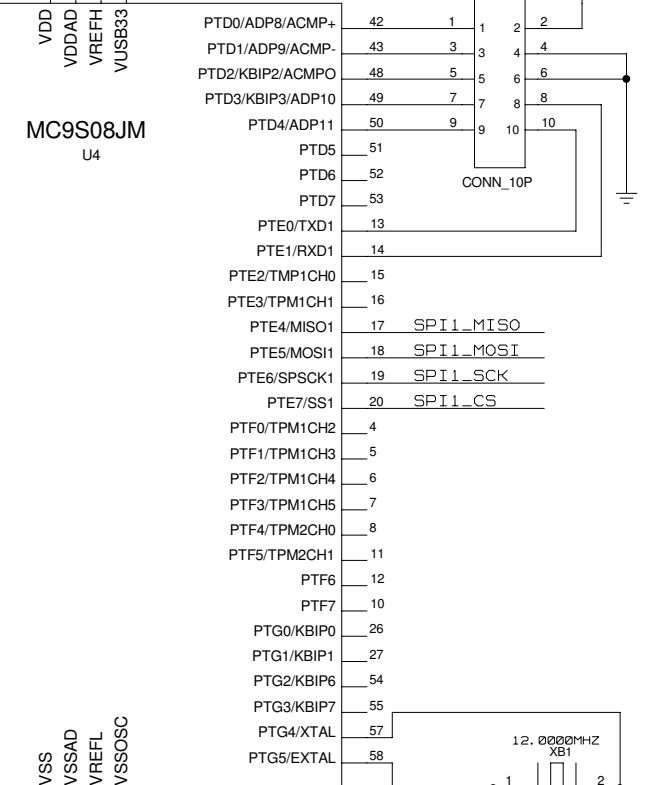
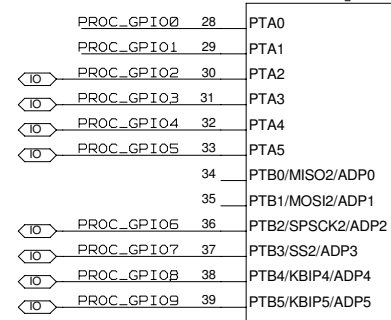
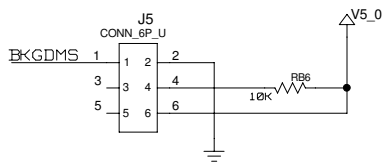
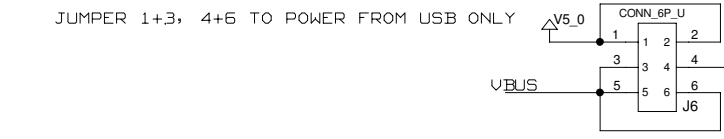
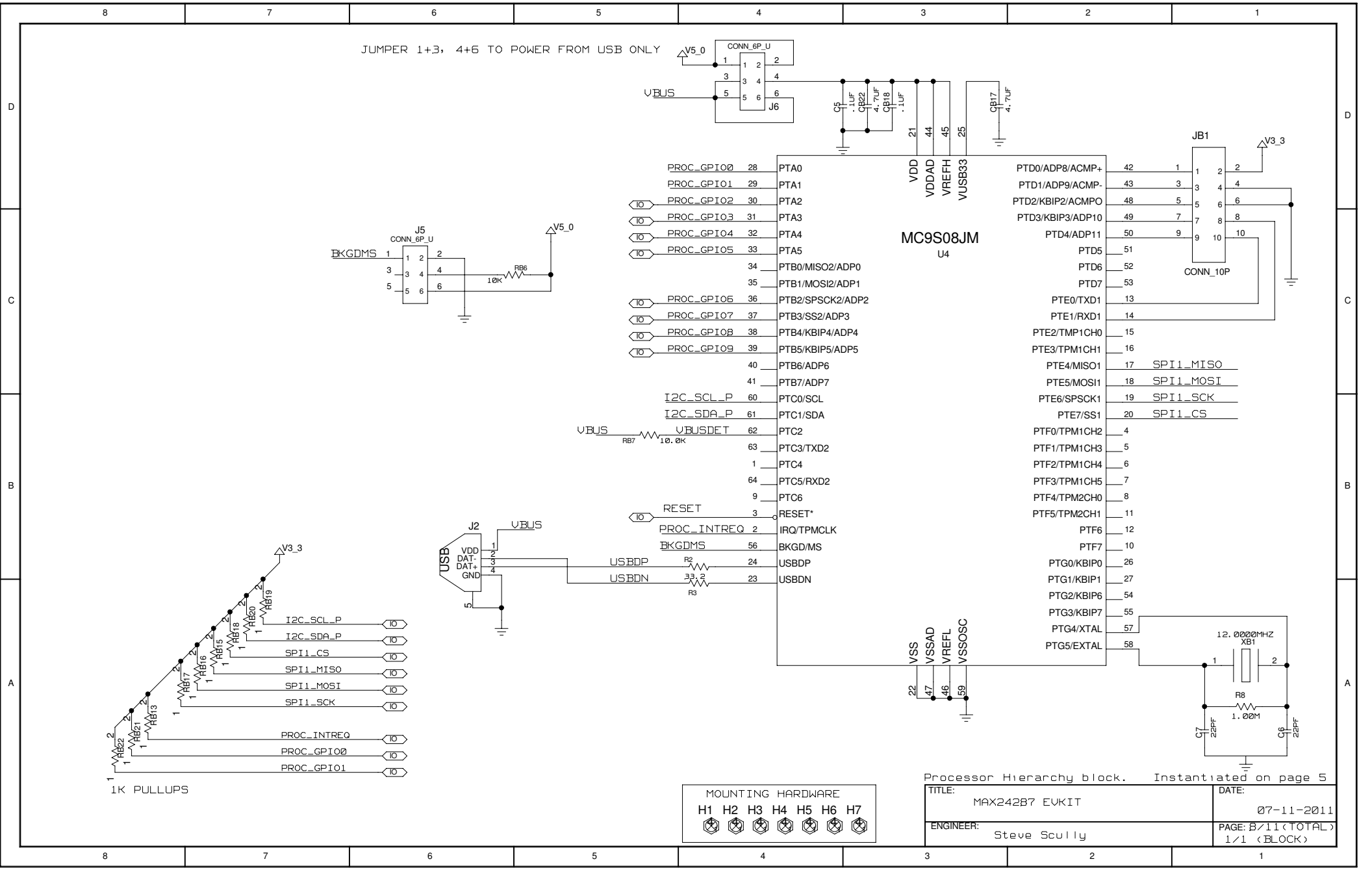
A



REV\_A NOTE: UB1, UB8 AND U3 HAVE  
 REWORK TO CONNECT PIN 2 TO DUT\_RST  
 THE REWORK IS IN THE FORM OF LIFTED PINS + 20 AWG WIRE  
 COMPONENT RN1 HAS BEEN ADDED TO PIN2 OF J7  
 THE SCHEMATIC HAS BEEN UPDATED TO MATCH THE PCB

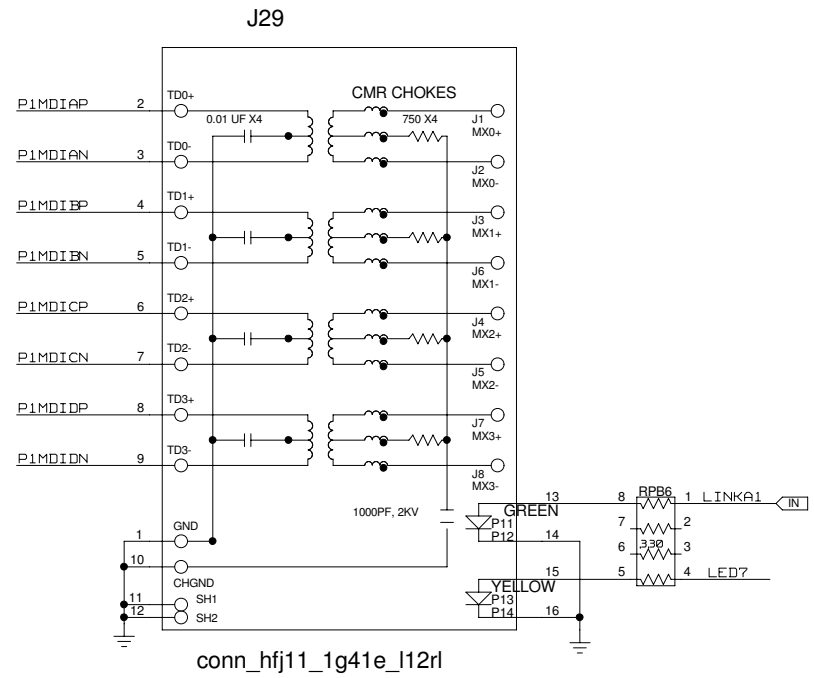
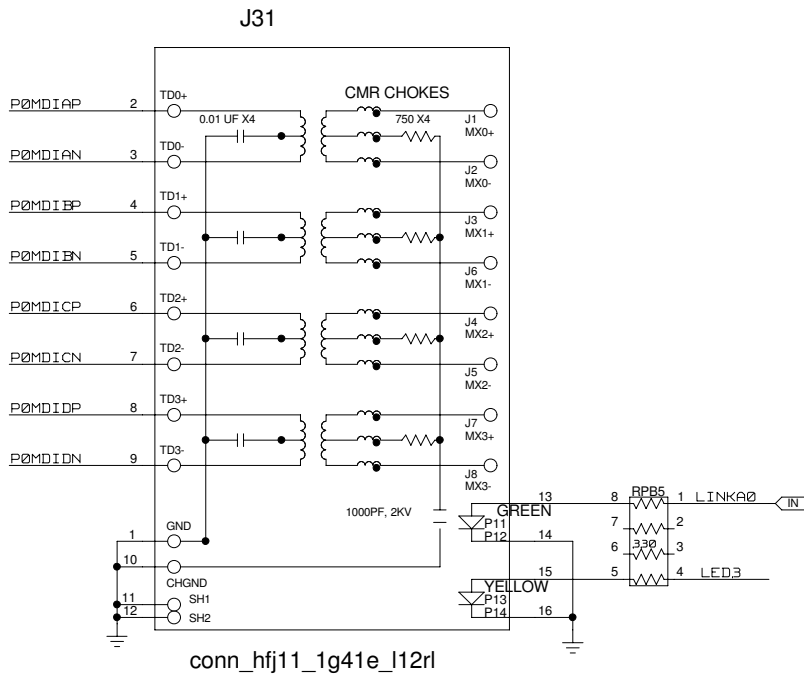
Top level Hierarchy block

TITLE: MAX2428B7 EVKIT Rev_B	DATE: 07-11-2011
ENGINEER: Steve Scully	PAGE: 7/11 (TOTAL) B/B (BLOCK)



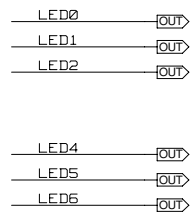
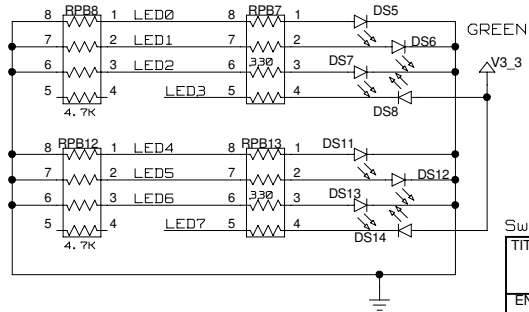






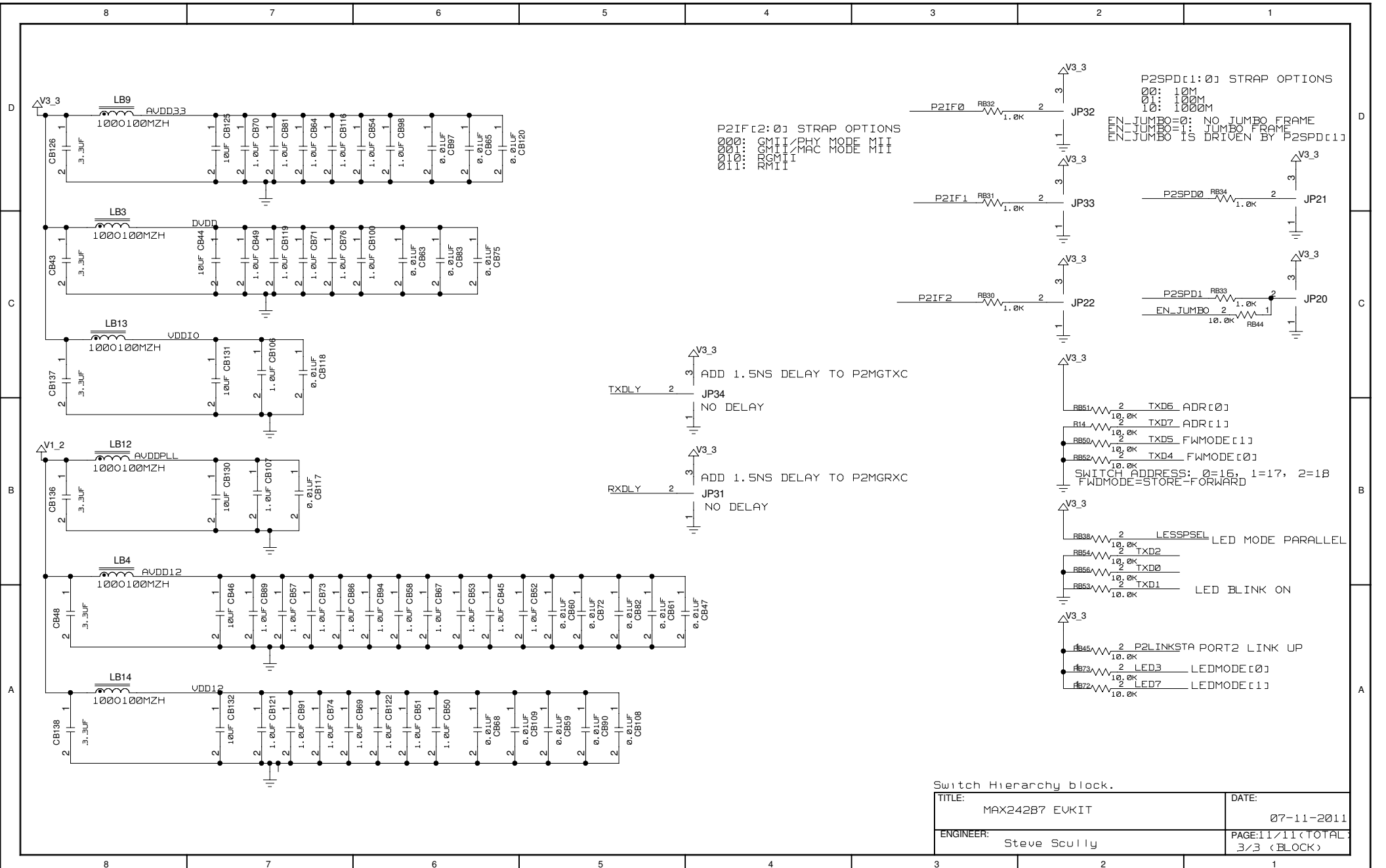
INDICATIONS FOR PARALLEL MODE0

- SWITCH0
- LED0=GIG-LINK/ACT
  - LED1=100-LINK/ACT
  - LED2=100-LINK/ACT
  - LED3=DUP/COL
- SWITCH1
- LED4=GIG-LINK/ACT
  - LED5=100-LINK/ACT
  - LED6=100-LINK/ACT
  - LED7=DUP/COL



Switch Hierarchy block.

TITLE:	MAX24287 EVKIT	DATE:	07-11-2011
ENGINEER:	Steve Scully	PAGE:10/11 (TOTAL)	2/3 (BLOCK)



P2IF[2:0] STRAP OPTIONS  
 000: GMII/PHY MODE MII  
 001: GMII/PHY MODE MII  
 010: RMII/MAC MODE MII  
 011: RMII/MAC MODE MII

TXDLY 3 ADD 1.5NS DELAY TO P2MGTXC  
 2 JP34  
 1 NO DELAY

RXDLY 3 ADD 1.5NS DELAY TO P2MGRXC  
 2 JP31  
 1 NO DELAY

P2SPD[1:0] STRAP OPTIONS  
 00: 10M  
 01: 100M  
 10: 1000M

EN\_JUMBO=0: NO JUMBO FRAME  
 EN\_JUMBO=1: JUMBO FRAME  
 EN\_JUMBO IS DRIVEN BY P2SPD[1:0]

SWITCH ADDRESS: 0=16, 1=17, 2=18  
 FWMODE=STORE-FORWARD

LESSPSEL LED MODE PARALLEL

LED BLINK ON

P2LINKSTA PORT2 LINK UP

LED3 LEDMODE[0]  
 LED7 LEDMODE[1]

Switch Hierarchy block.

TITLE: MAX24287 EVKIT	DATE: 07-11-2011
ENGINEER: Steve Scully	PAGE:11/11(TOTAL) 3/3 (BLOCK)