

MMA051PP45 Datasheet

DC–22 GHz 1W GaAs MMIC pHEMT Distributed Power Amplifier





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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Release Revision 1.0

Release revision 1.0 is the first publication of this document.

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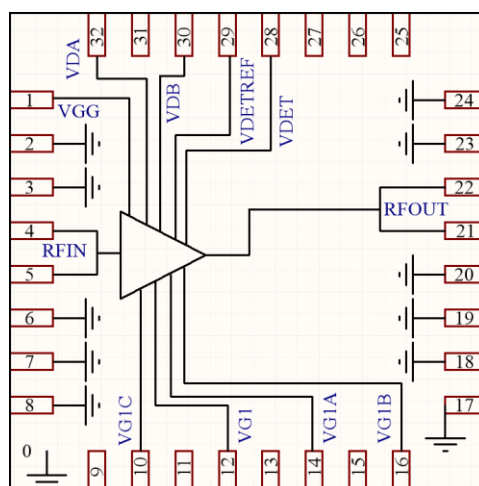
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2 Product Overview

MMA051PP45 is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) distributed amplifier that operates between DC and 22 GHz. It is ideal for test instrumentation, wideband military and space applications. The amplifier provides a flat gain of 14 dB, 3.5 dB noise figure, and 30 dBm of output power at 3 dB gain compression at 10 GHz with a nominal bias condition of 10 V 350 mA. Output IP3 is typically 35 dBm. The MMA051PP45 amplifier features RF I/Os that are internally matched to 50 Ω , which is ideal for any surface mount technology (SMT) assembly equipment.

The following figure is a functional block diagram for the MMA051PP45 device.

Figure 1 Functional Block Diagram



2.1 Applications

The MMA051PP45 device is designed for the following applications:

- Test and measurement instrumentation
- Military and space
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

2.2 Key Features

The following are key features of the MMA051PP45 device:

- Frequency range: DC to 22GHz
- 15dB gain
- High IP3: 35dBm@18GHz
- Supply: 10V @ 350mA
- Power Detector
- 50 Ohm Matched Input/Output
- Package size: 4.5mm x 4.5mm, 32L plastic QFN

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings at 25 °C unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1 Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 to 150 °C
Operating temperature	–55 to 85 °C
Drain bias voltage, (V_D)	12 V
Drain bias current, (I_{DD})	600mA
First gate bias voltage, (V_{G1})	0 V
RF input power	26 dBm
DC power dissipation ($T = 85\text{ °C}$)	6.7 W
Channel temperature	165 °C
Thermal impedance	12 C/W

3.2 Typical Electrical Performance

The following table lists the specified electrical performance of the MMA051PP45 device at 25 °C, where VDD is 10 V, IDD is 350mA, and VGG is –0.7 V.

Table 2 Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		DC		22	GHz
Gain	2-6 GHz	13	14		dB
	6 GHz-12 GHz	13	14		dB
	12 GHz-22 GHz	13	14		dB
Gain flatness	2 GHz-22 GHz		± 0.5		dB
Noise figure	DC-6 GHz		5		dB
	6 GHz-12 GHz		3.2		dB
	12 GHz-22 GHz		4		dB
Input return loss	DC-6 GHz		15	12	dB
	6 GHz-12 GHz		15	12	dB
	12 GHz-22 GHz		13	9	dB
Output return loss	DC-6 GHz		15	12	dB
	6 GHz-12 GHz		18	12	dB
	12 GHz-22 GHz		13	9	dB
P1dB @ 11 V, 500mA	DC-6 GHz	28.5	31		
	6 GHz-12 GHz	26.5	29		
	12 GHz-22 GHz	22	23		
P3dB @ 11 V, 500mA	DC-6 GHz		32		
	6 GHz-12 GHz		31		
	12 GHz-22 GHz		29		
OIP3	DC-6 GHz		42		
	6 GHz-12 GHz		39		
	12 GHz-22 GHz		35		
VDD (drain voltage supply)			10		V
IDD (drain current)			350		mA

3.3 Typical Performance Curves

The following graphs show the typical performance curves of the MMA051PP45 device at 25 °C, unless otherwise indicated. These measurements were taken on the evaluation board.

Figure 2 Gain vs V_{DD} ($I_{DD} = 350\text{mA}$, $T = 25\text{ °C}$)

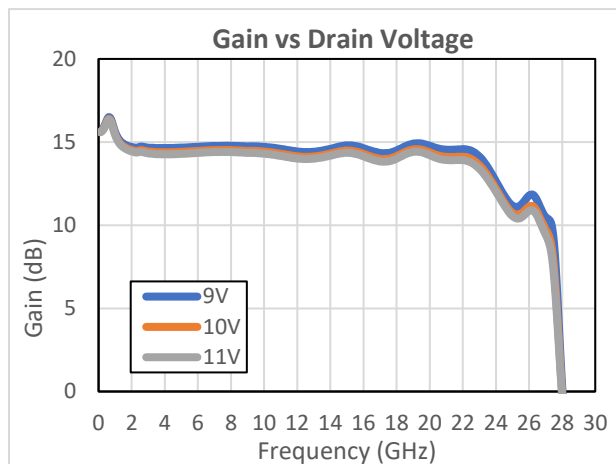


Figure 4 Gain vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$)

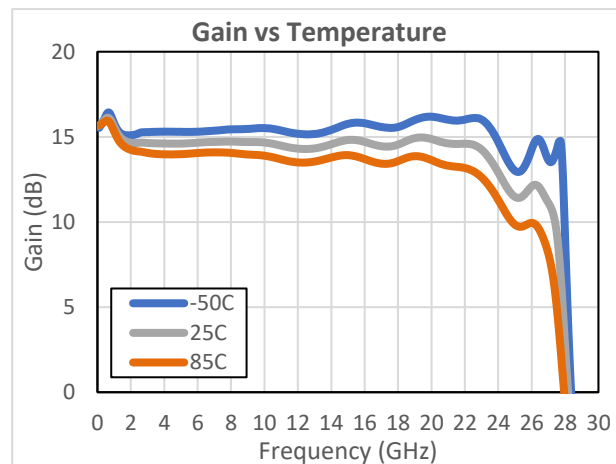


Figure 3 Gain vs I_{DD} ($V_{DD} = 10\text{ V}$, $T = 25\text{ °C}$)

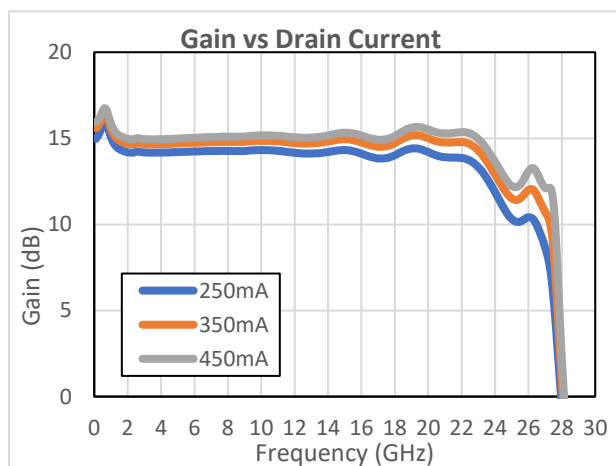


Figure 5 S_{11} vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$)

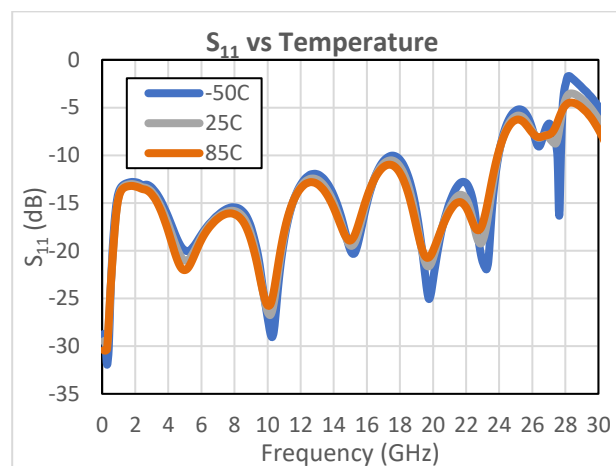


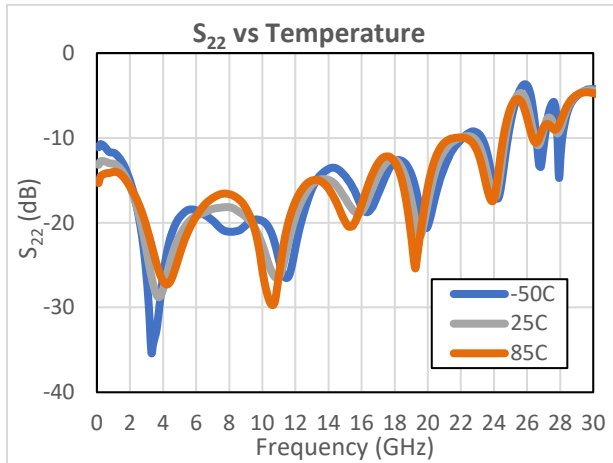
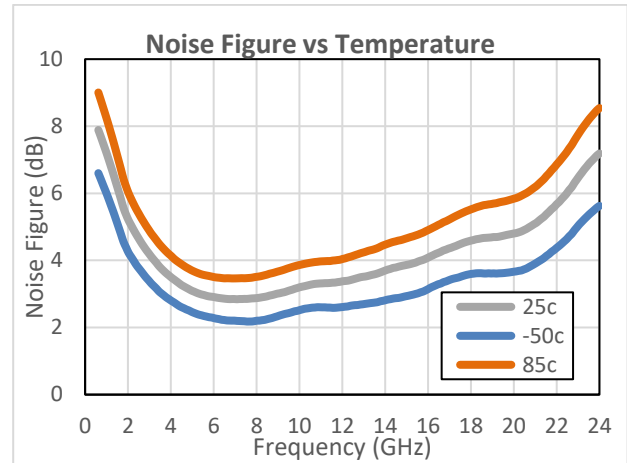
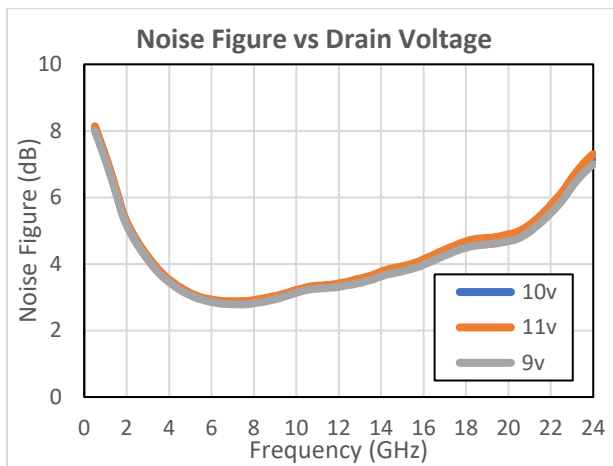
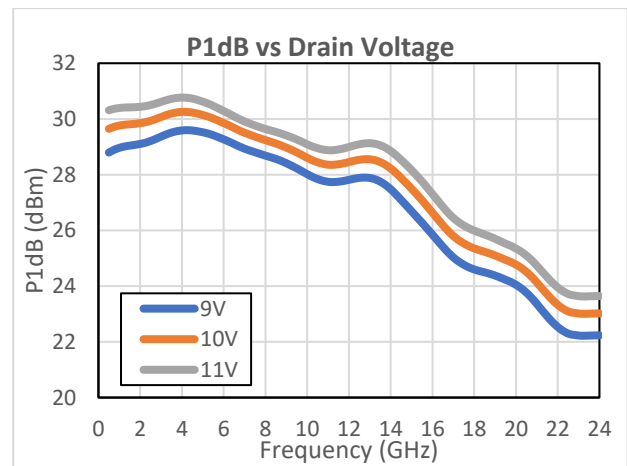
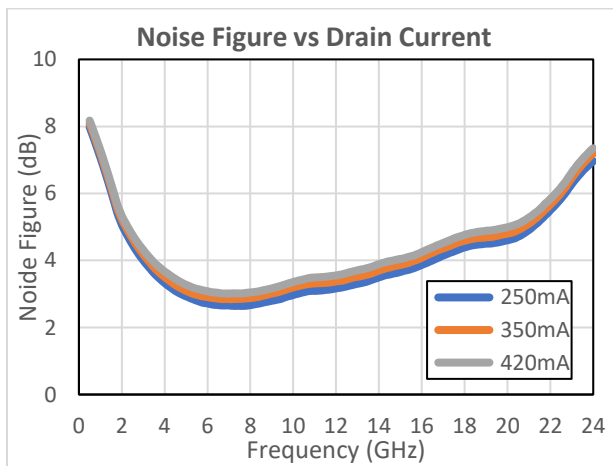
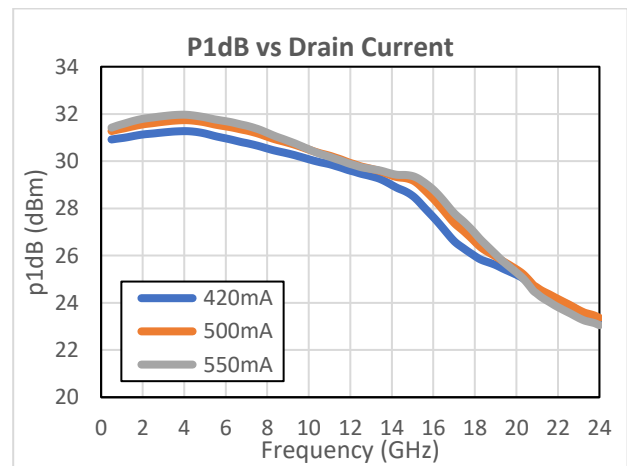
Figure 6 S_{22} vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$)**Figure 9 Noise Figure vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$)****Figure 7 Noise Figure vs V_{DD} ($I_{DD} = 350\text{mA}$, $T = 25\text{ °C}$)****Figure 10 P1dB vs V_{DD} ($I_{DD} = 350\text{mA}$, $T = 25\text{ °C}$)****Figure 8 Noise Figure vs I_{DD} ($V_{DD} = 10\text{ V}$, $T = 25\text{ °C}$)****Figure 11 P1dB vs I_{DD} ($V_{DD} = 11\text{ V}$, $T = 25\text{ °C}$)**

Figure 12 P1dB vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$)

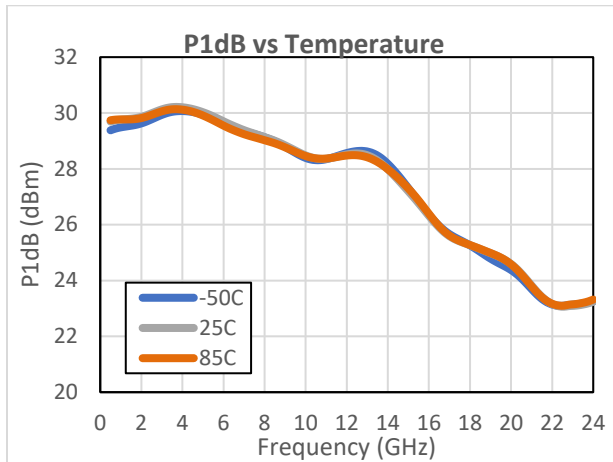


Figure 15 P3dB vs Temperature ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$)

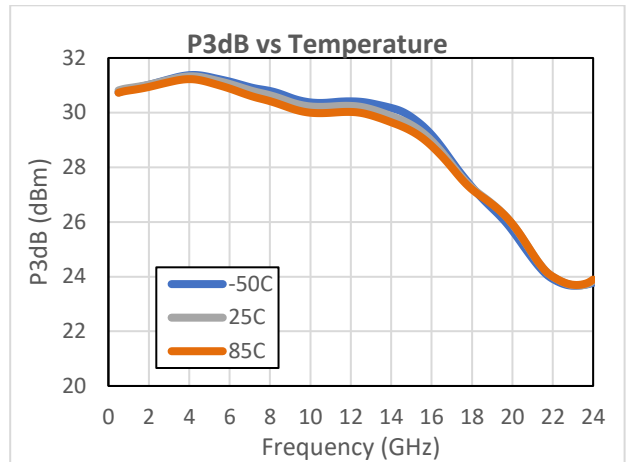


Figure 13 P3dB vs V_{DD} ($I_{DD} = 350\text{mA}$, $T = 25\text{ }^{\circ}\text{C}$)

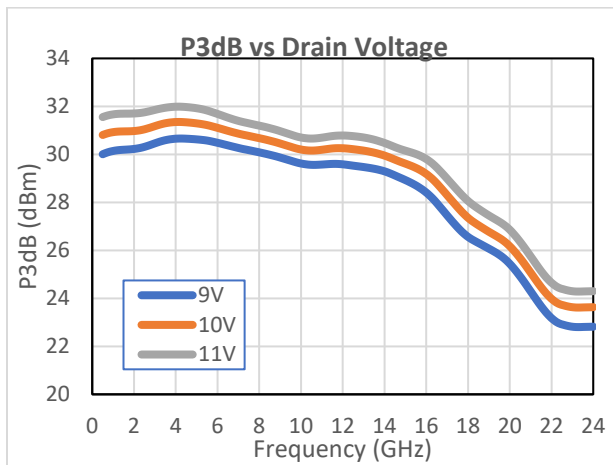


Figure 16 OIP3 vs V_{DD} ($I_{DD} = 350\text{mA}$, $T = 25\text{ }^{\circ}\text{C}$, $P_{out} = 10\text{dBm}$)

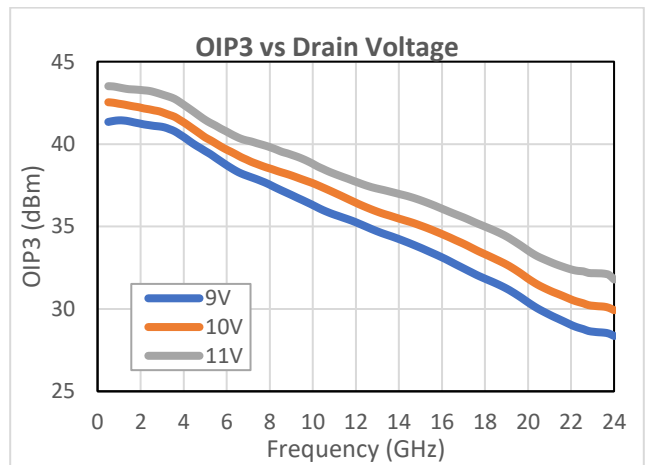


Figure 14 P3dB vs I_{DD} ($V_{DD} = 11\text{ V}$, $T = 25\text{ }^{\circ}\text{C}$)

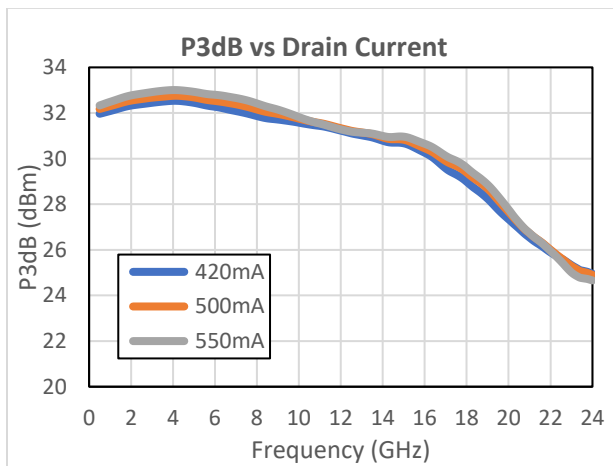


Figure 17 OIP3 vs Temp ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$, $P_{out} = 10\text{dBm}$)

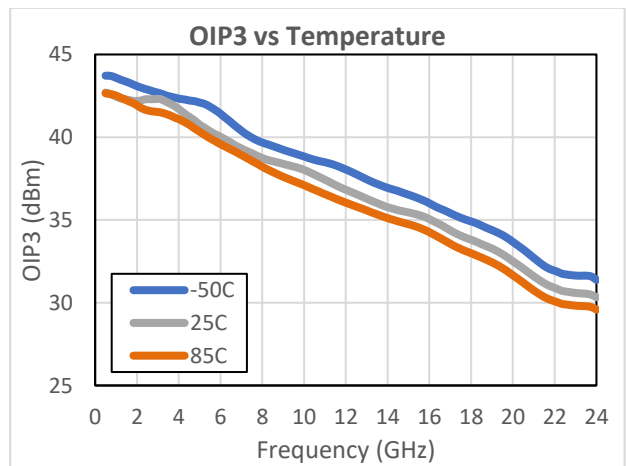


Figure 18 IM3 vs Output Power ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$, $T = 25\text{ }^{\circ}\text{C}$)

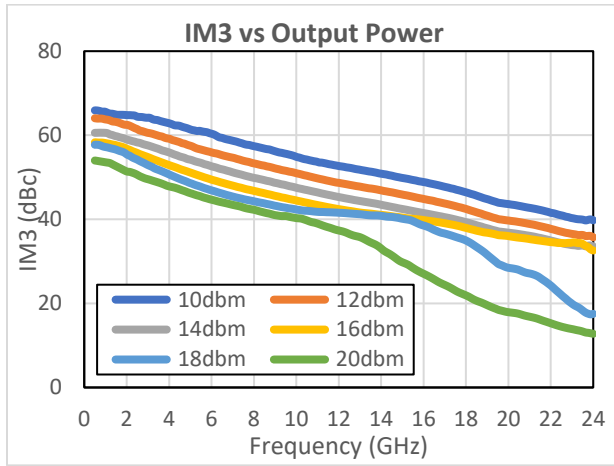


Figure 19 Second Harmonic vs Output Power ($V_{DD} = 10\text{V}$, $I_{DD} = 350\text{mA}$, $T = 25\text{ }^{\circ}\text{C}$)

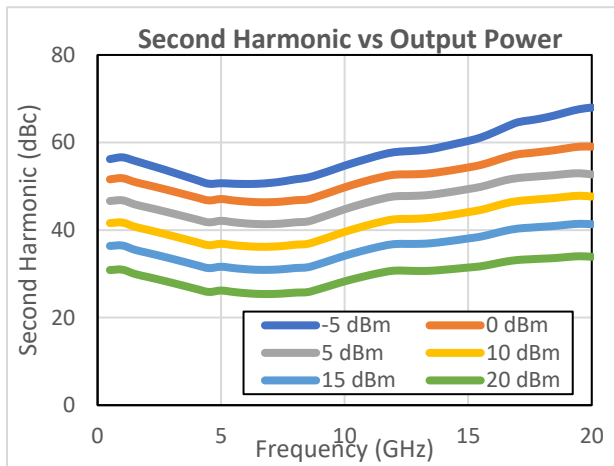


Figure 20 Detector vs Output Power ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$, $T = 25\text{ }^{\circ}\text{C}$)

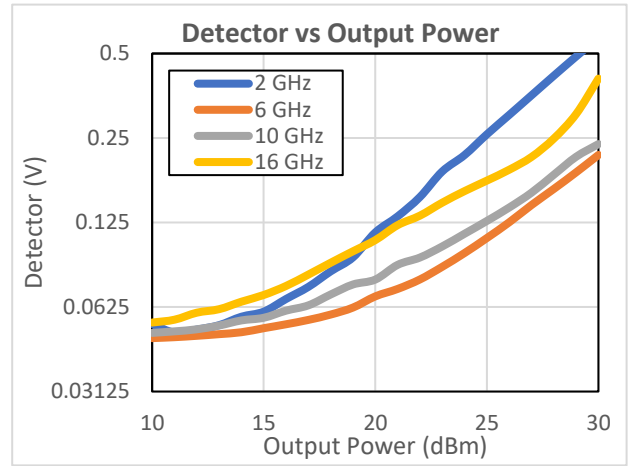
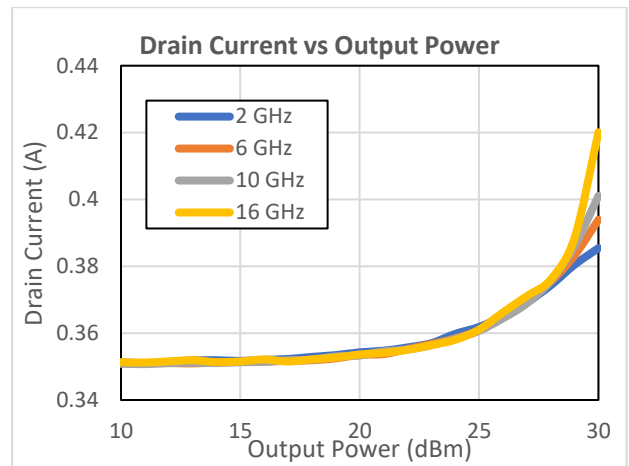
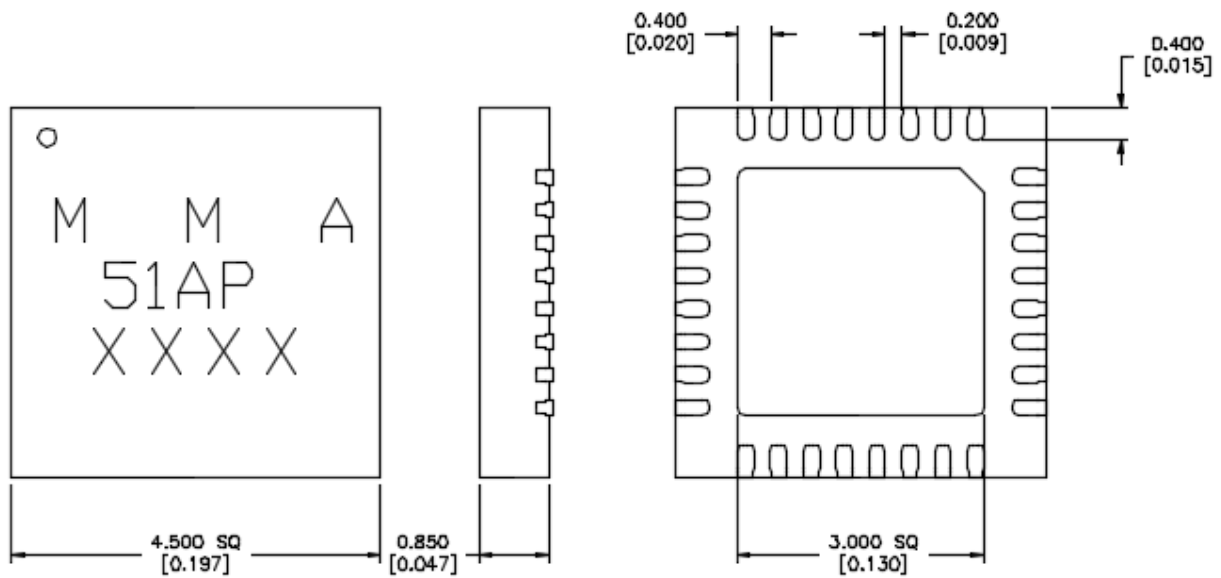


Figure 21 Drain Current vs Output Power ($V_{DD} = 10\text{ V}$, $I_{DD} = 350\text{mA}$, $T = 25\text{ }^{\circ}\text{C}$)





Part Number	Package Body Material	Lead Finish
MMA051PP45	RoHS - Compliance Low-stress injection molded plastic	Matte Sn

4.3 Pin Descriptions

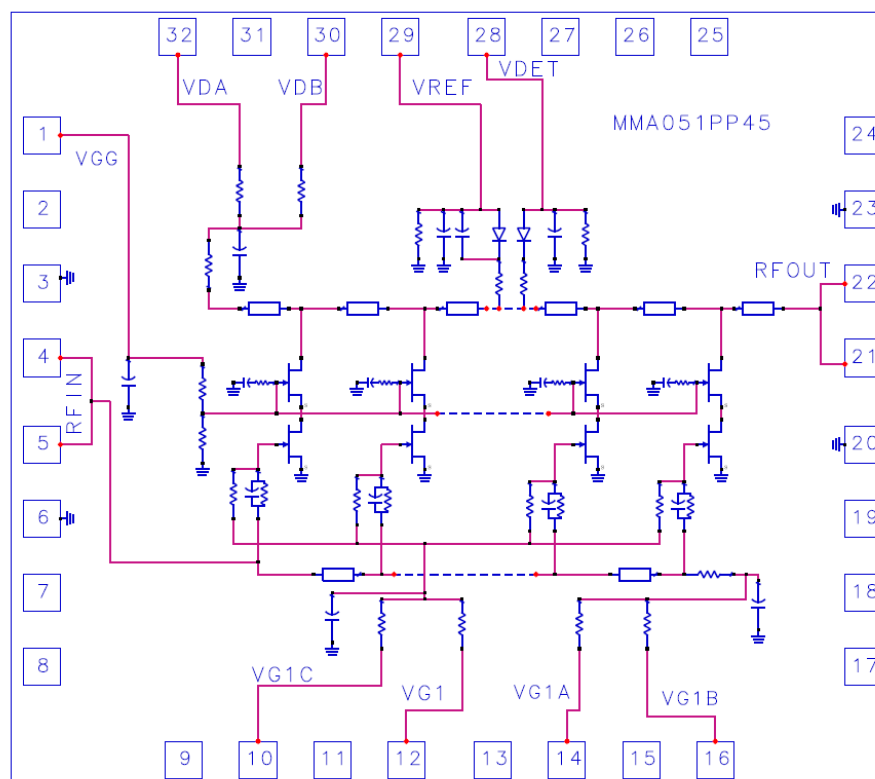
The following table describes the pins of the MMA051PP45 device.

Table 4 Pin Description

Pin Number	Pin Name	Description
4, 5	RF _{IN}	Pin 4 and 5 must be merged on the layout and are matched to 50 Ω. DC coupled to gate 1. Please see the layout pattern. (Figure 24)
12	V _{G1}	First gate bias. Adjust to achieve required I _{DD} .
13	V _{G2}	DC couple to V _{DA} externally for nominal operation.
14	V _{G1A}	Low-frequency termination. Connect bypass capacitors per application circuit below.
21, 22	RF _{OUT} + V _{DD}	Pin 21 and 22 must be merged on the layout and are matched to 50 Ω. VDD bias through bias tee. Please see the layout pattern. (Figure 24)
28	V _{DET}	Detector pin. Voltage depends on RF output.
29	V _{DETREF}	Reference voltage for detector.
30, 32	V _{DB} , V _{DA}	DC linked to V _{DD} internally. External bypass capacitors are required to extend RF match and gain flatness below 2 GHz.
1, 2, 7, 10, 12, 14, 19	Ground	
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	Connect to ground.

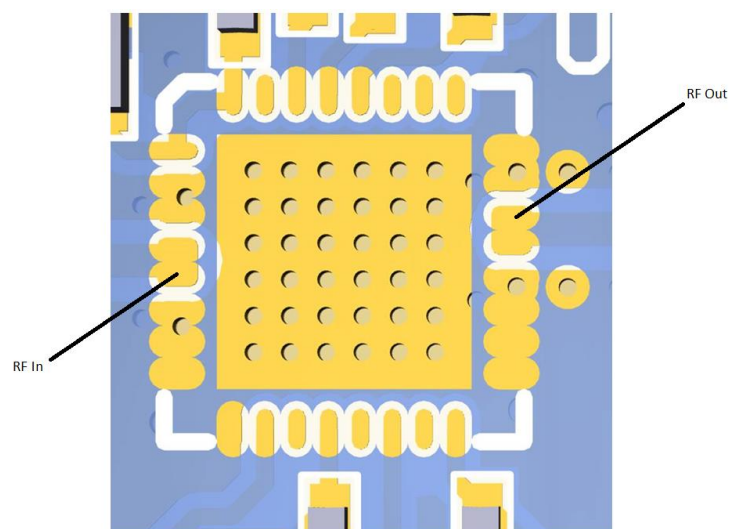
The following image shows the functional schematic of the MMA051PP45 device.

Figure 20 Drain Functional schematic



The following image shows the recommended layout pattern of the MMA051PP45 device.

Figure 21 Layout Pattern



The following illustration shows the application circuit of the MMA051PP45 device. Note that there is no internal DC blocking capacitor, and a bias tee must be used to on pin 21 and 22 for biasing V_{DD} .

The schematic diagram illustrates the MMA051PP45 evaluation board. The central component is the MMA051PP45 chip, which has numerous pins labeled with functions such as VDDA, VGG, RFIN, RFOUT, VDET, VDB, VDETRF, VG1C, VG1, VG1A, VG1B, and others. The board includes several connectors: J1 and J2 are 25-pin headers; J3 is a 2x2 connector; J4 is a 3-pin header; J5 is a 3-pin header; J6 is a 4-pin connector; and J7 is a 2-pin connector labeled CON_SHORT. Capacitors C1 through C8 are distributed across the board, with values ranging from 10nF to 2.2uF(16V). Ground connections are indicated by GND symbols throughout the circuit.

5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note [AN01 GaAs MMIC Handling and Die Attach Recommendations](#).

6 Evaluation Board Information

The following image shows the evaluation board of the MMA051PP45E device.

Figure 23 Evaluation Board

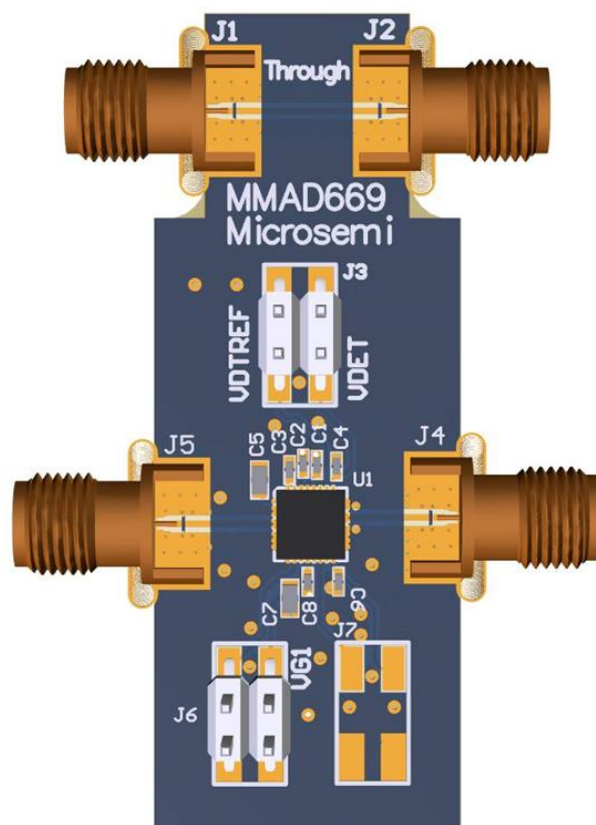


Table 5 List of Materials for Evaluation PCB MMA051PP45E

Item	Description
C1, C3, C6, C7	CAP 10 nF 50 V –20% to +80% 0402
C2, C5, C8	2.2 μ F 16 V ceramic capacitor X5R 0603
C4	CAP 100 pF 50 V $\pm$ 10% 0402
J4	Header, 2-pin, dual row
J2, J3, J5, J6	CONN 2.92 mm female PCB edge mount .012 pin

Table 6 Bias Sequence

Bias Sequence
1) Set the gate voltage VG1 to -1V
2) Set drain voltage VDD to 10V
3) Adjust the gate voltage until the drain current is 350mA

Ordering Information

Table 6 Ordering Information

Part Number	Description	Minimum Quantity
MMA051PP45	32 Lead SMT	1
MMA051PP45E	Evaluation Board	1
MMA051PP45TR	Tape and Reel	500