MMA051AA

1 W DC-24 GHz GaAs pHEMT Distributive Power Amplifier

Power Matters.™

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About Microsemi

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Revision History

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

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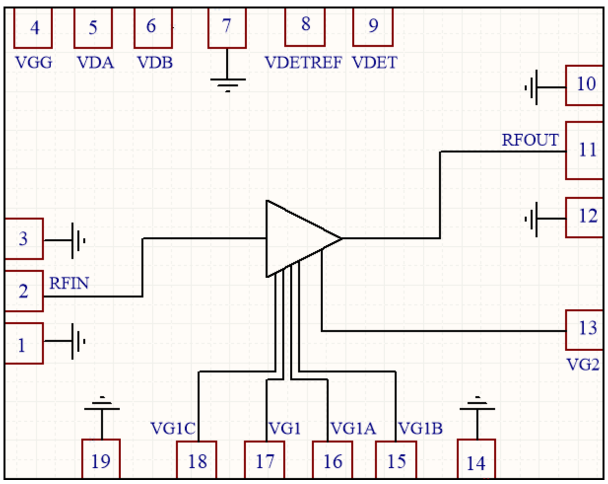
2 Product Overview

MMA051AA is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron-mobility transistor (pHEMT) distributed amplifier that operates between DC and 24 GHz. It is ideal for test instrumentation, wideband military and space applications. The amplifier provides a flat gain of 15 dB, 4 dB noise figure, and 30 dBm of output power at 3 dB gain compression with a nominal bias condition of 350 mA from a 10 V supply. Output IP3 is typically 40 dBm. The MMA051AA amplifier is DC coupled and features RF I/Os that are internally matched to 50 Ω.

The following image shows the primary functional blocks of the MMA051AA device.

Figure 1 Functional Block Diagram



2.1 Applications

The MMA051AA device is designed for the following applications:

- Test and measurement instrumentation
- Military and space
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

2.2 Key Features

The following are key features of the MMA051AA device:

- Frequency range: DC to 24 Ghz
- Gain: 15 dB
- High IP3: 37dBm@15GHz
- Low Noise: 4dB@15GHz
- Supply: 10V @ 350mA
- Power Detector
- 50 Ohm Matched Input/Output
- Die size: 3 x 1.56 x 0.075 mm

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings at 25 °C unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1 Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 to 150 °C
Operating temperature	–55 to 85 °C
Drain bias voltage, (V_{DD})	12 V
Gate bias voltages, (V_{G1})	0 V
V_{DD} current (I_{DD})	600 mA
RF input power	26 dBm
DC power dissipation (T = 85 °C)	6.7 W
Channel temperature	165 °C
Thermal impedance	12 °C/W

3.2 Typical Electrical Performance

The following table lists the specified electrical performance of the MMA051AA device at 25 °C, where VDD is 10 V, and IDD is 350 mA.

Table 2 Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		DC		26	GHz
Gain	DC-6 GHz	14	15		dB
	6 GHz-12 GHz	14	15		dB
	12 GHz-20 GHz	14	15		dB
Gain flatness	4 GHz-12 GHz		± 0.5		dB
	12 GHz-20 GHz		± 0.5		dB
Noise figure	2-6 GHz		4.5		dB
	6 GHz-12 GHz		3.2	4	dB
	12 GHz-20 GHz		4	5	dB
Input return loss	DC-6 GHz		14		dB
	6 GHz-12 GHz		14		dB
	12 GHz-20 GHz		15		dB
Output return loss	DC-6 GHz		15		dB
	6 GHz-12 GHz		15		dB
	12 GHz-20 GHz		15		dB
P1dB @ 11 V, 350mA	DC-6 GHz	29	30		dBm
	6 GHz-12 GHz	27.5	29		dBm
	12 GHz-20 GHz	26	28		dBm
P3dB @ 11 V, 350mA	DC-6 GHz		31		dBm
	6 GHz-12 GHz		31		dBm
	12 GHz-20 GHz		30		dBm
OIP3	DC-6 GHz		42		dBm
	6 GHz-12 GHz		40		dBm
	12 GHz-20 GHz		36		dBm
V_{DD} (drain voltage supply)			10		V
I_{DD} (drain current)			350		mA

3.3 Typical Performance Curves

The following graphs show the typical performance curves of the MMA051AA device at 25 °C, unless otherwise indicated.

Figure 2 Gain vs. I_{DD} (V_{DD} = 10v, T=25 °C)

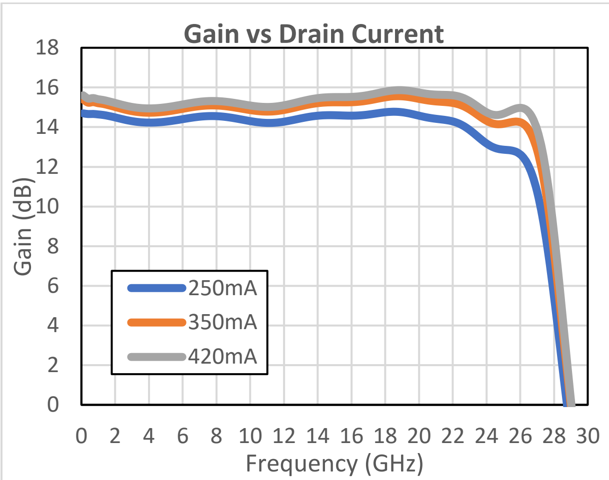


Figure 3 Gain vs V_{DD} (I_{DD} = 350mA, T = 25 °C)

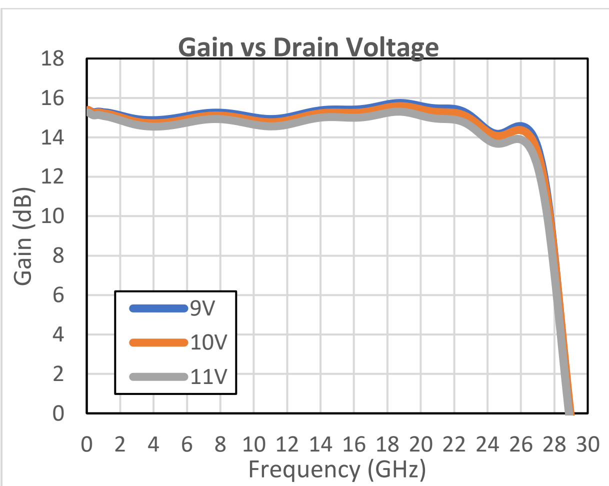


Figure 4 Gain vs Temperature (V_{DD} = 10v, I_{DD} = 350mA)

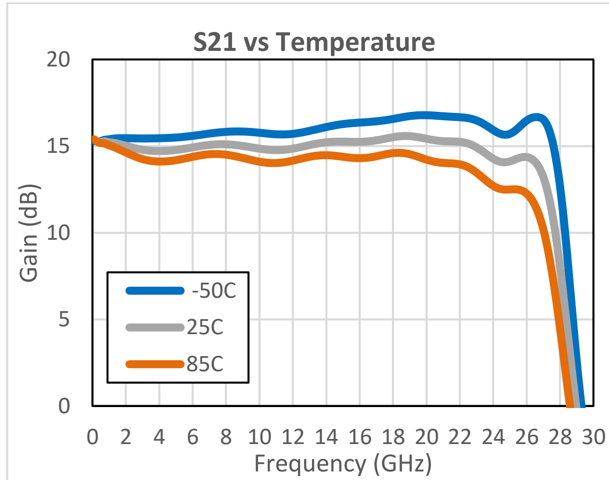


Figure 5 S_{11} vs Temperature (V_{DD} = 10v, I_{DD} = 350mA)

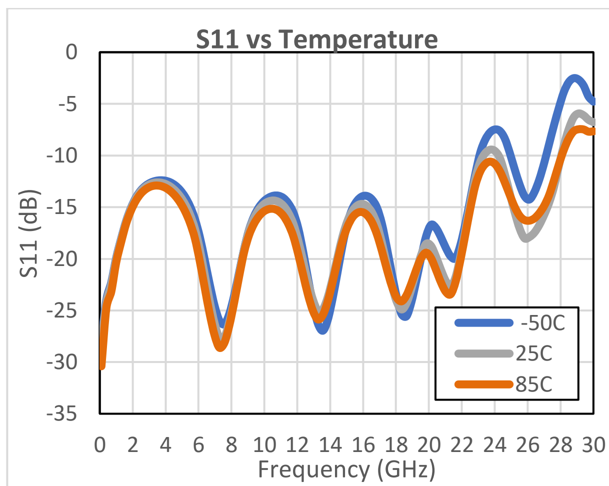


Figure 6 S_{22} vs Temperature (V_{DD} = 10v, I_{DD} = 350mA)

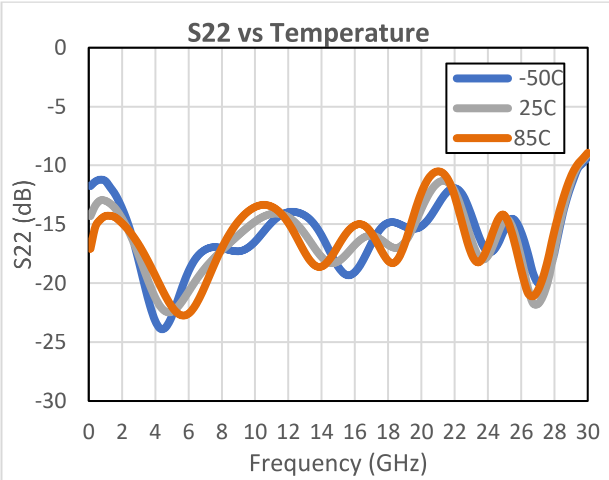


Figure 8 Noise Figure vs I_{DD} (V_{DD} = 9v, T = 25 °C)

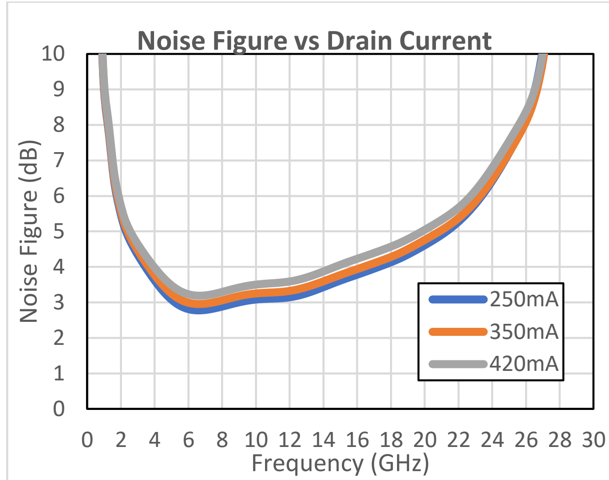


Figure 6 NF vs. Temperature (V_{DD} = 9v, I_{DD} = 350mA)

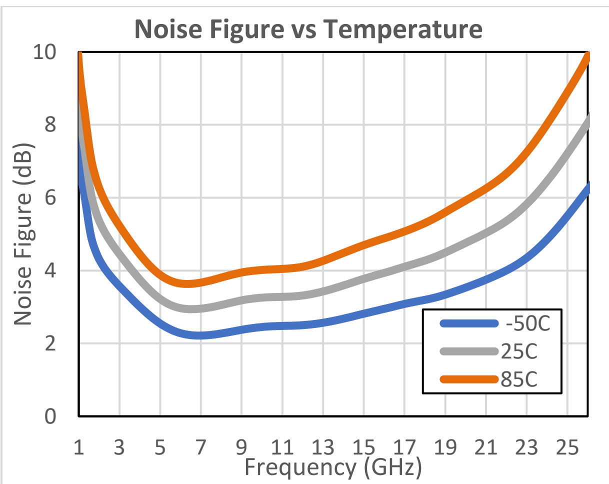


Figure 9 P1dB vs V_{DD} (I_{DD} = 350mA, T = 25 °C)

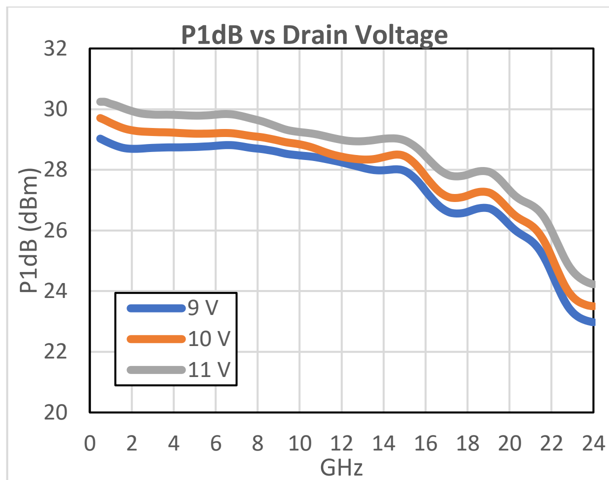


Figure 7 Noise Figure vs V_{DD} (I_{DD} = 350mA, T = 25 °C)

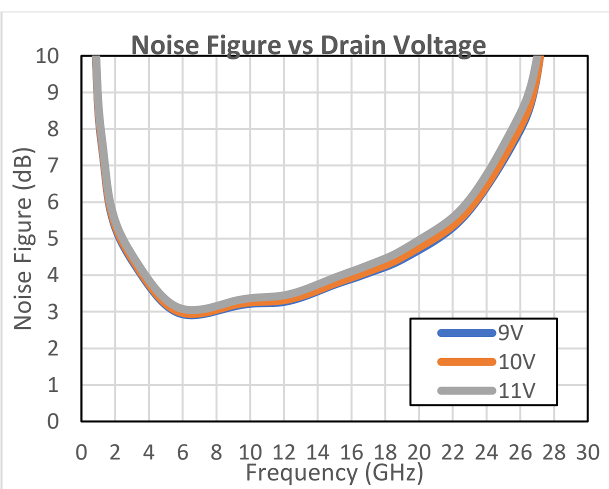


Figure 10 P1dB vs V_{DD} (I_{DD} = 350mA, T = 25 °C)

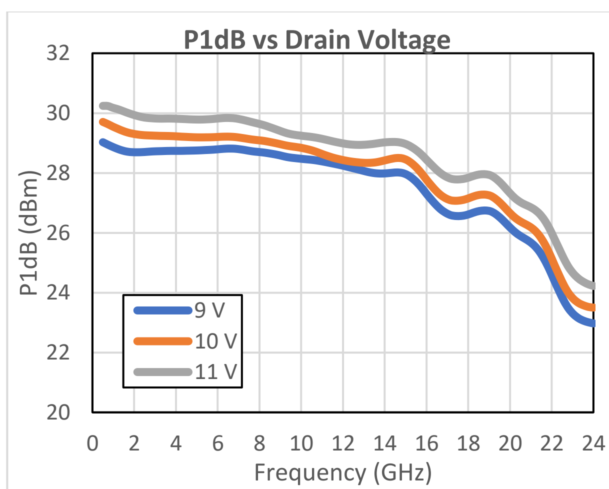


Figure 11 P3dB vs V_{DD} (I_{DD} = 420mA, T = 25 °C)

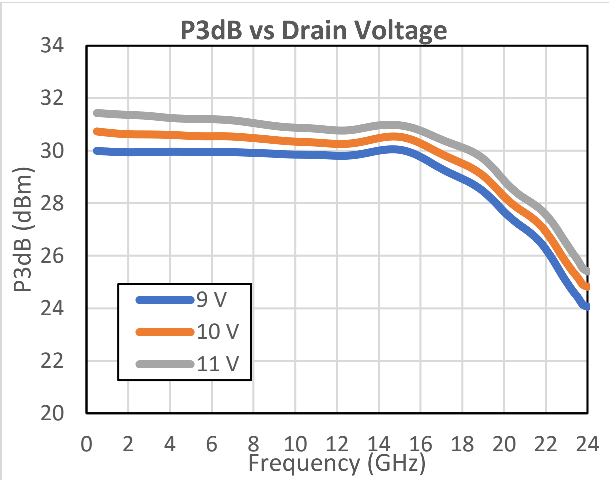


Figure 12 P3dB vs Temperature (V_{DD} = 10 V, I_{DD} = 350mA)

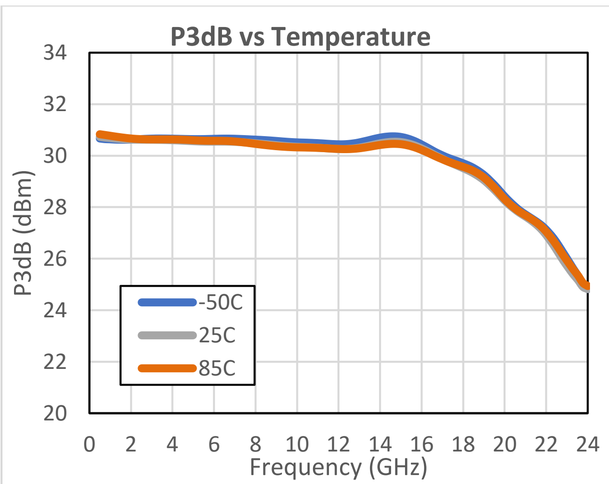


Figure 13 OIP3 vs Temperature (V_{DD} = 10 V, I_{DD} = 350mA)

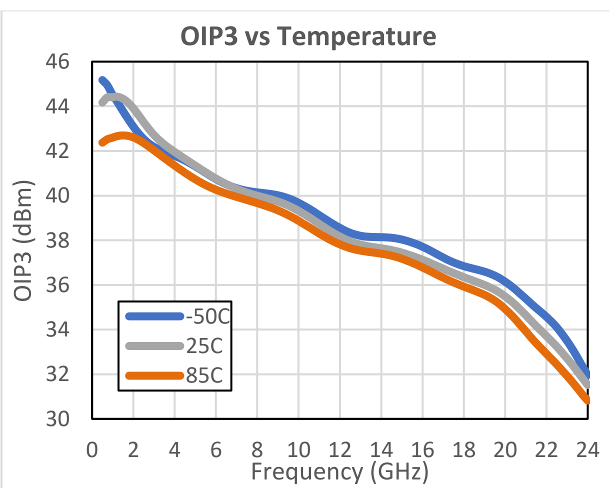


Figure 14 OIP3 vs I_{DD} (V_{DD} = 10 V, T = 25 °C)

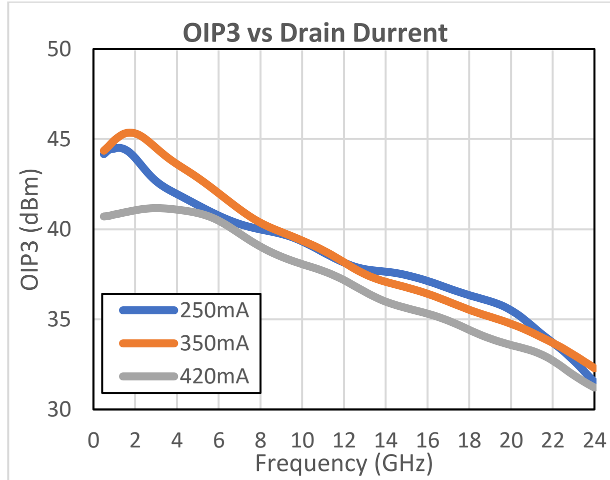


Figure 156 IM3 vs Output Level (V_{DD} = 10 V, I_{DD} = 350mA, T = 25 °C)

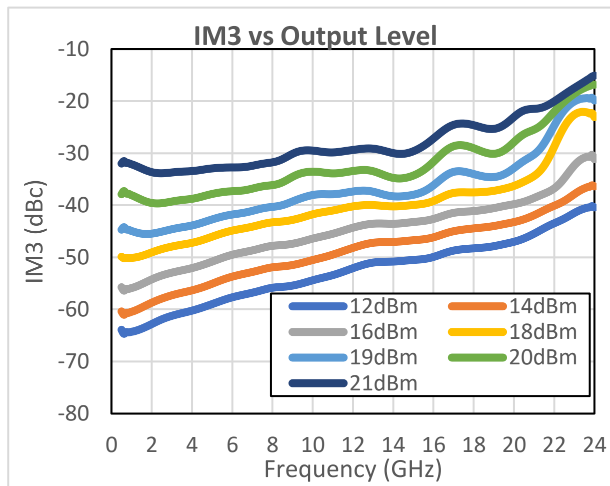


Figure 16 2nd Harmonic vs Pout (V_{DD} = 10 V, I_{DD} = 350mA, T = 25 °C)

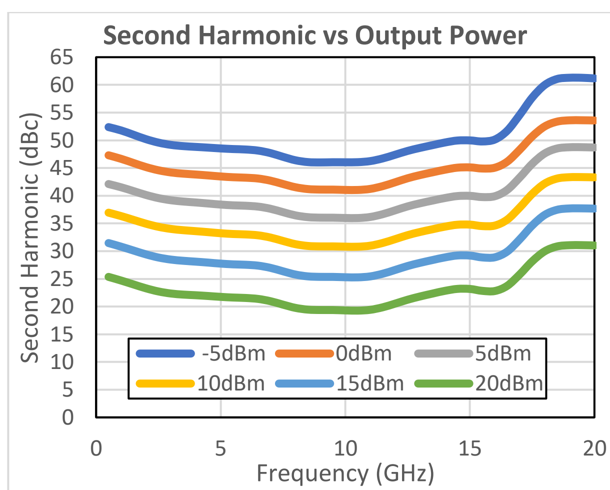


Figure 17 Detector vs Output Power (V_{DD} = 10 V, I_{DD} = 350mA, T = 25 °C)

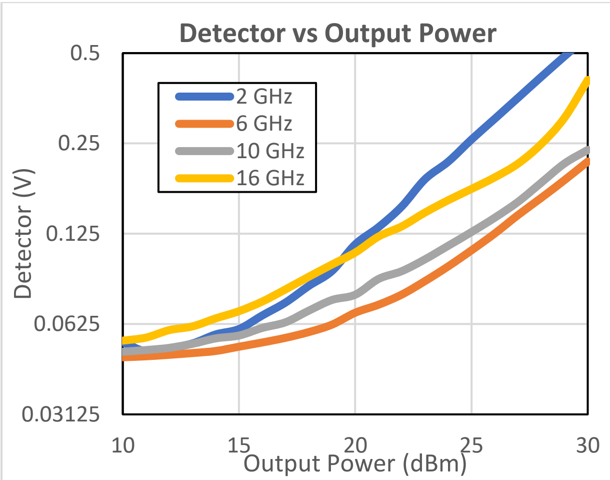
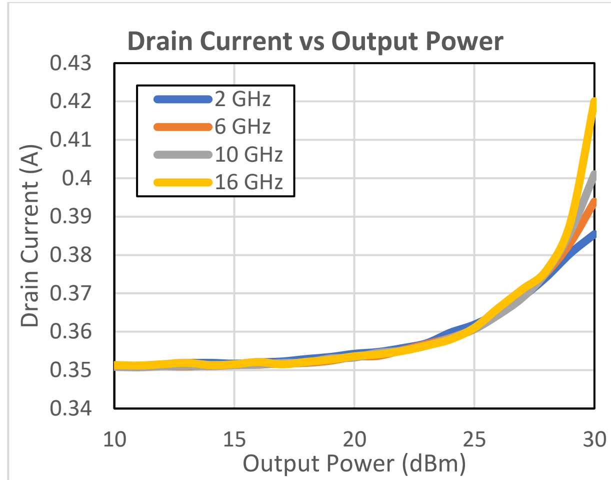


Figure 18 Detector vs Output Power (V_{DD} = 10 V, I_{DD} = 350mA, T = 25 °C)



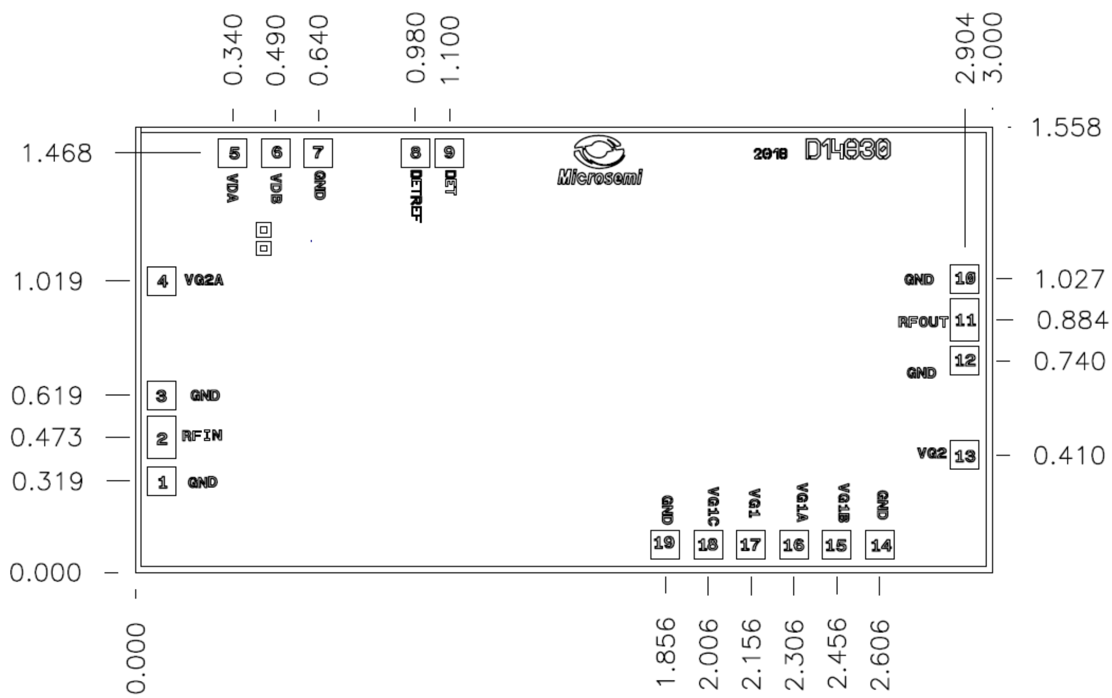
4 Chip Outline Drawing, Die Packaging, Bond Pad, and Assembly Information

This section details the package specifications of the MMA051AA device.

4.1 Chip Outline Drawing

The following illustration shows the chip outline of the MMA051AA device.

Figure 19 P3dB Outline Package



4.2 Die Packaging Information

The following table shows the chip outline of the MMA051AA device. For additional packaging information, contact your Microsemi sales representative.

Table 3 Packaging Information

Standard Format	Optional Format
Gel pack	JEDEC pack
50 pieces per pack	100 + pieces per pack

4.3 Bond Pad Information

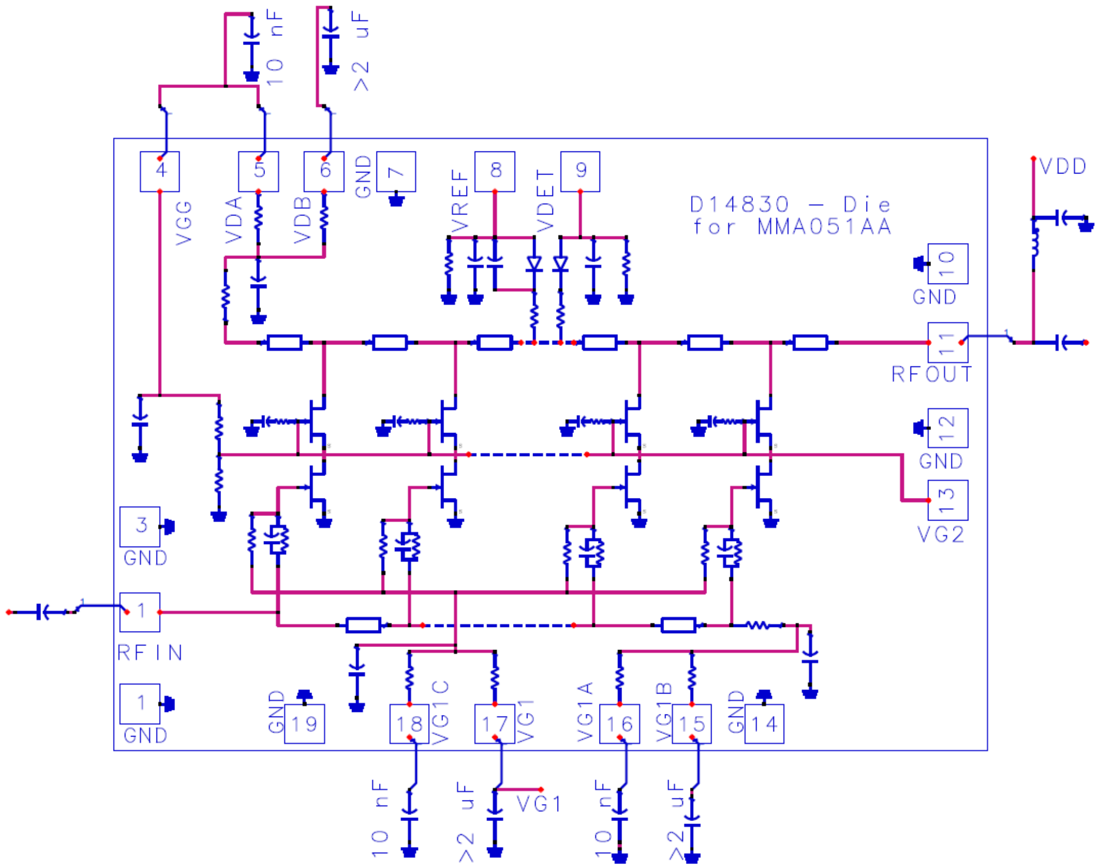
The following table shows the bond pad information of the MMA051AA device.

Table 4 Pin Description

Bond Pad Number	Bond Pad Name	Description
2	RF_{IN}	This pad is DC-coupled and matched to 50 Ω.
11	RF_{OUT} + V_{DD}	This pad is matched to 50 Ω. V_{DD} bias through bias tee.
4	V_{G2A}	DC couple to V_{DB} for nominal operation
5,6	V_{DB}, V_{DA}	DC linked to V_{DD} internally. External bypass capacitors are required to extend RF match and gain flatness below 2 GHz.
8	V_{DETREF}	Reference voltage for detector.
9	V_{DET}	Detector pad. Voltage depends on RF output.
13	V_{G2}	DC couple to V_{DA} externally for nominal operation.
15	V_{G1A}	Low-frequency termination. Connect bypass capacitors per application circuit below.
16	V_{G1B}	Low-frequency termination. Connect bypass capacitors per application circuit below.
17	V_{G1}	V_{GG} bias. Adjust to achieve required I_{DD}.
18	V_{G1C}	Low-frequency termination. Connect bypass capacitors per application circuit below.
1, 2, 7, 10, 12, 14, 19	Ground	

The following image shows the functional schematic of the MMA051AA device.

Figure 20 Functional Schematic



4.4 Assembly Diagram

The following figure shows the assembly diagram of the MMA051AA device. In the die test assembly shown, both RFIN and RFOUT ports should utilize bias tees or DC blocks to isolate external circuits from the IC. VDD to the MMA051AA die is supplied through DC bypass caps of >10 nF (the actual value depends on the low-frequency bandwidth requirements of the application).

Figure 21 Assembly Diagram

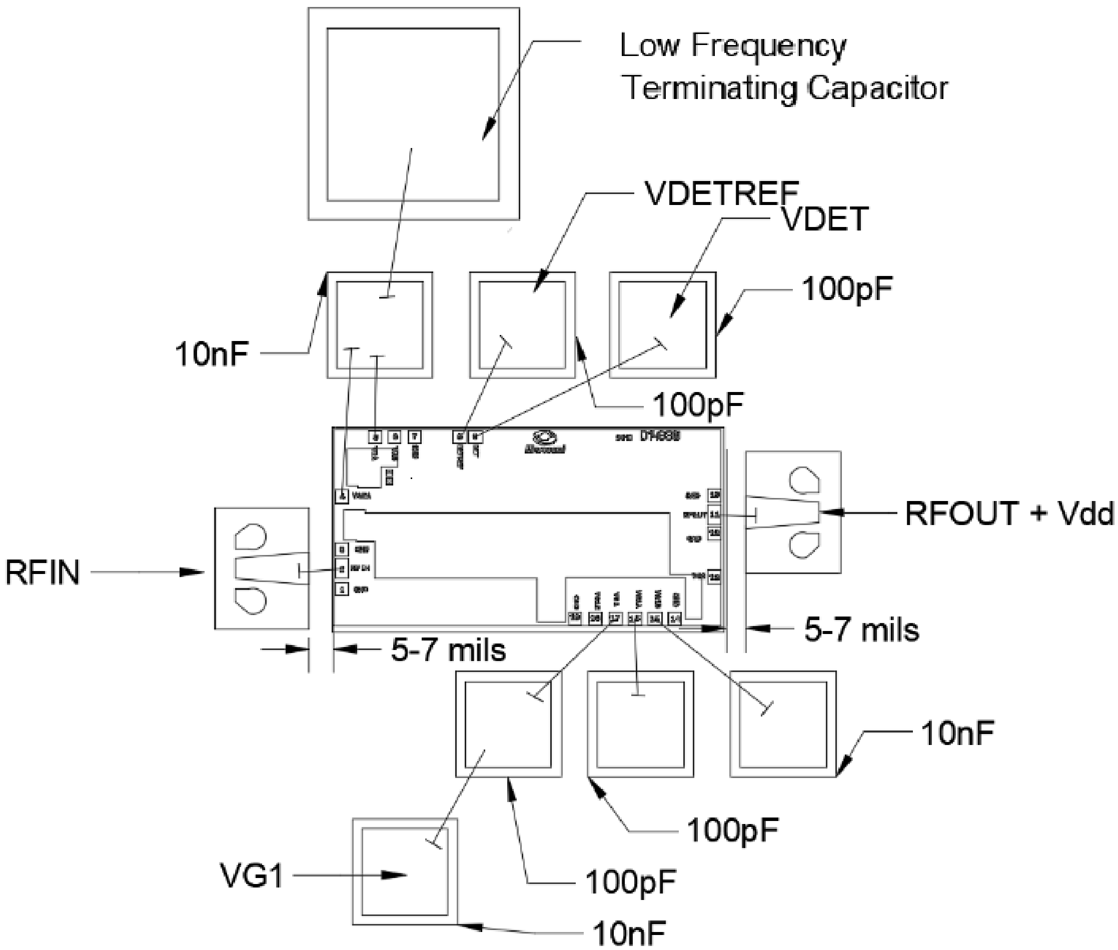


Table 5 List of Materials for the Evaluation Circuit of the MMA051AA

Items
10 nF 50 V Capacitors
Large Low Frequency Terminating Capacitors
100 pF Capacitors
1 mil Gold Bond Wire
RF Probe Launchers

Table 6 Bias Sequence

Bias Sequence
1) Set the gate voltage VG1 to -1V
2) Set drain voltage VDD to 10V
3) Adjust the gate voltage until the drain current is 350mA

5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01 GaAs MMIC Handling and Die Attach Recommendations.

6 Ordering Information

The following table shows the ordering information for the MMA051AA device.

Table 6 Packaging Information

Part Number	Package
MMA051AA	Die