


Helping Customers Innovate, Improve & Grow



Description

The PS-702 is a SAW Based Clock Oscillator that achieves low phase noise and very low jitter performance. The PS-702 is housed in an industry standard 6-Pad leadless ceramic package that is hermetically sealed. Packaging options include bulk or tape and reel.

Features

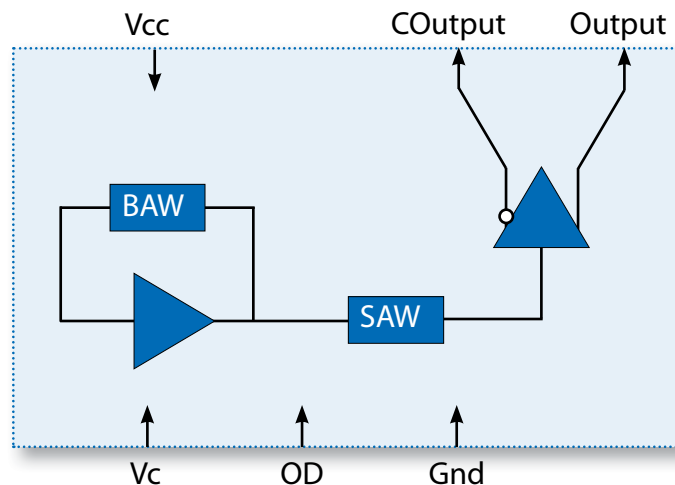
- Industry Standard Package, 5.0 x 7.5 x 2.0 mm
- ASIC Technology For Ultra Low Jitter
 - 0.100 ps-rms typical across 12 kHz to 20 MHz BW
 - 0.120 ps-rms typical across 50 kHz to 80 MHz BW
- Output Frequencies from 150 MHz to 1 GHz
- 3.3 V Operation
- LV-PECL or LVDS Configuration with Fast Transition Times
- Complementary Outputs
- Output Disable Feature
- Improved Temperature Stability over Standard SAW XO
- Product is free of lead and compliant to EC RoHS Directive 

Applications

Reference Clock for Wired and Wireless Products

Description	Standard
• 1-2-4 Gigabit Fibre Channel	INCITS 352-2002
• 10 Gigabit Fibre Channel	INCITS 364-2003
• 10GbE LAN / WAN	IEEE 802.3ae
• OC-192	ITU-T G.709
• SONET / SDH	GR-253-CORE Issue4

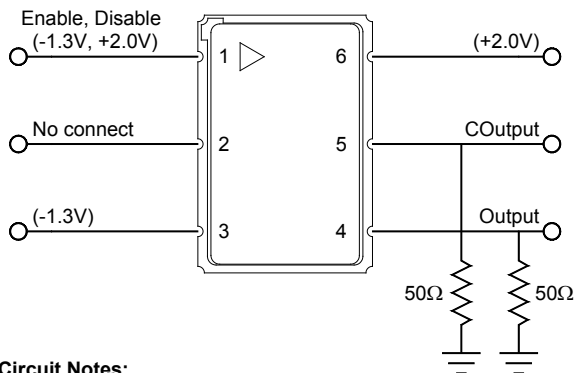
Block Diagram



Performance Specifications

Table 1: Electrical Performance					
Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ^{2,3}	V_{CC}	2.97	3.3	3.63	V
Current (No Load) ³	I_{CC}		55	70	mA
Frequency					
Nominal Frequency ^{1,2}	f_N	150		1000	MHz
Frequency Stability ^{1,2} (Ordering Option)	f_{STAB}		$\pm 50, \pm 100$		ppm
Aging ^{6,8}				10	ppm
Outputs					
Mid Level - LVPECL ^{2,3}		$V_{CC}-1.4$	$V_{CC}-1.25$	$V_{CC}-1.0$	V
Swing - LVPECL ^{2,3}		450	600	750	mV-pp
Mid Level - LVDS ^{2,3}			$V_{CC}-1.2$		V
Swing - LVDS ^{2,3}		250	450		mV-pp
Current ⁶	I_{OUT}			20	mA
Rise Time ^{5,6}	t_R			500	ps
Fall Time ^{5,6}	t_F			500	ps
Symmetry ^{2,3}	SYM	45	50	55	%
Jitter ^{6,7} (12 kHz - 20 MHz BW) 622.08 MHz	ϕJ		0.100	0.250	ps-rms
Jitter ^{6,7} (50 kHz - 80 MHz BW) 622.08 MHz	ϕJ		0.120	0.300	ps-rms
Period Jitter ⁹ , RMS (622.08 MHz)	ϕJ		2.5	3.0	ps-rms
Period Jitter ⁹ , Peak - Peak (622.08 MHz)	ϕJ		16	24	ps pk-pk
Operating Temperature ¹	T_{OP}	0/70, -20/70 or -40/85			°C
Package Size		5.0 x 7.5 x 2.0			mm

- 1] See Standard Frequencies and Ordering Information tables (Pg 7) for more specific information
- 2] Parameters are tested with production test circuit below (Fig 1).
- 3] Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
- 4] Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
- 5] Measured from 20% to 80% of a full output swing (Fig 2).
- 6] Not tested in production, guaranteed by design, verified at qualification.
- 7] Integrated across stated bandwidth per GR-253-CORE Issue4.
- 8] Tested with $V_C = 0.3V$ to $3.0V$ unless otherwise stated in part description
- 9] Broadband Period Jitter measured using Lecroy Wavemaster 8600A 6 GHz Oscilloscope, 250K samples taken



Test Circuit Notes:

- 1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
- 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
- 3) 50Ω Terminations are Within Test Equipment.

Fig 1: Test Circuit

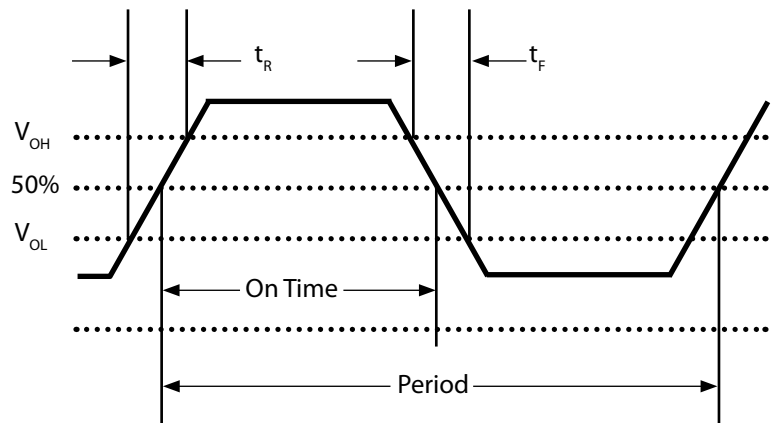
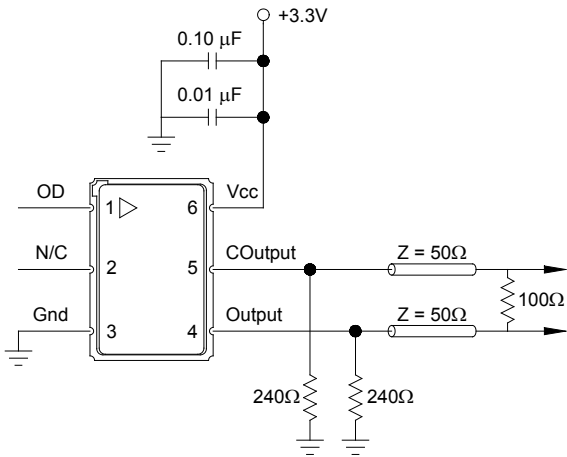


Fig 2: LV-PECL Waveform

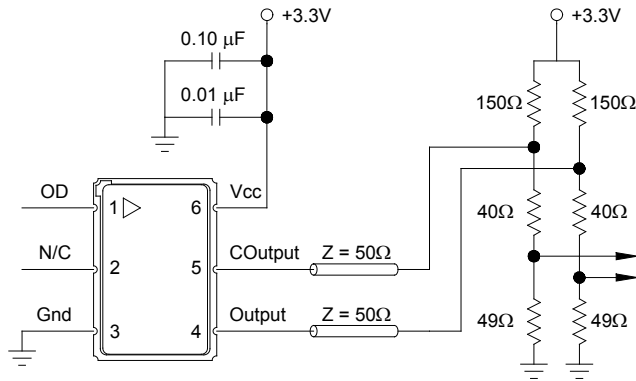
Absolute Maximum Ratings			
Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 4	V
Output Current	I_{OUT}	25	mA
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	260 / 40	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

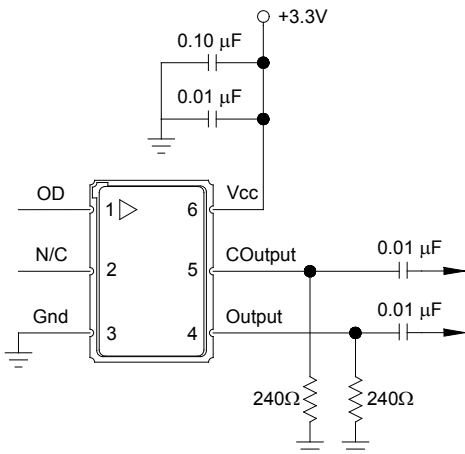
Suggested Output Load Configurations



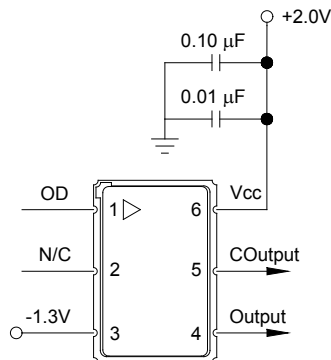
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.

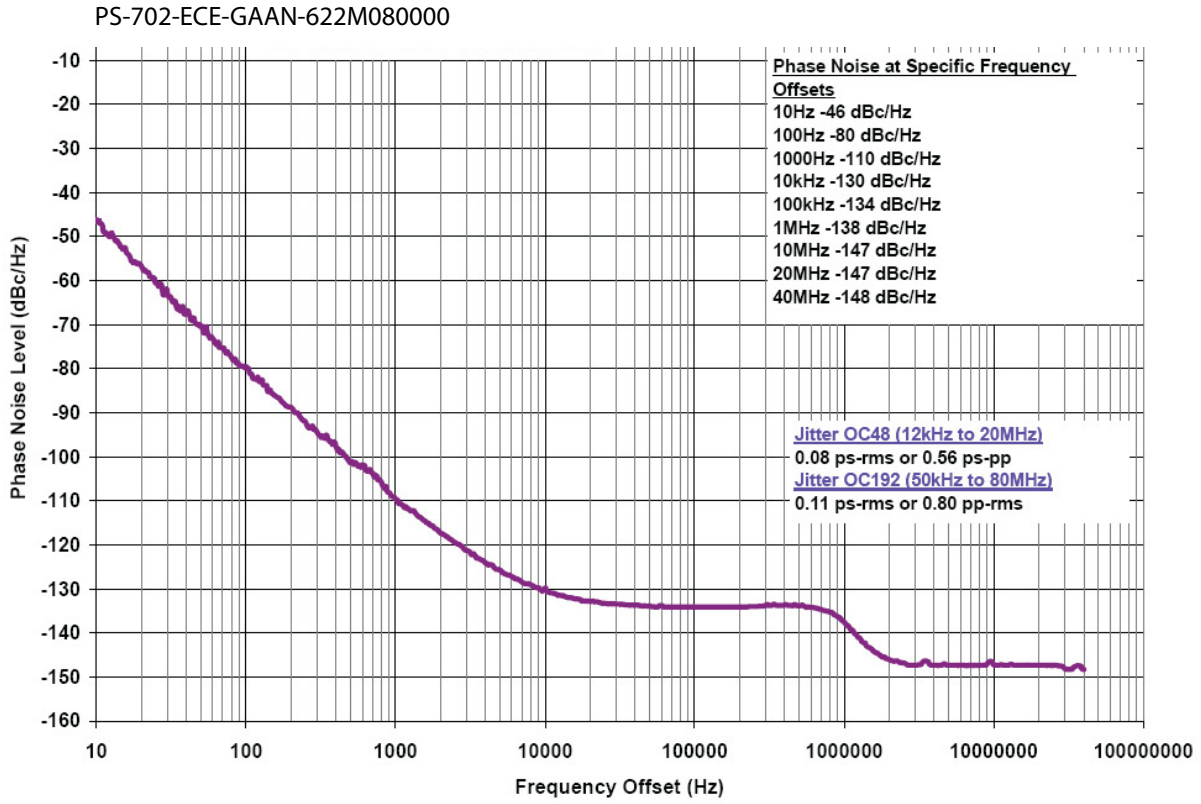


Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplies as shown. Similar to Figure 1.

Typical Characteristics - Phase Noise



Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The PS-702 family is capable of meeting the following qualification tests:

Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

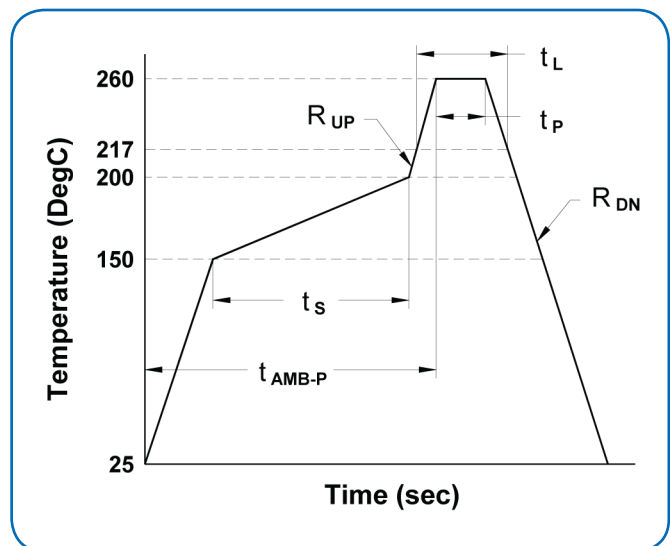
Although ESD protection circuitry has been designed into the PS-702 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	Minimum	Conditions
Human Body Model	1500V	MIL-STD-883, Method 3015
Man Man Model	200V	V/JESD22-A115-A

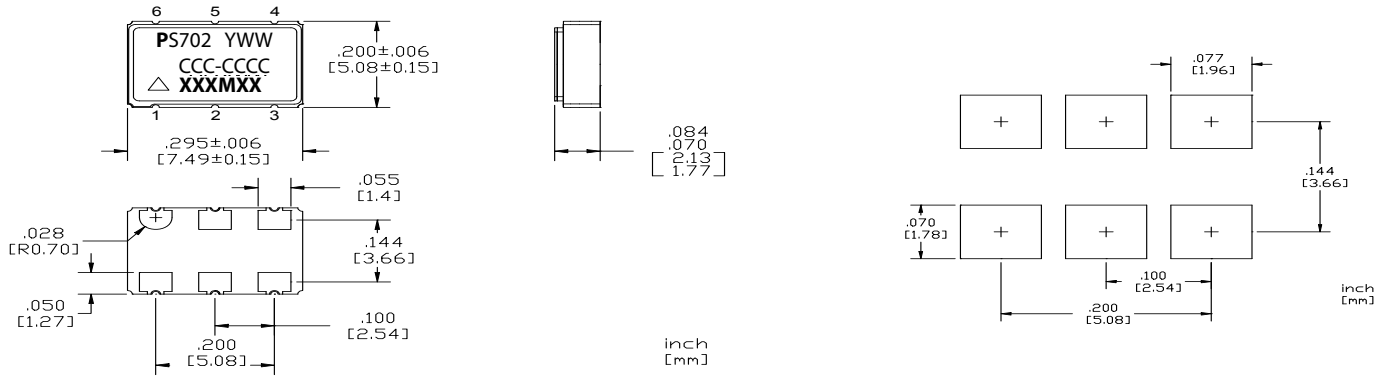
Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	Symbol	Value
PreHeat Time	t_s	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The PS-702 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating:
Electroless Gold Plate over Nickel Plate



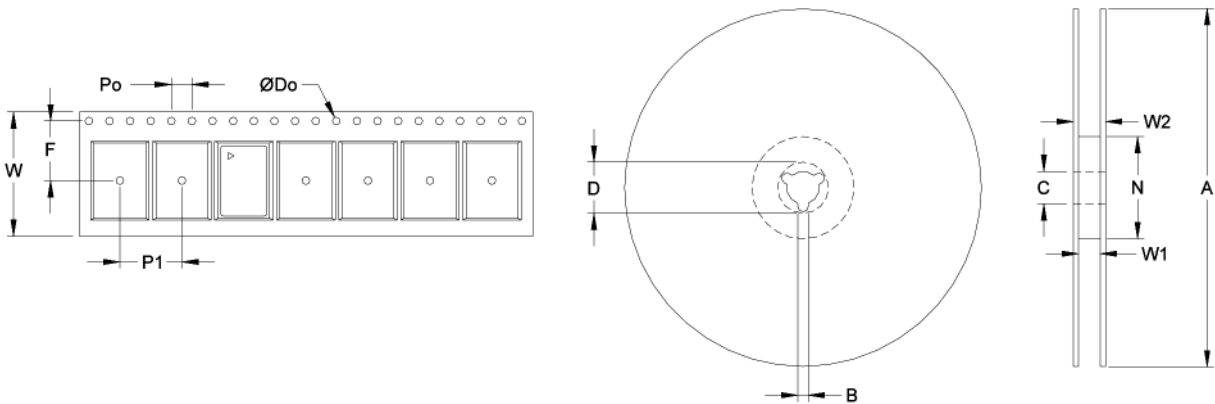
Outline Drawing & Pad Layout



Pin Out		
Pin	Symbol	Function
1	NC or OE ¹	NC or Enable = LV-CMOS logic 0 or Ground Disable = LV-CMOS logic 1 **see Note 1 below**
2	NC or OE ¹	NC or Enable = LV-CMOS logic 0 or Ground Disable = LV-CMOS logic 1 **see Note 1 below**
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V _{CC}	Power Supply Voltage (3.3V ±10%)

Note 1: For proper operation disable pin can not be left floating and a pin1 or pin 2 enable option must be ordered. See page 7 for alternative input logic operation

Tape & Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
PS-702	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

