


Helping Customers Innovate, Improve & Grow


VT-701

Description

Vectron's VT-701 Temperature Compensated Crystal Oscillator (TCXO) is a quartz stabilized, clipped sine wave output, analog temperature compensated oscillator, operating off either a 3.3 or 5.0 volt supply in a hermetically sealed 5x7 ceramic package.

Features

- CMOS Output
- Output Frequencies to 27 MHz
- Fundamental Crystal Design
- Optional VCXO Function available
- Gold over nickel contact pads
- Hermetically Sealed Ceramic SMD package
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

Applications

- FPGA's
- A/D's, D/A's
- Broadband Access Head End
- Wireless Communications
- Base Stations
- Point to point radios
- Broadband Access
- Test Equipment

Block Diagram

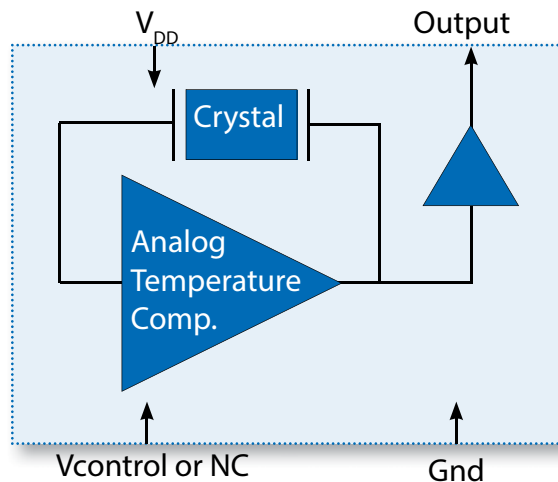
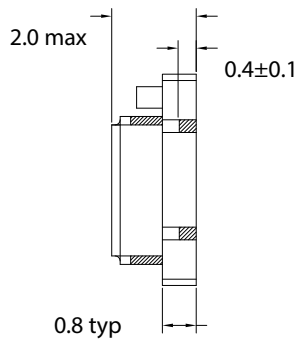
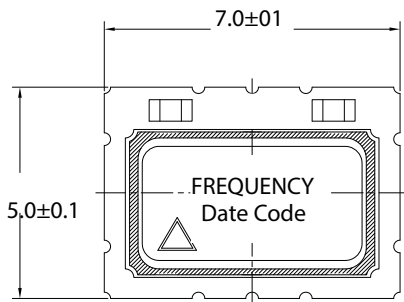


Table 1. Electrical Performance

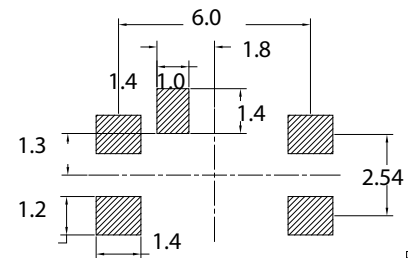
Parameter	Symbol	Min.	Typ	Max	Units
Output Frequency	f_o	5		27	MHz
Supply Voltage ¹ , Ordering Option	V_{DD}	+3.3 or +5.0			Vdc
Supply Current	I_{DD}			10	mA
Operating Temperature, Ordering Option	T_{OP}	0/55, -10/60, -20/70, -30/80, -40/85			°C
Stability Over T_{OP} , Ordering Option		$\pm 0.5, \pm 1.0, \pm 1.5, \pm 2.0, \pm 2.5, \pm 3.0, \pm 4.0, \pm 5.0$			ppm
Initial Accuracy, "No Adjust" Option				± 1.0	ppm
Power Supply Stability				± 0.3	ppm
Load Stability				± 0.2	ppm
Aging				± 1.0	ppm/yr
Pull Range, ordering option	TPR	$\pm 5, \pm 8, \pm 10, \pm 12$			ppm
Control Voltage to reach Pull Range		0.5		2.5	V
Control Voltage Impedance		1			Mohm
Output Level ²					
Output Logic High	V_{OH}	$0.8 * V_{DD}$			V
Output Logic Low	V_{OL}			$0.1 * V_{DD}$	V
Output Logic High Drive	I_{OH}			-4	mA
Output Logic Low Drive	I_{OL}	4			mA
Output Load				15	pF
Phase Noise, 10.000MHz					dBc/Hz
10Hz			-92		
100Hz			-116		
1kHz			-137		
10kHz			-149		
100kHz			-154		
Enable Disable ³ , Output Enabled	V_{IH}	$0.3 * V_{DD}$		$0.7 * V_{DD}$	
Output Disabled	V_{IL}				
Start Up Time				2	ms

1. The V-701 power supply pin should be filtered, eg, a 0.1 and 0.01 uf capacitor
2. The Output is DC coupled
3. Output is Enabled if E/D is left open

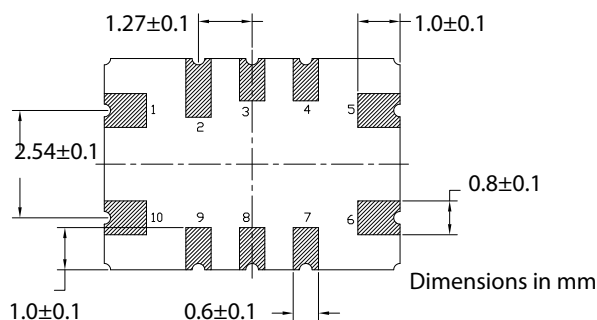
Outline Drawing



Recommended Pad Layout



Pad Layout mm

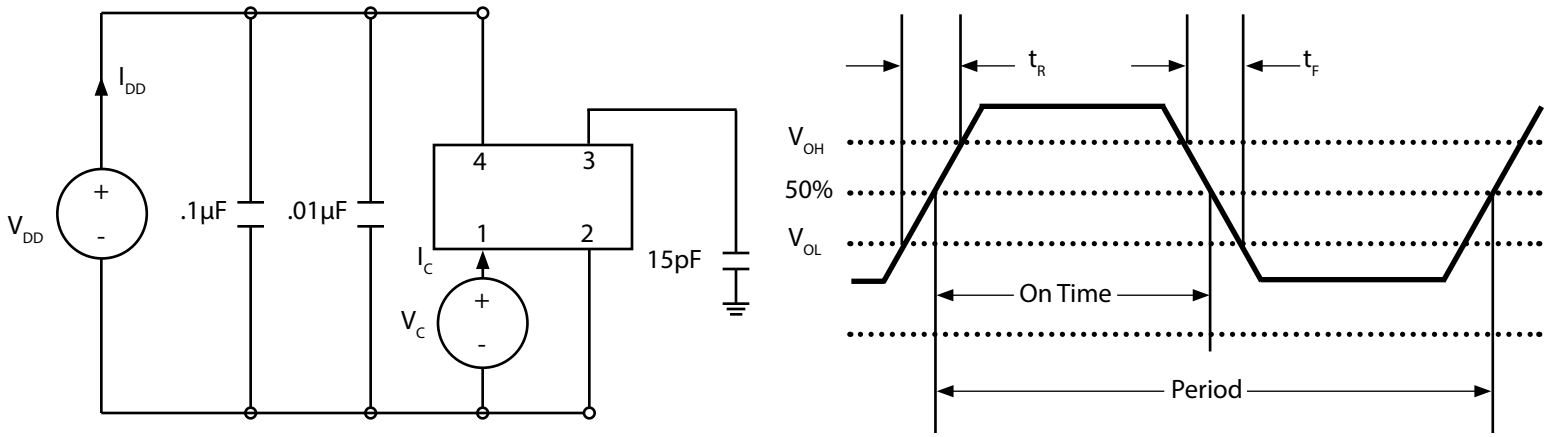


Dimensions in mm

Table 2. Pinout

Pin #	Symbol	Function
1	V_C	TCXO Control Voltage or Ground
2,3,4	NC	Make No Connection
5	GND	Electrical and Lid Ground
6	f_o	Output Frequency
7,8	NC	Make No Connection
9	E/D	Enable Disable
10	V_{DD}	Supply Voltage

Test Circuit



VCXO Function

VCXO Feature: The VT-701 can be ordered with a VCXO function for applications where it will be used in a PLL, or the output frequency needs fine tune or calibration adjustments. This is a high impedance input, 1Mohm, and can be driven with an op-amp or terminated with adjustable resistors etc. **Pin 1 should not be left floating on the VCXO optional device.**

“No Adjust” Option: In applications where the VT-701 will not be used in a PLL, or the output frequency does not need fine tune adjustments, the best device to use would be a VT-701-xxx-xxx0. By using the “no adjust” option, the circuit is simplified as V_C does not need to be adjusted or set to a predetermined voltage and pin 1 should be grounded (pin 1 can be left open but should not be set to a voltage such as an RF signal or power supply voltage).

Maximum Ratings

Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Although ESD protection circuitry has been designed into the VT-701, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.

ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefore can be used for comparison purposes.

Table 3. Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{STORE}	-55/125	°C
Supply Voltage	V_{DD}	6	V
Control Voltage	V_C	0/ V_{DD}	V
ESD, Human Body Model		1500	V
ESD, Charged Device Model		1000	V

Table 4. Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold over Nickel

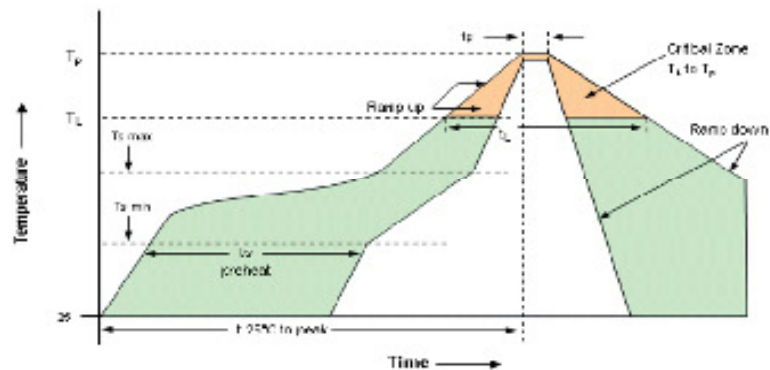
IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 5. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Parameter	Symbol	Value
PreHeat Time	t_s	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	t_L	150 sec Max
Time to Peak Temperature	t_{AMB-P}	480 sec Max
Time at 260°C	t_P	30 sec Max
Time at 240°C	t_{P2}	60 sec Max
Ramp down	R_{DN}	6°C/sec Max

Solderprofile:



Tape & Reel

Table 6. Tape and Reel Information

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	1.5	13	20.2	60	16.4	20.4	1000

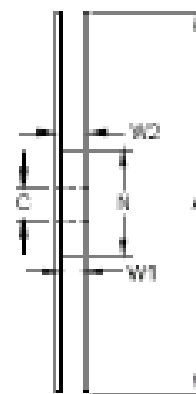
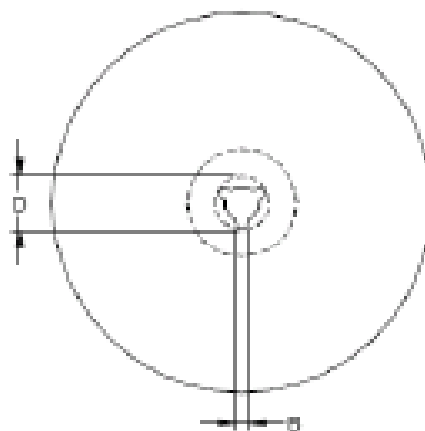
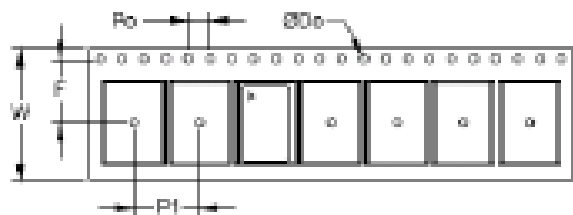


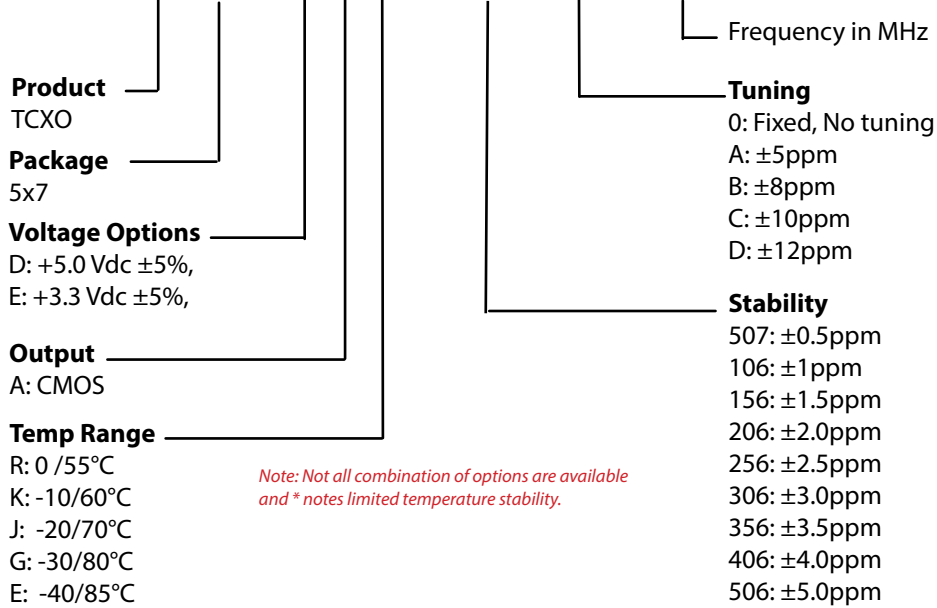
Table 7. Standard Frequencies (MHz)

Standard Frequencies

5.000*	6.400*	8.192	10.000	12.500*	12.800	13.000*	16.384	19.200	20.000
19.440	19.800	20.000	24.000	25.000	26.000	27.000			

Ordering Information

VT-701- E A G - X X X A- xxMxxxxxxx



Example: VT-701-EAG-206A-19M2000000

*** Add _SNPBDIP for tin lead solder dip**

Example: VT-701-EAG-206A-19M2000000__SNPBDIP

Revision History

Revision Date	Approved	Description
August 10, 2018	FB	Rev 0.4: Updated logo and contact information, added "SNPBDIP" ordering option



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