

RTG4 Proton Test Report

May 2020



a  **MICROCHIP** company

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in May 2020. The following is a summary of changes.

- Preliminary marks were removed.
- Changed "Testing" to "Test".

1.2 Revision 2.0

Revision 2.0 was published in June 2018. The following is a summary of changes in revision 2.0 of this document.

- The format of this document was updated to the latest template. As a result, DUT 1 and 2 Design content now appear in the same section, and DUT 1 and 2 Test Results content now appear in the same section.
- Tables in section "DUT 2 Proton Test Results" data changed from "Cross-Section/Block" to "Cross-Section/Bit"
- Table in section "DUT 1 and DUT 2 Proton SEL Test Results" data changed from "Cross-Section /Block" to "Cross-Section/FPGA"

1.3 Revision 1.0

Revision 1.0 is the initial release of this document published in February 2018.

2 Summary

This report presents the testing results of proton-induced single event effects in RTG4 device. Tested circuit component include fabric blocks: STMRFF, LSRAM, μ SRAM, and PLL at clock speeds of 1 MHz to 200 MHz. The results show that the RTG4 device is SEL immune; STMRFF is practically proton-SEU immune; and LSRAM/ μ SRAM SEU rates are low as expected, and can be mitigated using optional built-in EDAC circuits.

There is a technique¹ to convert heavy-ion SEU results, expressed in a Weibull four parameters plot, to proton SEU results. The results by applying this methodology on SEU of LSRAM and μ SRAM show that the worst-case result has only 24% difference between derived and tested proton SEU data. In the future, proton SEU performance will be predicted using this method if heavy-ion Weibull data is available.

1. L. Edmonds and F. Irom, "Extension of a proton SEU cross section model to include 14 MeV neutrons," IEEE Trans. Nucl. Sci., vol. 55, no. 1, pp. 649-655, Feb. 2008.

3 Proton Testing

The objective of this test is to obtain proton cross-section for fabric blocks on Microsemi's RTG4 FPGA. This is the first Proton Test conducted on this family. The blocks tested included the STMRFFs, LSRAMs, μ SRAMs and the PLLs operating in CCC internal and PLL internal feedback modes.

3.1 Test Facility

The testing uses the 200 MeV proton-beam source at Massachusetts General Hospital in Boston, MA. The following table lists the testing parameters.

Table 1 • Proton Beam Parameters

| Condition | Setting |
|--------------------|--------------------|
| Beam Energy | 200.5 MeV |
| Temperature | Room |
| Bias | Nominal |
| Sample Preparation | Lidless RTG4 parts |

3.2 Device-Under-Test (DUT) Designs

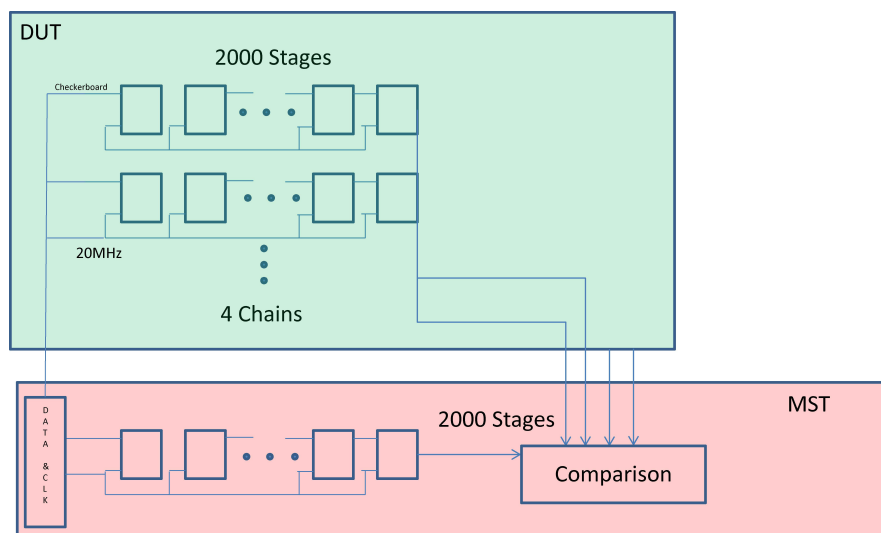
There are two Device-Under-Test (DUT) designs: DUT 1 and DUT 2.

3.2.1 DUT 1 Designs

DUT 1 has three testing designs:

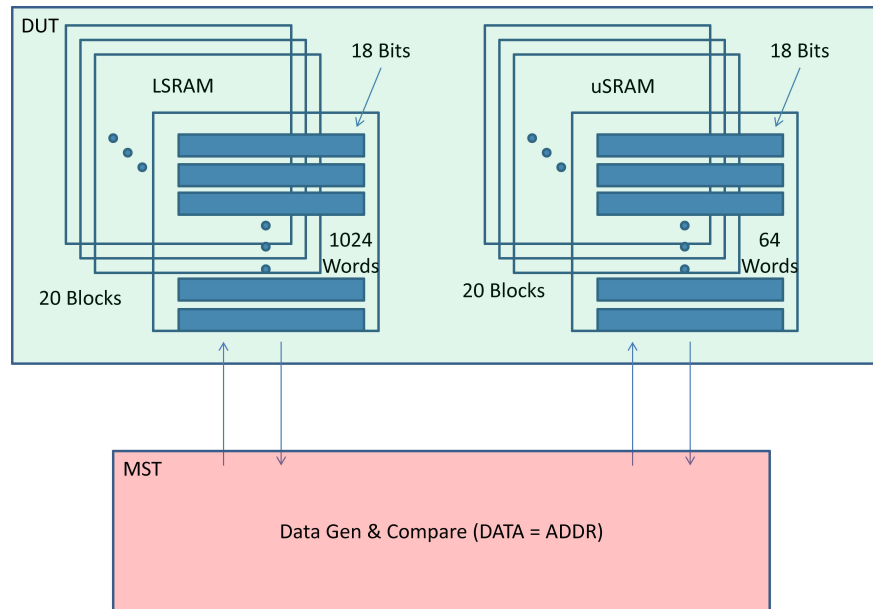
1. STMRFF design: four chains of 2000 stages run at 20MHz with a checkerboard pattern. The following illustration shows the block diagram for this design. The DUT is represented in the top block and the control chip in the bottom block.

Figure 1 • STMRFF Testing Design



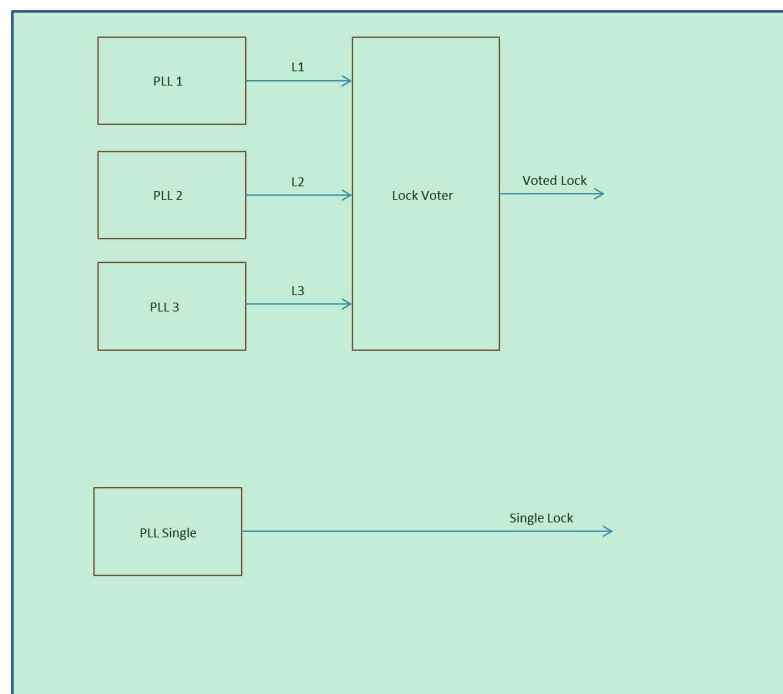
- LSRAM and μ SRAM designs: each has 20 Blocks of 18-bit words with total 1024 words per each block, and each word stores its address as the data. The LSRAM and μ SRAM blocks are used without the optional built-in error detection and correction encoding circuits. The following illustration shows the block diagram for this design. The DUT is represented in the top block and the control chip in the bottom block.

Figure 2 • LSRAM and μ SRAM Testing Designs



- Configures PLL into single mode using CCC internal loopback and into TMR mode using PLL internal loopback. Both modes have the LOCK signal to monitor their functionality. The following illustration shows the block diagram for this design.

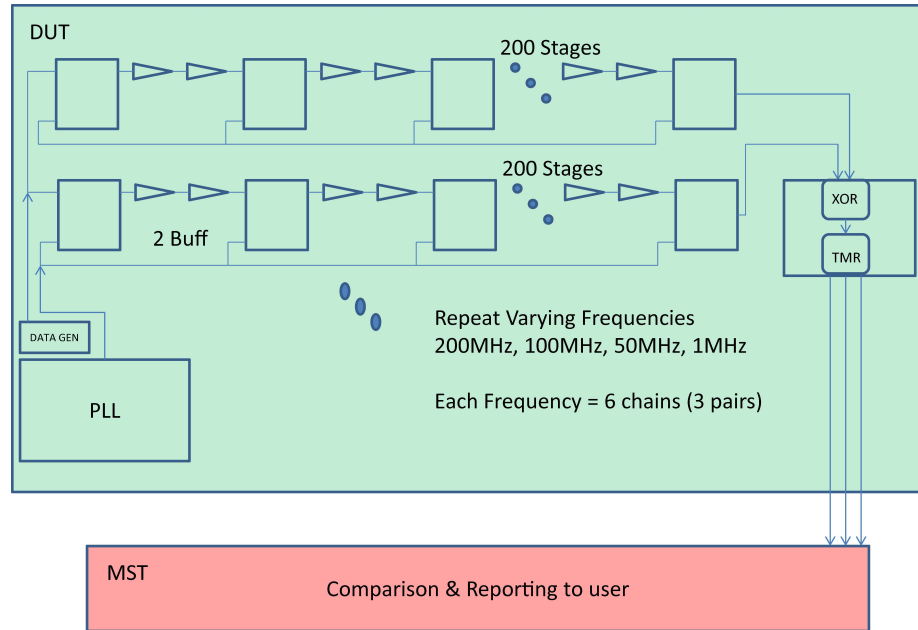
Figure 3 • Single and TMR PLL Testing Design



3.2.2 DUT 2 Design

The DUT 2 design has 24 parallel chains of 200 stages STMRFF with two buffers between two adjacent FFs. There are four groups, each group with six chains and running by DUT-PLL generated clocks of 1, 50, 100, or 200 MHz. The PLL lock signal is monitored to identify any loss of lock. The outputs of 2 parallel chains running at the same frequency are XOR'ed to detect errors. This results in 1 monitor signal for a pair of FF chains (i.e 12 monitors for 24 chains). The monitor is then TMR'ed and sent to the Master chip which resides on another board. The Master chip is not irradiated. The following illustration shows the block diagram for the DUT 2 design.

Figure 4 • DUT 2 Design



3.3 Test Results

3.3.1 DUT 1 Proton Test Results

The following table summarizes proton-irradiation induced error rates in fabric elements including STMRFF, LSRAM and μ SRAM. In the last column, the calculated error rates use JPSS-1 environment.

Table 2 • Fabric Results Summary

| Circuit | Error Counts | Fluence (p/cm ²) | Cross-Section/bit (cm ²) | Error/bit/day |
|-----------------|--------------|------------------------------|--------------------------------------|---------------|
| STMRFF – 20 MHz | 1 | 5.10158E+11 | 2.45022E–16 | 2.08E–09 |
| LSRAM | 1599 | 5.10158E+11 | 8.5024E–15 | 7.21E–08 |
| μ SRAM | 73 | 5.10158E+11 | 6.21063E–15 | 5.26E–08 |

The SEU hardened STMRFF block only shows one error over the whole testing session. In fact, the facility and testing system can generate noise to cause very small background errors. Further investigation would be required to exclude or include this as proton-induced. Practically, in almost all cases, one can ignore the effect with minute cross-section.

All SRAM errors are single bit errors, i.e using EDAC techniques can mitigate them.

Observing the lock monitor indicated that there were no occurrence of loss of lock in either PLL Single or TMR configurations. The following table summarizes proton-irradiation induced error rates in PLL Single and TMR configurations.

Table 3 • PLL Results Summary

| Circuit | Error Counts | Fluence Tested (p/cm ²) | Cross-Section/PLL (cm ²) | Error/bit/day |
|------------|--------------|-------------------------------------|--------------------------------------|---------------|
| PLL Single | 0 | 5.10158E+11 | <1.96018E-12 | <1.66E-05 |
| PLL TMR | 0 | 5.10158E+11 | <1.96018E-12 | <1.66E-05 |

3.3.2 DUT 2 Proton Test Results

The following tables display the proton induced soft errors or SEU in each group. Because the error rate of turning SET filter “ON” or “OFF” is statistically about the same, the results shown in the following table combine error counts.

Table 4 • STRMRFF: Combined Data of SET Filter On and Off

| Frequency | Error Counts | Fluence (p/cm ²) | Cross-Section/bit (cm ²) |
|-----------|--------------|------------------------------|--------------------------------------|
| 200 MHz | 1 | 4.10328E+11 | 2.0309E-15 |
| 100 MHz | 1 | 4.10328E+11 | 2.0309E-15 |
| 50 MHz | 0 | 4.10328E+11 | <2.031E-15 |
| 1 MHz | 0 | 4.10328E+11 | <2.031E-15 |

The following table displays results with the SET filter set to “OFF”. In the last column, the calculated error rates use JPSS-1 environment.

Table 5 • STRMRFF: Data of SET Filter Off

| Frequency | Error Counts | Fluence (p/cm ²) | Cross-Section/bit (cm ²) | Error/bit/day |
|-----------|--------------|------------------------------|--------------------------------------|---------------|
| 200 MHz | 1 | 2.0016E+11 | 4.16334E-15 | 3.53E-08 |
| 100 MHz | 0 | 2.0016E+11 | <4.16334E-15 | <3.53E-08 |
| 50 MHz | 0 | 2.0016E+11 | <4.16334E-15 | <3.53E-08 |
| 1 MHz | 0 | 2.0016E+11 | <4.16334E-15 | <3.53E-08 |

The following table displays results with the SET filter set to “ON”. In the last column, the calculated error rates use JPSS-1 environment.

Table 6 • STRMRFF: Data of SET Filter On

| Frequency | Error Counts | Fluence (p/cm ²) | Cross-Section/bit (cm ²) | Error/bit/day |
|-----------|--------------|------------------------------|--------------------------------------|---------------|
| 200 MHz | 0 | 2.10168E+11 | <3.96508E-15 | <3.36E-08 |
| 100 MHz | 1 | 2.10168E+11 | 3.96508E-15 | 3.36E-08 |
| 50 MHz | 0 | 2.10168E+11 | <3.96508E-15 | <3.36E-08 |
| 1 MHz | 0 | 2.10168E+11 | <3.96508E-15 | <3.36E-08 |

In summary, only two errors occurred at clock running at high frequencies of 100 MHz and 200 MHz. As mentioned before, these two single errors could be background-noise induced.

3.3.3 DUT 1 and DUT 2 Proton SEL Test Results

The following table summarizes the experiment results of proton-induced single event latch-up (SEL). The data are coming from two DUTs, biased at nominal VDD and irradiated at room temperature. Note that these SEL test data are incidental and considered as a sanity check. The fact that RTG4 is immune to SEL had been proved by heavy-ion irradiation by very high, approximate 103 MeV-cm²/mg, LET heavyions and at approximately 100 °C.

Table 7 • SEL Results Summary

| Phenomenon | Occurrences | Fluence (p/cm ²) | Cross-Section/bit (cm ²) | Error/unit/day |
|------------|-------------|------------------------------|--------------------------------------|----------------|
| SEL | 0 | 9.20486E+11 | <1.08638E-12 | <9.24E-06 |

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