RTG4 PLL SEE Test Results

July 10, 2017
Revised March 29, 2018
Revised July 31, 2018

Radiation Group

I. Introduction

This document disseminates recently acquired single-event-effects (SEE) data on the phase-locked-loop (PLL) in RTG4. The contents are the heavy-ion test results of regular PLLs in the clock conditioning circuits (CCC), but does not include data on the PLLs in the serial transceivers.

There are three modes to implement PLL in the CCC: the first uses a clock externally located outside the RTG4 as the source to feed the unhardened PLL; the second uses the triple-module-redundant (TMR) hardened PLL; the third uses the inside RC oscillator as the source to feed the unhardened PLL. The following sections present the PLL single event effects of the PLLs observed in heavy-ion beam test. From the test data Weibull curves were generated and fitting parameters were extracted. CREME96 was used to calculate the upset rates under standard conditions.

II. External-Clock-PLL Heavy-Ion SEE Test Results CCC-Internal Feedback – Single Instance Mode

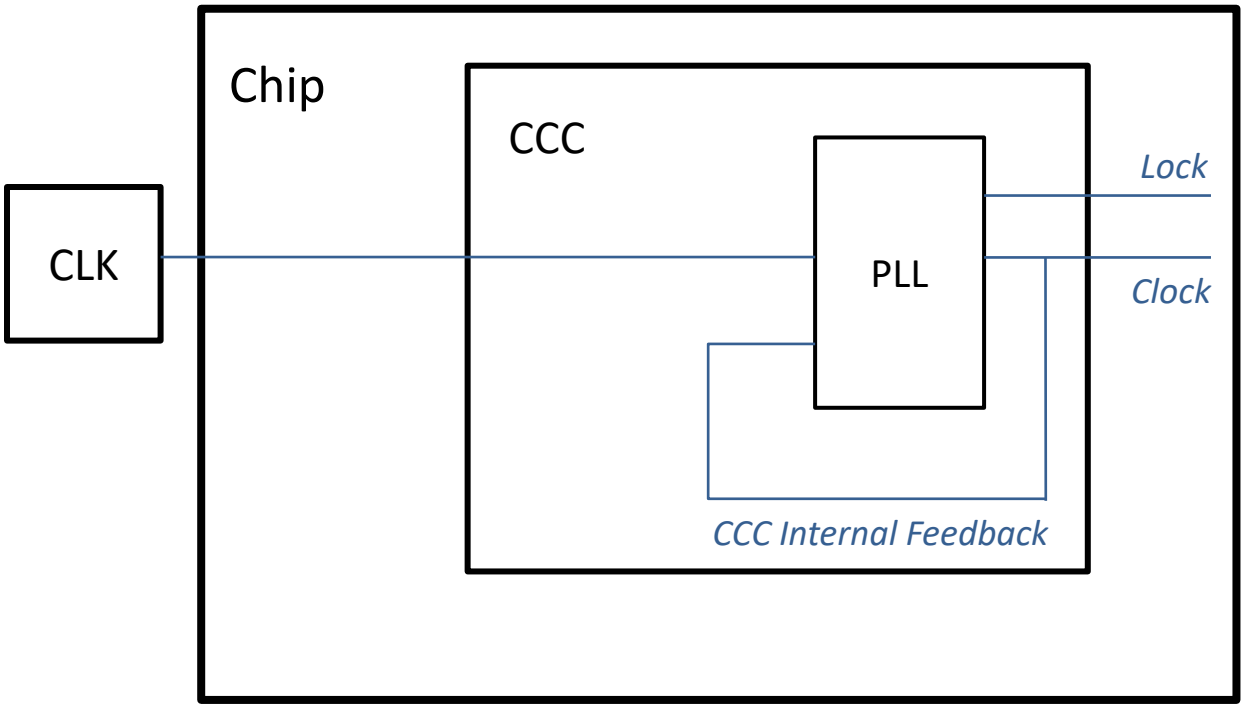

Fig. 1 Block diagram illustrates an external clock feeding into single PLL with CCC-internal feedback.

Fig. 1 shows an external clock of 20MHz feeding the unhardened PLL and generating four (4) clocks with frequency of 1MHz, 50MHz, 100MHz, and 200MHz. Each generated clock controls a chain of 200 flip-flops (FF). A checkerboard data pattern is the input to these chains, and outputs are monitored to identify single event upsets (SEU). Heavy ions used for irradiation have LET of 8.9, 14.2, 22, 34.7, and 64.7MeV-cm^2/mg. Results in below show two (2) modes of non-destructive functional interruption, Fig. 2 plots their cross-sections versus LET, and Table 1 displays the extracted Weibull parameters.

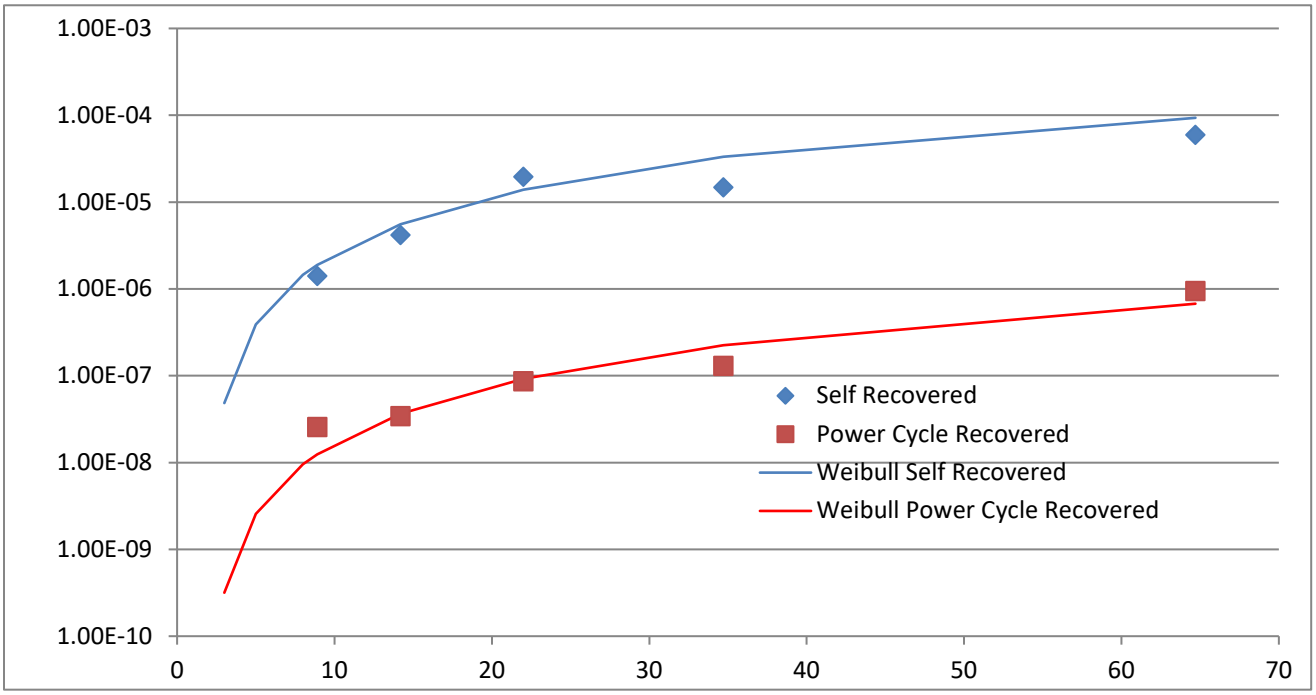

Fig. 2 Cross-section versus LET of Single Instance PLL-upset modes

- Mode 1: PLL lost lock when the output clock has gone out of phase with respect to the input reference clock. This mode of failure is self-recoverable and no reset is required.
- Mode 2: The output clock stopped toggling and it needed an asynchronous reset or power-cycle to the PLL to recover the function. In this particular test, it was power cycling to recover the PLL function. The output stopped toggling displayed a significant decrease in current across the chip as well as data stopped flopping through shift register chains.

Table 1 Single Instance PLL-Upset Weibull Parameters

	L0 (MeV·cm^2/mg)	W (MeV·cm^2/mg)	S	A0 (cm^2)
Self-Recover	2	80	1.9	2.00E-04
Power-Cycle-Recover	2	100	1.9	2.00E-06

III. External-Clock-PLL Heavy-Ion SEE Test Results PLL-Internal Feedback – TMR Mode

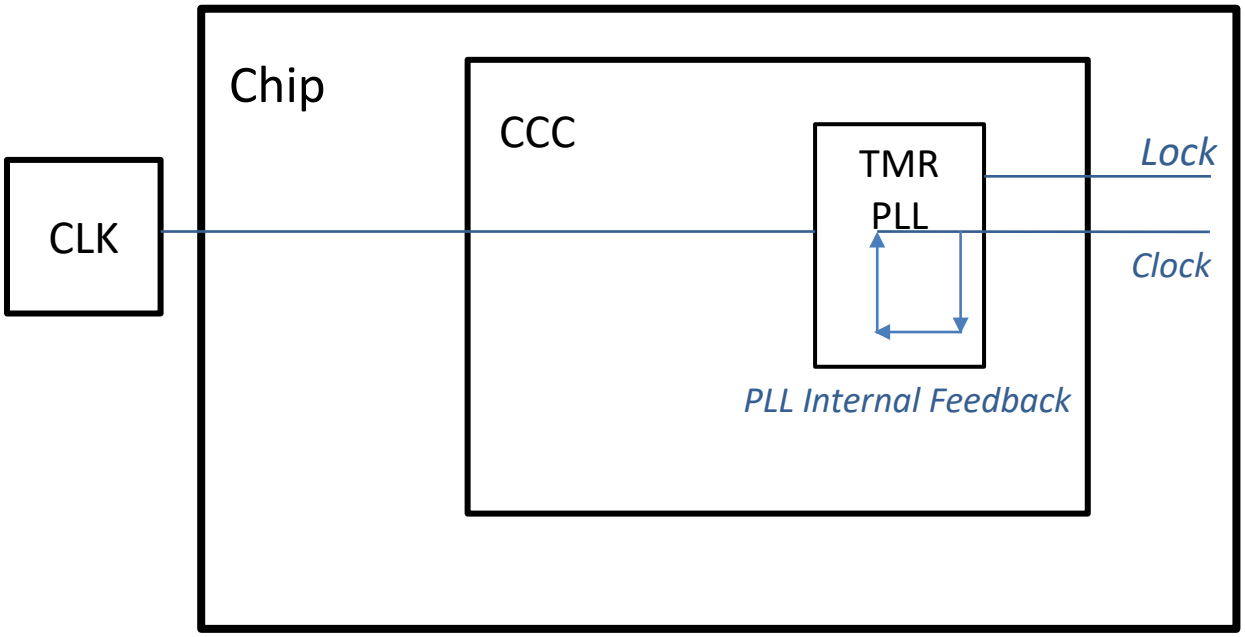

Fig. 3 Block diagram illustrates an external clock feeding into TMR PLL with PLL-internal feedback.

As shown in Fig. 3, an external clock of 20MHz is the source to feed a TMR PLL in PLL-internal feedback mode. The TMR PLL generates four (4) clocks with frequency of 1MHz, 50MHz, 100MHz, and 200MHz. Each generated clock controls a chain of 200 FF. A checkerboard data pattern is the input to these chains. Outputs are monitored to identify and count the numbers of SEU. Heavy ions used to irradiate the device-under-test (DUT) are with LET of 8.9, 14.2, 22, 34.7, and 64.7MeV-cm^2/mg.

When the PLL is in triple redundant configuration and PLL Internal feedback mode, a loss of lock will not self-recover and requires assertion of the PLL_ARSTN_N reset input to regain lock. During this time, the clock output from the triple redundant PLL will continue to run, but the quality of the clock (frequency stability, jitter) has not been determined. Fig. 4 shows the cross-sections versus LET data and the Weibull curve, with extracted parameters displayed in Table 2.

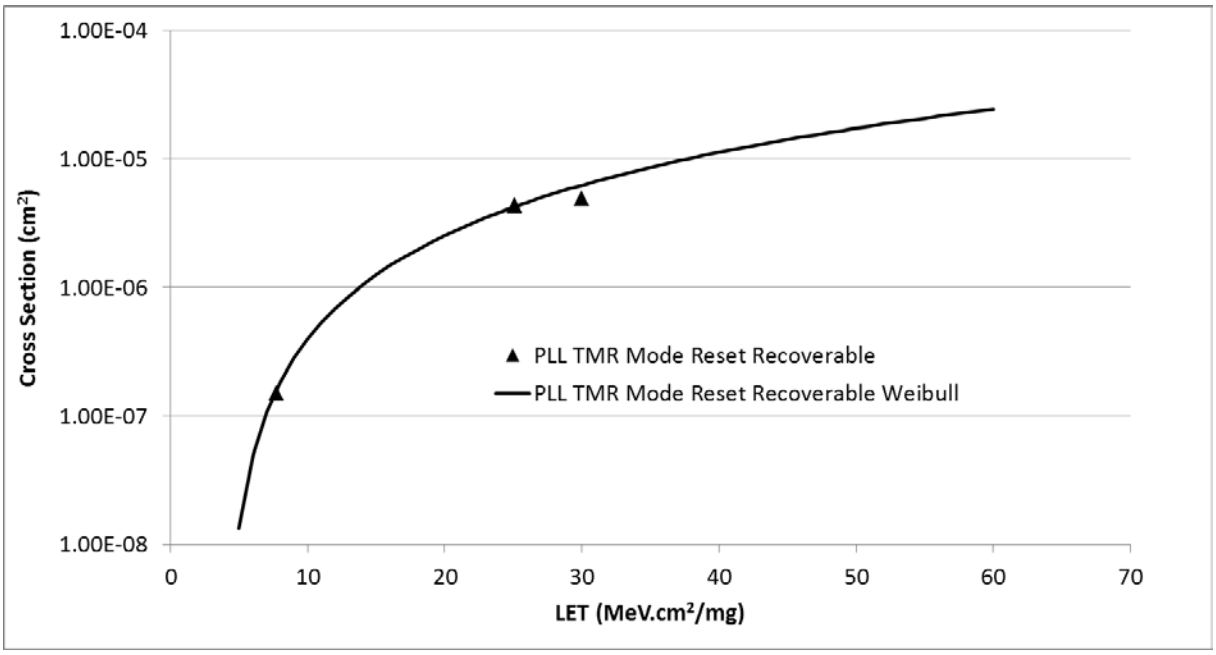

Fig. 4 Cross-section versus LET of TMR PLL Loss of Lock Reset Recoverable

Table 2 TMR PLL Mode Loss of Lock Reset Recoverable Weibull Parameters

	L0 (MeV·cm²/mg)	W (MeV·cm²/mg)	S	A0 (cm²)
External-Clock-PLL TMR Mode Reset Recoverable	4	110	1.9	1.00E-04

IV. OSC-PLL Heavy-Ion SEE Test Results

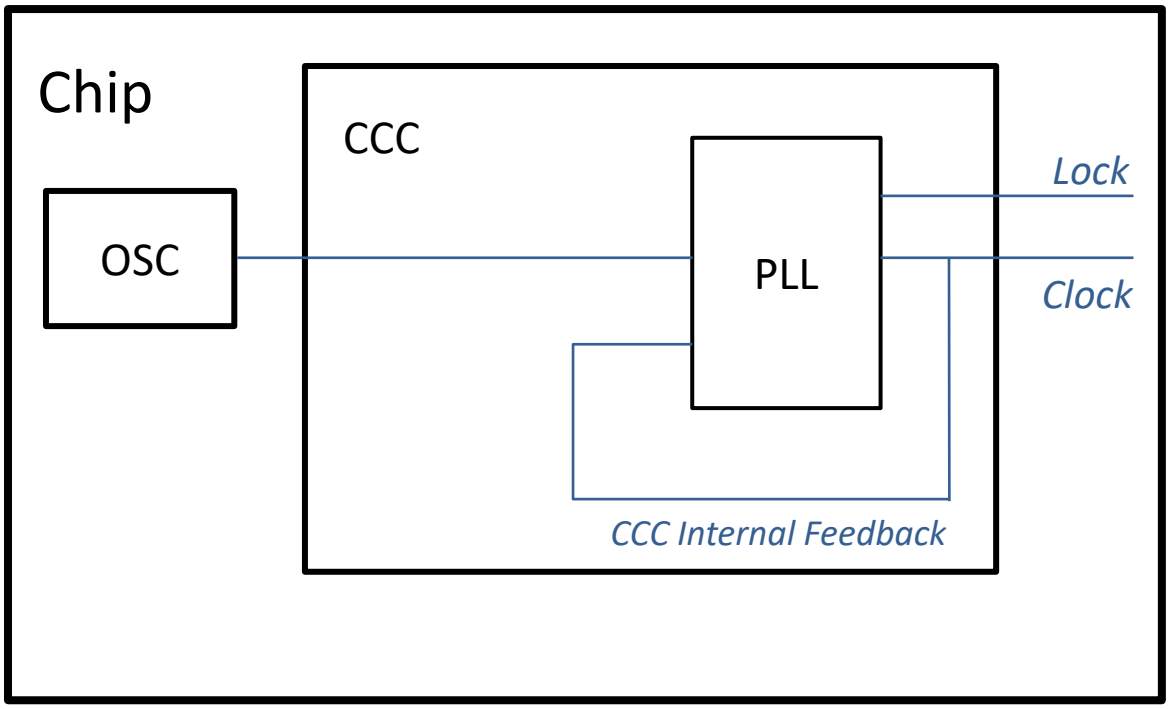

Fig. 5 Block diagram illustrates an internal oscillator feeding into single PLL with CCC-internal feedback.

Fig. 5 shows an on-chip RC-oscillator feeding the PLL to perform the same testing as before. Fig. 6 plots the testing results and Table 3 displays the extracted Weibull parameters. Note that the cross-sections in Fig. 6 is due to the combined SEU of OSC and PLL, therefore they are larger than those in Fig. 2 which only shows the PLL SEU only.

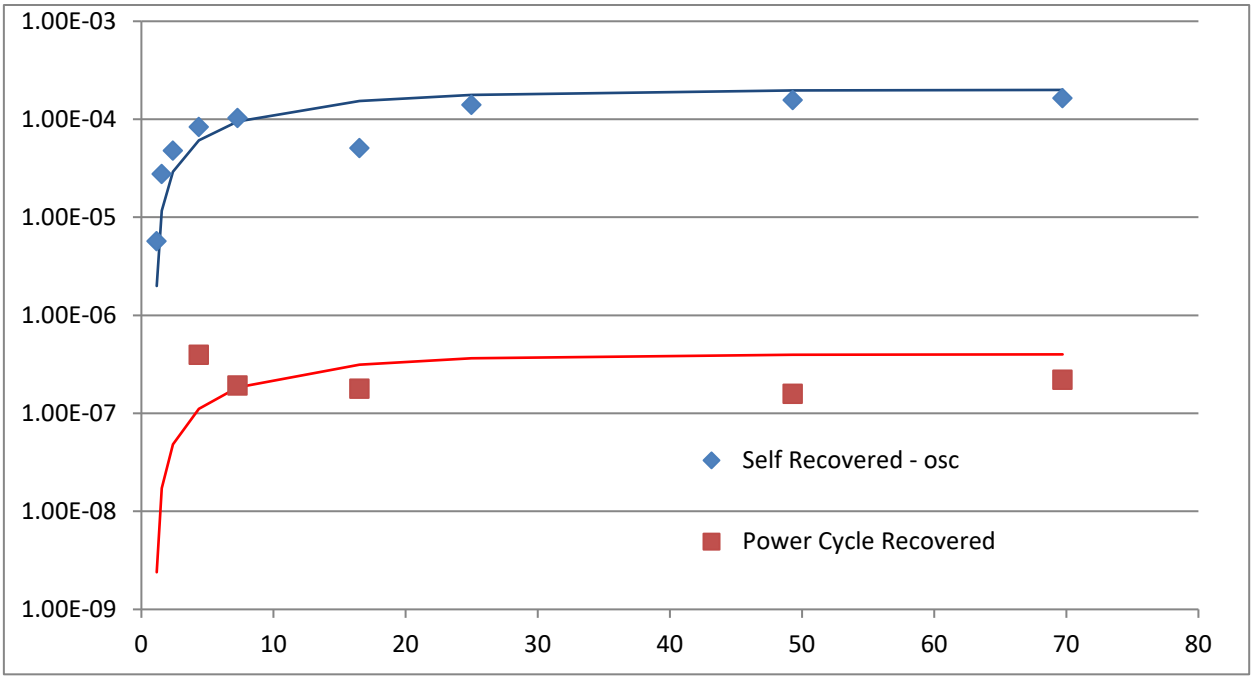

Fig. 6 Cross-section versus LET of OSC-PLL upset modes: Self-Recoverable and Power-Cycle Recoverable.

Table 3 OSC-PLL Upset Weibull Parameters

	L0 (MeV·cm²/mg)	W (MeV·cm²/mg)	S	A0 (cm²)
Self-Recover	1.1	10	0.9	2.00E-04
Power-Cycle-Recover	1.1	10	1.0	4.00E-07

V. Upset Rate in Orbit

Using extracted Weibull parameters, the PLL upset rates at geosynchronous orbit in solar-minimum environment with100ml Aluminum shielding are calculated using CREME96 and displayed in table 4.

Table 4 Orbital Upset and Event Rates

External-Clock-PLL Single Instance Self-Recover Upset Rate	8.28E-05 upset/PLL/day
External-Clock-PLL Single Instance Reset Recoverable Upset Rate	4.00E-07 upset/PLL/day
External-Clock-PLL TMR Mode Self-Recover Upset Rate	Not applicable
External-Clock-PLL TMR Mode Reset Recoverable Upset Rate	1.88E-05 upset/PLL/day
OSC-Clock-PLL Self-Recover Upset Rate	4.81E-03 events/PLL/day
OSC-Clock-PLL Power-Cycle-Recover Upset Rate	7.44E-06 events/PLL/day

VI. Revision History

7/10/2017 Initial version

3/29/2018 Clarified that the tests were performed on unhardened single instance PLL,
Corrected typo in Table 1 (cross section A0 for power-cycle-recoverable is 2.00E-6 not 2.00E-7)
Recalculated orbital upset rates in Table 3

7/31/2018 Added results from testing on triple-redundant PLL
Corrected External Clock single-instance Power-Cycle Recover upset rate from 4.00E-7 to 5.71E-7 upsets/PLL/day in Table 4 (was Table 3 in prior versions)