

Synopsys[®], Inc.

690 East Middlefield Road Mountain View, CA 94043 USA Website: www.synopsys.com

Synopsys® FPGA Design Microsemi Edition Release Notes

Includes Synplify Pro® and Identify® Version N-2017.09M-SP1, January 2018

Release Note Topics

About the Release	2
Feature and Enhancement Highlights	2
Identify Tool Device Support	2
Recommended Versions of Compatible Tools	3
Platforms	4
Documentation	5
Known Problems and Solutions	5 6
Limitations	8

Compiled 26 January 2018

About the Release

This N-2017.09M-SP1 release includes software features and enhancements for the Synplify Pro® and Identify Microsemi Edition products. For the complete summary of features and enhancements supported in this release, see Feature and Enhancement Highlights below.

Feature and Enhancement Highlights

The following table summarizes the supported features and enhancements:

Feature	Description			
Features in the N-2017.09M-SP1 Release				
INIT Value Packing Support for LSRAM and URAM blocks in PolarFire	INIT value packing is supported for RAM1K20 and RAM64x12 RAM blocks in the PolarFire device. It is also supported for ECC mode of RAM1K20 and SeqShifts inferred as URAMs. Reference->Designing with Microsemi->Microsemi RAM Implementations			
Features in the N-2017.09 Release				
HDL Analyst® Tool Enhancements	 The next-generation HDL Analysis tool is enabled by default. This version contains many new and improved features, such as: Multi-threaded Find improvements New schematic preferences Dissolving of ports Handling of partially dissolved nets Crossprobing to objects in a source file from the HDL Analyst schematic User Guide->Analyzing with HDL Analyst->Working in the Schematic The HDL Analyst tool also supports new and updated Tcl and find commands. Command Reference->Tcl Commands->analyst and Tcl Commands->design 			

Identify Tool Device Support

The Identify tool supports the device families shown in the table below. You must select devices from the synthesis tool, which get passed to the Identify Instrumentor in the synthesis project file. If you specify a library from the synthesis tool that is not supported in the Identify tool, then this results in a "device not supported" message when launching the Identify Instrumentor.

Microsemi
Fusion
IGLOO
IGLOO PLUS
IGLOO2
PolarFire
ProASIC
ProASIC3
ProASIC3E
ProASIC3L
RTG4
SmartFusion
SmartFusion2

Recommended Versions of Compatible Tools

The FPGA design tools are tested with specific versions of other compatible Synopsys and third-party tools. The recommended versions of these tools are listed below.

Compatible Versions of Synopsys Tools

The table lists the recommended version for VCS:

Tool	Recommended Version
VCS	L-2016.06-SP1

Platforms

The software is supported on the platforms listed below:

Windows	 Windows 10 Professional or Enterprise (64-bit) 		
	 Windows 8.1 Professional or Enterprise (64-bit) 		
	 Windows 7 Professional or Enterprise (64-bit) 		
	 Windows Server 2016 (64-bit) 		
	 Windows Server 2012 R2 (64-bit) 		
	 Windows Server 2008 R2 (64-bit) 		
Linux	All Linux platforms require 32-bit compatible libraries.		
	 CentOS 6.6 or later/7.1 or later (64-bit) 		
	 Red Hat Enterprise Linux 6.6 or later/7.1 or later (64-bit) 		
	 SUSE Linux Enterprise 11-SP1 or later/12 or later (64-bit) 		

Documentation

The following documents are included with the Synopsys FPGA synthesis product.

Document	Access
User Guide	Online help, PDF
Reference Manual	Online help, PDF
Attribute Reference Manual	Online help, PDF
Command Reference Manual	Online help, PDF
Language Support Reference Manual	Online help, PDF
Messages Reference Manual	Online help
Identify Instrumentor User Guide	Online help, PDF
Identify Debugger User Guide	Online help, PDF
Identify Debugging Environment Reference Manual	Online help, PDF

Known Problems and Solutions

The current known problems in the tool are divided into the following categories:

- FPGA Synthesis Known Problems and Solutions, on page 5
- FPGA and Identify Platform-Specific Known Problems and Solutions, on page 6
- Identify Tool Known Problems and Solutions, on page 6

FPGA Synthesis Known Problems and Solutions

The following problem applies to supported features in the Synplify Pro product.

Locked FSMs

FSMs are locked in an illegal state.

Solution: If you have uninitialized FSMs, turn off the FSM compiler throughout the synthesis flow.

FPGA and Identify Platform-Specific Known Problems and Solutions

The following platform-specific problems apply to supported features in the Synplify Pro and Identify tools.

False Flagging of Product Executables as Malware

On Microsoft Windows, some endpoint protection systems could flag executables as similar to malware threats. These are false positives, as Synopsys thoroughly scans all released files.

Solution: If your endpoint system blocks a Synopsys file, white-list it so that it is not flagged. Also, open a CASE so that Synopsys can investigate.

Identify Tool Known Problems and Solutions

The following problems are specific to the Identify instrumentor and Identify debugger tools.

Eligible Signals Can no Longer be Marked for Debug

After opening an instrumentor view and if you have edited signals for debug using the Instrumentations Select field from the GUI for an implementation, eligible signals can no longer be edited from the source code view (icons disappear and signal names change from blue to black).

Solution: Use the Search panel or the Instrumentation tab instead. Open a text view using the hot link in the File column of the Search panel or Instrumentation tab and set debug points from that view.

To restore the ability to mark the signals for debug from the main source code view:

- Save your work (File->Save)
- Close the instrumentor view (File->Close)
- Select the implementation where the debug logic points are to be inserted
- Re-open the Instrumentation view

Incremental Debug Points from Previous Release Cannot be Used

Attempting to open an incremental debug specification created from a previous Identify release results in an assertion error.

Solution: The incremental debug points from the previous release cannot be used, and new debug points must be defined using this release.

Unable to Launch the GTKWave Viewer from the Identify Debugger

Occasionally when launching the GTKWave viewer from Linux, the viewer fails to open with the following message:

ERROR: couldn't execute "installPath/bin/gtkwave/gtkwave": no such file or directory

Solution: Restart both the Synplify tool and the debugger. This problem is scheduled to be addressed in a future release.

Identify Instrumentor Can Become Unresponsive While Using Multiple Implementations

When using multiple implementations, selecting a different debug point from the user interface of the Identify Instrumentor view can cause the tool to become unresponsive.

Solution: Select the desired implementation from the project view in the synthesis tool, then invoke the Identify Instrumentor rather than attempting to select a different debug point directly from the user interface.

Issue Running Identify Instrumentor and Identify Debugger on Different Platforms

When using real-time debugging with the Identify Instrumentor running on a Linux platform and the Identify Debugger running on a Windows platform, an error is reported when scanning the logic analyzer stating that the remote copy (RCP) could not be executed.

Solution: Run the Identify Debugger from the Linux platform.

Pod Assignments not Displayed After Execution of the Logic Analyzer Command

When using real-time debugging, the iice assignments report command fails to display any pod assignments after successful execution of the assignpod and submit options of the logicanalyzer command.

Solution: This problem is scheduled to be addressed in a future release.

Context-Sensitive Help May not Display Correct Help Page on Linux

When using context-sensitive help (F1) for the Identify tool on Linux, help does not open to the expected page.

Solution: Use the table of contents, global index, or the online help search mechanism to access the correct help page.

Limitations

The current limitations in the tool are divided into the following categories:

- FPGA Synthesis Limitations, on page 8
- Identify Tool Limitations, on page 9

FPGA Synthesis Limitations

The following limitations apply to supported features in the Synplify Pro product.

Page Could Not Be Found Message when Invoking Online Help

When online help is first invoked, it creates a cached version of the compiled help file in a local hierarchy to allow you to save preferences, bookmarks, and full-text search information. This cached version records the path to the installed version. If the same product version is subsequently re-installed in a new directory, invoking online help displays a message, "*The page could not be found*," because the cached version does not recognize the path to the re-installed product.

Solution: Go to the platform-specific directory with the cached help files:

Windows

C:\Users\username\AppData\Local\assistant\Synopsys\Synplify\

Linux

~/.local/share/data/assistant/Synopsys/Synplify/

- Delete any "online*" directories from the cache directory.
- Restart help. This creates a new cache, and correctly displays the online help.

Adobe Reader Error About Opening PDF Files (Linux)

Random links in the document PDFs on the Linux platform do not work. Adobe Reader generates an error message about not being able to find the appropriate PDF file. This does not happen on Windows platforms.

Solution: This is a problem with Adobe Reader on Linux. Work around it by first opening all the PDFs, and then trying the link again.

Online Search Does Not Handle Hyphens as Expected

If the search term includes a hyphen (for example, byte-enable), search in online help does not produce the search hits you expect, because it searches for byte and enable. This limitation does not affect underscores.

It is also limited to online help search and does not affect search in PDF documents.

Solution: Here are some workarounds:

- Basic Search: Use the \ character before the hyphen to escape the hyphen
- Try the index
- Basic Search: Try using the * wildcard
- Basic Search, and Advanced Search with exact term: Try the term with a space in place of the hyphen

GUI Processing Can Fail on Windows 7 for the Synthesis Tool

The synthesis tool GUI might intermittently stop responding on Windows 7.

Solution: To resolve this issue, apply the hotfix from Microsoft by going to suppport.microsoft.com/kb/2718841/.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis GUI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project GUI.

Identify Tool Limitations

The following limitations are specific to the Identify instrumentor and Identify debugger tools.

Verilog/SystemVerilog Limitations When Importing Signals from Verdi

The following Verilog/SystemVerilog language limitations are present when importing signals directly from the Verdi® platform:

- Enums with syn_enum_encoding attribute are not supported for instrumentation and, if present, can impact data expansion.
- Conditional expression settings for unions are either in the form of a serialized bit vector or hex/integer with the bit width representing the maximum available bit width among all union members. Expressions for unions are planned to be enhanced in a future release to allow expressions to target individual union members.
- Generate statements are not supported.

VHDL Limitations When Importing Signals from Verdi

The following VHDL language limitations are present when importing signals directly from the Verdi platform:

- Boolean vector representation in the Identify-generated FSDB is different from the VCS generated FSDB, but does not have any known impact during the data expansion.
- Record elements are represented in reverse order in the Identify-generated FSDB. This
 reversal does not have any known impact during data expansion.
- Generate statements are not supported.

GUI Processing Can Fail on Windows 7 for the Synthesis Tool

The synthesis tool GUI might intermittently stop responding on Windows 7.

Solution: To resolve this issue, apply the hotfix from Microsoft by going to suppport.microsoft.com/kb/2718841/.



Synopsys, Inc. 690 East Middlefield Road Mountain View, CA 94043 USA

Copyright 2018 Synopsys, Inc. All rights reserved. Specifications subject to change without notice. Synopsys, Synplify, Synplify Pro, Certify, Identify, HAPS, VCS, and SolvNet are registered trademarks of Synopsys, Inc. Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at:

http://www.synopsys.com/Company/Pages/Trademarks.aspx

All other product or company names may be trademarks of their respective owners.