Microsemi Corporation: PCN18011

August 21, 2018

Product/Process Change Notification No: PCN18011

Change Classification: Minor

Subject
RTG4 LSRAM Read-Before-Write Mode Data Errors

Description of Change
Using the LSRAM RAM1K18 with WMODE set to “10” for Read-Before-Write mode can result in data corruption of the LSRAM word being addressed. This is observable as an incorrect data bit(s) when reading back previously written data. If ECC is enabled when the issue occurs, the ECC error flag(s) will assert. The error is due to an internal timing marginality in the LSRAM block when in Read-Before-Write mode, and thus it might be observed sporadically and inconsistently.

This issue cannot be screened out during the manufacturing test flow. Therefore, Microsemi will defeature the Read-Before-Write mode of the dual-port RAM1K18 macro. The Libero SoC v11.9 development software, due to be released in August 2018, will not support Read-Before-Write mode for the RAM1K18 dual-port RAM macro. Upon opening an existing design, Libero v11.9 will check and report any instances of RAM1K18 using Read-Before-Write mode. The user will not be allowed to pass the compile step in the design flow if there are RAM1K18 macros using the Read-Before-Write mode. The RTG4 datasheet will be updated to remove timing data for RAM1K18 in Read-Before-Write mode. Instructions on how to use RAM1K18 in Read-Before-Write mode will be deleted from the RTG4 Fabric Users Guide, and the Macro Library Guide will be updated to remove references to Read-Before-Write mode. The RTG4 Errata will also be updated to reflect this issue. Lastly, Microsemi will request an update to Synplify Pro synthesis software such that it no longer infers the Read-Before-Write mode of the RAM1K18 macro. The Synplify release bundled with Libero v11.9 will not contain this update.

Application Impact
RTG4 Dual Port LSRAM will no longer have any native support for simultaneous read and write operations at the same address on the same port. The remaining write mode capability is the “Simple Write” mode (WMODE = “00”), which has no built-in collision prevention or detection. Designs that attempt to simultaneously read and write to the same address should be modified to ensure that no simultaneous read and write operations exist on RTG4 LSRAM, either by instantiation or inference. For a given clock cycle and LSRAM address, the RAM port should either perform a write or a read operation, but not both.

Action Required
Designers should recode their design to use Simple Write mode for RTG4 dual-port LSRAMs and either prevent simultaneous reads and writes to the same address for dual-port LSRAMs or add user logic to detect and avoid this scenario. Updating to the Simple Write mode may be achieved in any of the following ways:

Using the RTG4 Dual-Port LSRAM Configurator
Open the RTG4 Dual-Port LSRAM Configurator and note that the DOUT on Write setting is now grayed-out and locked to select the “Previous DOUT” setting in the configurator dialog box. Regenerate all dual-port LSRAM components to update the WMODE setting and ensure that the design will not simultaneously issue a read and write to the same address of the LSRAM.

Manual instantiation of the RAM1K18 macro
Set WMODE = 00 to select simple write operation and ensure that the design will not simultaneously issue a read and write to the same address of the LSRAM.

Inferencing using synthesis

The following two examples illustrate coding styles to infer dual-port memory structures using RAM1K18 blocks, without invoking Read-Before-Write operations. The first example shows direct reading of the memory contents, and the second example shows pipelined reading of the memory contents. The key difference in this coding style is that for a given clock cycle and address, the code either performs a write (if write-enable is asserted) or performs a read otherwise. There is no scenario where a write and a read occur on the same clock cycle.

```
module truedpramclk2( clka, clkb, wea, addra, dataina, qa, web, addrb, datainb, qb );
parameter addr_width = 10;
parameter data_width = 36;
input clka, clkb, wea, web;
input [data_width-1 : 0] dataina, datainb;
input [addr_width-1 : 0] addra, addrb;
output reg [data_width-1 : 0] qa, qb;

  reg [data_width-1 : 0] mem [(2**addr_width)-1 : 0];

  always @( posedge clka )
  begin
    if ( wea )
      mem[addra] <= dataina;
    else
      qa <= mem[addra];
  end

  always @( posedge clkb )
  begin
    if ( web )
      mem[addrb] <= datainb;
    else
      qb <= mem[addrb];
  end

endmodule
```

```
module truedpramclk2pipe( clka, clkb, wea, addra, dataina, qa, web, addrb, datainb, qb );
parameter addr_width = 10;
parameter data_width = 36;
input clka, clkb, wea, web;
input [data_width-1 : 0] dataina, datainb;
input [addr_width-1 : 0] addra, addrb;
output reg [data_width-1 : 0] qa, qb;

  reg [data_width-1 : 0] mem [(2**addr_width)-1 : 0];
  reg [data_width-1 : 0] qa_pipe, qb_pipe;

  always @( posedge clka )
  begin
    if ( wea )
      mem[addra] <= dataina;
    else
      qa_pipe <= mem[addra];
    qa <= qa_pipe;
  end

  always @( posedge clkb )
  begin
    if ( web )
      mem[addrb] <= datainb;
    else
      qb_pipe <= mem[addrb];
    qb <= qb_pipe;
  end

endmodule
```

Products Affected by this Change

See Appendix A.

Contact Information

If you have any questions, please contact Microsemi's SoC Technical Support at soc_tech@microsemi.com.

Regards,

Microsemi Corporation

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Microsemi Sales Office, the factory contact shown above, or your local distributor.

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Appendix A

Microsemi Part Number	DLA SMD Number
RT4G150-CB1657PROTO	
RT4G150-CG1657B	5962-1620801QXF
RT4G150-CG1657E	5962-1620805QXF
RT4G150-CG1657EV	
RT4G150-CG1657V	5962-1620809VXF
RT4G150-CG1657PROTO	
RT4G150-CQ352B	
RT4G150-CQ352E	
RT4G150-CQ352EV	
RT4G150-CQ352PROTO	
RT4G150-LG1657B	5962-1620803QZC
RT4G150-LG1657E	5962-1620807QZC
RT4G150-LG1657EV	
RT4G150-LG1657V	5962-1620811VZC
RT4G150-LG1657PROTO	
RT4G150-1CB1657PROTO	
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-1CG1657EV	
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-1CG1657PROTO	
RT4G150-1CQ352B	
RT4G150-1CQ352E	
RT4G150-1CQ352EV	
RT4G150-1CQ352PROTO	
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-1LG1657EV	
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-1LG1657PROTO	

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