AC476
Application Note
High-Level Design Migration Overview from Kintex to PolarFire

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 2.0

The following are the changes made in this document.

- Updated Table 8, page 11, Table 10, page 13, Table 11, page 13, and Table 14, page 15.
- Added Reliability, page 16.

1.2 Revision 1.0

The first publication of this document.

2 Introduction

PolarFire® FPGAs are the fifth-generation family of 28nm non-volatile flash-based SoC FPGA devices from Microchip. The PolarFire family offers multiple devices that vary in the number of logic elements (LE), I/Os, memories, and packages thus, offering device variants for a variety of applications.

PolarFire devices consume drastically lower total power than competitive FPGAs.The following Flash-based characteristics of PolarFire devices attribute to this low power consumption feature:

- Inherent low leakage current
- Zero in-rush current
- Zero configuration current

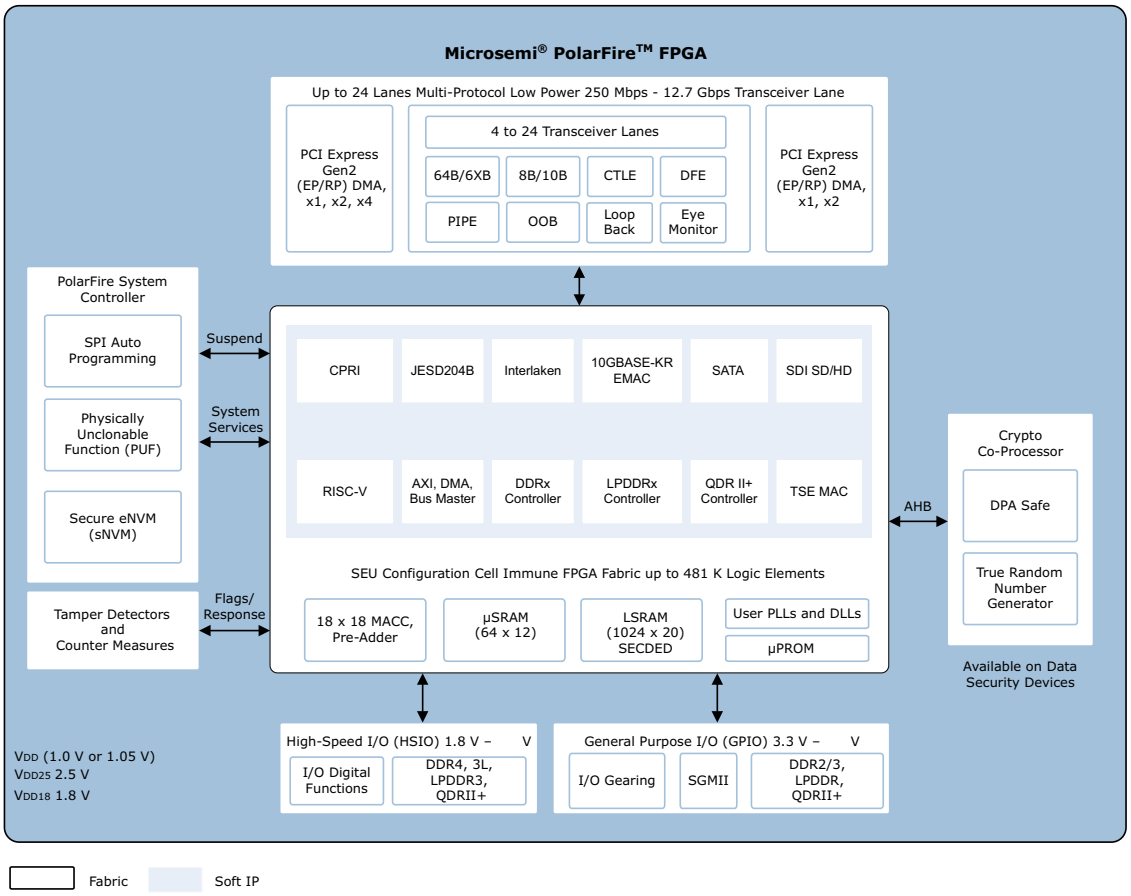
PolarFire devices are live at power-up because they are non-volatile and hence, do not need external configuration devices for re-programmability. Hence, PolarFire devices eliminate hundreds of milliwatts at device startup and configuration, and thereby, eliminate the need for external devices for mitigation.

This document is a high-level feature comparison of Microchip PolarFire FPGA and Xilinx Kintex-7 FPGA, along with Libero SoC and Vivado tools respectively. Some utilization and resource count information is specific to PolarFire 300T and Kintex-7 325T.

2.1 Device Architecture

Figure 1 shows the high-level device architecture of the PolarFire Device.

Figure 1 • **Device Architecture**



Note: For synchronous reset, PolarFire has higher priority for enable pin than sync reset pin.

2.2 Device Resource Comparison

This section lists the functional resources of PolarFire devices and Kintex 7 devices. Table 1 shows PolarFire MPF100T, MPF200T, and MPF300T devices which are similar to XC7K70T, XC7K160T, and XC7K325T devices. Table 2 shows PolarFire MPF300T, and MP5200T devices which are similar to XC7K355T, XC7K410T, XC7K420T, and XC7K480T devices.

This information is useful in changing to the best matching PolarFire device.

Table 1 • **Device Resource Comparison (up to 300T devices)**

Device Name	XC7K70T	MPF100T	XC7K160T	MPF200T	XC7K325T	MPF300T
LUT6 Count	410,00	-	101,400	-	203,800	-
Equivalent: LUT4+FF	59,450	109,000	147,030	192,408	295,510	299,544
Flip-Flops	82,000	109,000	202,800	192,408	407,600	299,544
Math Block	240	336	600	588	840	924
Max 18X18 Multiplier	240	336	600	588	840	924
Total RAM (Kb)	5,698	7,796	13,888	13,643	20,020	21,119
Max SerDes Blocks	8	4	8	16	16	16
Max SerDes Speed (Gbps)	12.5	12.7	12.5	12.7	12.5	12.5
Smallest Package	FBG484	FCSG325	FBG484	FCSG325	FBG676	FCSG536
Size (mm)	23x23	11x11	23x23	11x14.5	27x27	16x16
Pitch (mm)	1	0.5	1	0.5	1	0.5
Max IO Count	300	284	400	368	500	512
3.3V Capable IOs	200	164	250	236	350	236
Temperature Grades	C, I	C, I	C, I	C, I	C, I	C, I
Process Technology	28 nm	28 nm	28 nm	28 nm	28 nm	28 nm
PLLs	6	8	8	8	10	8
PCIe	1 (Gen1 and Gen2, Gen3 soft IP)	2 (Gen1 and Gen2)	1 (Gen1 and Gen2, Gen3 soft IP)	2 (Gen1 and Gen2)	1 (Gen1 and Gen 2, Gen3 soft IP)	2 (Gen1 and Gen2)
Core Voltage(V)	1.0V, 0.95V, 0.9V	1.05V, 1.0V	1.0V, 0.95V, 0.9V	1.05V, 1.0 V	1.0V, 0.95V, 0.9V	1.05V, 1V

Table 2 • **Device Resource Comparison (300T to 500T devices)**

Device Name	MPF300T	XC7K355T	XC7K410T	XC7K420T	XC7K480T	MPF500T
LUT6 Count	-	222600	254200	260600	298600	-
Equivalent: LUT4+FF	299,544	322,770	368,590	377,870	432,970	481,272
Flip-Flops	299,544	4,45,200	5,08,400	5,21,200	5,97,200	481,272
Math Block	924	1440	1540	1680	1920	1480
Max 18X18 Multiplier	924	1440	1540	1680	1920	1480
Total RAM (Kb)	21,119	30,828	34,283	35,998	41,168	33,730
Max SerDes Blocks	16	24	16	32	32	24
Max SerDes Speed (Gbps)	12.5	12.5	12.5	12.5	12.5	12.5

Table 2 • **Device Resource Comparison (300T to 500T devices)** ***(continued)***

Device Name	MPF300T	XC7K355T	XC7K410T	XC7K420T	XC7K480T	MPF500T
Smallest Package	FCSG536	FFG901	FBG676	FFG901	FFG901	FCG784
Size (mm)	16x16	31x31	27x27	31x31	31x31	29x29
Pitch (mm)	0.5	1	1	1	1	1
Max IO Count	512	300	500	400	400	584
3.3V Capable IOs	236	300	350	400	400	260
Temperature Grades	C, I	C, I	C, I	C, I	C, I	C, I
Process Technology	28 nm	28 nm	28 nm	28 nm	28 nm	28 nm
PLLs	8	6	10	8	8	8
PCIe	2 (Gen1 and Gen2)	1 (Gen1 and Gen2, Gen3 soft IP)	1 (Gen1 and Gen2, Gen3 soft IP)	1 (Gen1 and Gen2, Gen3 soft IP)	1 (Gen1 and Gen2, Gen3 soft IP)	2 (Gen1 and Gen2)
Core Voltage(V)	1.05V, 1V	1.0V, 0.95V, 0.9V	1.0V, 0.95V, 0.9V	1.0V, 0.95V, 0.9V	1.0V, 0.95V, 0.9V	1.05V, 1V

3 Libero SoC Overview

Libero® SoC Design Suite is the development tool for designing with Microchip's PolarFire FPGA Family. The suite integrates industry standard Synopsys Synplify Pro ME® synthesis and Mentor Graphics ModelSim ME® simulation with best-in-class Constraints Management, Debug Tool capabilities, and Secure Production Programming support.

3.1 License Types

The following table enlists the types of licenses available for Libero SoC.

Table 3 • **Libero SoC License Types**

License Type	Description
Evaluation	Free license to enable design evaluation. Supports mixed language simulation and all the FPGA/SoC families. Programming and debug functions are not included. Available with Libero SoC.
Silver	Free license supporting Libero SoC with programming and debug support.
Gold	Paid license supporting all the Libero versions with limited FPGA and SoC families. It supports mixed language simulation for Libero SoC.
Platinum	Paid license supporting all the FPGA and SoC families and features
Standalone	Paid license supporting all the FPGA and SoC families with Microchip tools. It does not support third party tools like Synopsys Synplify Pro, Identify and Mentor ModelSim tools.
Platinum Archival	Paid license enabling you to archive your design for a longer period. Supports all the features of the Platinum license for 20 years. It is valid for the latest version (at the time of purchase) and earlier Libero SoC and Libero IDE releases.
Standalone Archival	Paid license enabling you to archive your design for a longer period. Provides permanent support for all the features of Standalone license for the latest version (at the time of purchase) and earlier Libero SoC and Libero IDE releases.
Gold Archival	Paid license enabling you to archive your design for a longer period. Supports all the features of Gold license for 20 years. It is valid for the latest version (at the time of purchase) and earlier Libero SoC and Libero IDE releases.

3.2 Installation

1. Download and install Libero SoC on the host PC from the following location: *https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads*
2. Download and install SoftConsole (standalone) on the host PC from the following location: *https://www.microsemi.com/product-directory/design-tools/4879-softconsole#downloads*
3. Download and install Programming and Debug Tools (standalone) on the host PC from the following location: *https://www.microsemi.com/product-directory/programming/4977-flashpro#software*

Note: A minimum of 3.5GB disk space on a system with at least 32GB RAM is recommended for Libero SoC.

3.3 OS Support

Current information about OS support is available Online on Microchip’s Libero SoC Device Support webpage.

4 Tool Flow

This chapter describes the following sections.

4.1 Overview

Libero SoC manages the design flow for the user similar to Vivado Project mode flow.

Table 4 • **Design Flow**

Feature	Libero PolarFire	Vivado (Non-Project mode)	Vivado project mode
Manage HDL	`import_files -hdl_source {top.v}`	`read_verilog` `read_vhdl`	`add_files` `import_files`
Manage Constraints	`import_files -sdc {user.sdc}`	`read_xdc`	-
Synthesize	`run_tool -name {SYNTHESIZE}`	`synth_design`	`launch_run synth_1`
Optimize Design	-	`opt_design`	-
Compile	Compile is integrated with Synthesis.	-	-
Place and Route	`run_tool -name {PLACEROUTE}`	`place_design` `route_design`	`launch_run impl_1`
Report Timing	`run_tool -name {VERIFYTIMING}`	`report_timing`	`report_timing_summary`
Report Power	`run_tool -name {VERIFYPOWER}`	`report_power`	-
Generate Bitstream	`run_tool -name { GENERATEPROGRAMMINGFILE }`	`write_bitstream`	`write_bitstream`
Program Device	`run_tool -name {PROGRAMDEVICE}`	`program_hw_device`	`program_hw_device`

Early stage power estimation for PolarFire devices can be done using the PolarFire Power Estimator. The PolarFire Power Estimator can be downloaded from the Microchip website (see References, page 18). Xilinx offers XPE for early stage power estimation.

Microchip's Power Estimator tool enables users to estimate the power consumed by PolarFire devices with respect to the selected resources. A more real-time power consumption can also be estimated using Libero SoC->SmartPower after the FPGA design is ready. The Power Estimator link is available in References, page 18.

Note: A set of Perl scripts have been developed to expedite migration from Vivado to Libero. Download the scripts from https://download-soc.microsemi.com/FPGA/Apps/outgoing/Migration_Perl_Scripts.7z. These scripts are for reference.

4.2 Synthesis and Simulation Tools

Libero SoC integrates Synopsys Synplify Pro ME, ModelSim Pro ME software to perform synthesis and simulation.

Both tools are installed by default when installing Libero SoC. They can be launched directly from the Libero project manager.

The Libero Silver license supports only ModelSim ME, while Gold and Platinum licenses support ModelSim Pro. Customers have to select ModelSim Pro in Tool Profiles to access the latest release.

ModelSim Pro ME provides enhanced simulation capabilities. With this edition of the simulator, mixed-language simulation for Verilog, System Verilog, and VHDL is possible.

For more information on Synplify Pro ME and ModelSim ME, see *https://www.microsemi.com/product-directory/fpga-soc/1637-design-resources.*

4.3 Debug Tools

SmartDebug in PolarFire offers state-of-the-art non-intrusive (without using an ILA) debug of FPGA fabric and SERDES. SmartDebug uses probe points built into the FPGA, which eliminates recompile time. Smart Debug enables verification and troubleshooting at the hardware level. It does not require any Fabric logic and changes to design flow.

SmartDebug offers features such as Live Probe, Active Probe, Memory Debug, SERDES Debug, and Probe Insertion. For more information about how to use SmartDebug, see UG0743: Polar Fire FPGA Debugging User Guide.

PolarFire designs can also be debugged using Synopsys Identify.

Table 5 • **Debugging**

Feature	PolarFire	Kintex-7	Comments
Non-intrusive Debug	Yes	No	SmartDebug like feature is only available in PolarFire.
Debug using Integrated Logic Analyzer (ILA)	Yes, using Synopsys Identify	Yes, using Vivado LabTools	
SERDES debug	Yes, using SmartBERT	Yes, using IBERT	
Transceiver Eye Diagram	Yes	Yes	
GUI and Tcl support	Yes, both modes supported.	Yes, both modes supported.	

SmartBERT can be used to run diagnostic tests on the transceiver lanes to determine the Bit Error Rate (BER) using the built-in generator-checker or using the SmartBERT IP. The built-in generator supports PRBS7, PRBS9, PRBS15, PRBS23, and PRBS31 patterns, while SmartBERT IP supports additional protocol specific generator-checkers.

4.4 Design Initialization Methodologies

PolarFire provides a new flow for initializing the RAMs, Transceiver/PCIe. During design initialization, user design blocks such as LSRAM, µSRAM, transceiver configurations, and PCIe can be optionally initialized using data stored in a non-volatile storage memory. The initialization data can be stored in µPROM, sNVM, or an external SPI flash. The storage location of the initialization data is selected during the Libero design flow.

The user can monitor design initialization using the PolarFire Initialization Monitor macro available in the Libero catalog.

For details on power-up and reset sequencing, see *UG0725: PolarFire FPGA Device Power-Up and Resets User Guide*.

5 Device Features

This chapter describes the following sections:

5.1 Clocking Resources

PolarFire clocking resources are classified into three categories, which are:

- Clock routing
- On-chip oscillators
- Clock conditioning circuits (CCC) such as PLL and DLL

Clock routing resources are of five types

- Global clock network: To distribute high fanout nets such as clocks and resets.
- Regional clock network: To distribute clocks from I/Os and transceivers to fabric through Regional Clock Buffers (RCB).
- High-Speed I/O Clock network: To implement high speed source-synchronous interfaces.
- Preferred Clock Inputs: I/Os that can directly drive Global Buffers (GB), or CCC.
- Preferred Clock Outputs: I/Os that can be directly driven by CCC.

In addition, PolarFire provides 24 programmable clock dividers at the center of the edge of four sides of the device and 12 no-glitch MUXes for glitch free dynamic clock switching between two independent clocks.

PolarFire devices offer 2 On-chip oscillators (2 MHz and 160 MHz) to generate free running clocks.

Clock Conditioning Circuits are located at the 4 corners of the FPGA and offer functions such as frequency synthesis (generate higher or lower frequency compared to input clock), Spread Spectrum Clocking, jitter attenuation, clock delay and phase adjustment and duty cycle correction.

Table 6 • **Clocking Resources Comparison**

Feature	PolarFire	Kintex-7	Comments
Global Clocks	Yes. GB located at center of the die.	Yes. BUFG located along the center clocking backbone.	NA
Global Clock routing	1 horizontal and 2 vertical stripes	1 vertical backbone	NA
Regional Clocks	Yes. RGB for each half-row, driven by GB, I/O, or transceiver.	Yes. BUFH for each row.	NA

Table 6 • **Clocking Resources Comparison *(continued)***

Feature	PolarFire	Kintex-7	Comments
HS IO Clock	Yes. Integrated in IO banks, driven by CCC or IOs	Yes. through BUFR and BUFIO	For more information about HS IO, see *UG0686: PolarFire FPGA User I/O User Guide*.
Preferred Clock Inputs	Yes. Can drive GB, RGB, CCC.	Yes. Can drive BUFR, BUFH, BUFIO, BUFG, MMCM.	NA
Preferred Clock Outputs	Yes. Can be driven by CCC only.	Yes. Can be driven by MMCM only.	NA
On-chip Oscillator	Yes. 2 MHz and 160 MHz.	No	NA
Clock Gating	Yes	Yes	NA
Interface Clock Block	Yes. Independent block to modify and route clock nets.	No	NA
Multi regional Clock Buffers	No	Yes. Through BUFMR.	NA
PLL, DLL	Yes. Implemented as FCCC.	Yes. Implemented as MMCM.	NA
Number of Clock Outputs	4 to global and local routing	7 outputs and 4 inverted outputs.	NA
Input Jitter Filter	Yes	Yes	NA
Spread Spectrum Clocking	Yes	Yes	NA
Output Clock Delay	Yes	Yes	NA
Output Clock Phase Adjustment	Yes	Yes	NA
Dynamic Reconfiguration for PLL/DLL	Yes	Yes	NA
PLL/DLL Clock Switching	No	Yes	Both reference clock inputs to FCCC must be same frequency.
PLL/DLL Clock Fail-Safe	Yes	Yes	

5.2 On-chip Non-Volatile Memories

The following table compares the features between Microchip and Xlinx based on On-chip Non-Volatile Memories.

Table 7 • **On-chip Non-Volatile Memories**

Microchip	Xilinx	Features
sNVM - Secure Non-Volatile Memory	NA	Content can be used to initialize LSRAMs and µSRAM. It is also used to store secure data.
µPROM	NA	513 Kb of non-volatile, read-only memory.
NA	eFUSE	Non-reprogrammable FUSE bits.

The following table compares the features between PolarFire and Kintex based on DSPs.

Table 8 • **DSPs**

Feature	PolarFire	Kintex-7	Comments
Dot Product Mode (A.B + C.D)	Yes	No. Need to cascade two DSP slices to achieve this functionality.	DOTP enables 9-bit complex number multiplication for signal processing applications
Single-Instruction, Multiple-Data (SIMD) mode	Yes. Supports dual-independent multipliers functionality.	It supports only add/subtract/accumulate.	No independent multiplier functionality support in Kintex-7
Extended multiplication support	No	Yes	NA
Optional ALU	Not available	Optional ALU can perform 10 operations.	NA
Pattern Detector	Not available	— Connected to output of logic unit. — Support for convergent rounding, overflow/underflow, block floating point, and counter auto-reset	NA
Storage of Coefficients	Coefficients can be stored in 16x18 coefficient ROM	RAM resources are used	Higher logic usage for Kintex-7
Pre-adder	18-bit	25-bit	NA
Bit width	18x18	25x18	NA

5.3 Fabric Memories

The PolarFire FPGAs provide two volatile memories - LSRAM and µSRAM. In comparison, the Kintex-7 FPGAs contain distributed RAM (look-up tables configured as memory blocks) and block RAM hard macros.

Data is written synchronously into the RAM for both types. The primary difference between LSRAM and µSRAM is in the way data is read from the RAM.

- µSRAM- Must be used for RAM descriptions with asynchronous read. Distributed RAM provides the same functionality.
- LSRAM- Generally used for RAM descriptions with synchronous read. Dedicated block RAM provides the same functionality.

5.3.1 RAM Similarities

- Both LSRAM and Block RAMs are Synchronous and True Dual Port.
- Byte-write feature available in both RAMs but with different write configurations.
- Pipeline registers are available for the READ port with optional reset control.
- Supports True Dual Port and 2 Port modes of operation.
- Three types of write operations: Simple Write, Feed-Through Write, and Read-Before Write.
- Supports ECC mode.

5.3.2 Fabric Memory Initialization

Fabric memories (LSRAM and uSRAM) can be initialized using any of the following methods:

- Using Configurator: Microchip IP Catalog offers various RAM configurators and interfaces (AXI, AHB). The memory generated using the configurators can be initialized using an INTEL-HEX file.

- Using RTL initialization: `$readmemb` and `$readmemh` can be used to load initial values into the RAM when the RAM is inferred using RTL.

5.4 External Memory Interface

Libero has separate configurators for DDR3 and QDR, whereas Vivado has a single MIG (Memory Interface Generator), which is used to configure different types of supported memory configurations.

PolarFire, as well as, Kintex supports the AXI4 interface for DDR3. The QDR has a native interface for PolarFire and Kintex.

GUI configurator can be used to select the data widths, clock frequency, memory timings, and so on.

For PolarFire, DDR IOs must be assigned using the IO Editor in Libero. In Kintex-7, DDR IO's can be assigned directly in the memory configurator in Vivado.

Table 9 • **External Memory Interface**

	PolarFire	Kintex
DDR	Supported Memories: DDR4, DDR3, DDR3L, LPDDR3, LPDDR2	Supported Memories: DDR3, DDR3L, DDR2, LPDDR2,RLDRAM II, RLDRAM 3
	Supports 16, 32, 40, 64, and 72-bit DDR SDRAM data buses	Configurable data bus widths (multiples of 8, up to 72 bits)
	Supports a maximum of 16 memory banks	Supports a maximum of 8 memory banks
	Supports on-die termination (ODT) including dynamic ODT	On-die termination (ODT) support
	Supports ECC for 40 and 72 bit	Supports ECC for 72 bit
	Performs calibration to centre align capture clocks with read data	Performs calibration to centre align capture clocks with read data
	Up to 1333 Mbps (666 MHz DDR) data rates.	Upto 1866 Mbps data rate supported
	4:1 memory to FPGA logic interface clock ratio	4:1 memory to FPGA logic interface clock ratio
	Write levelling support for DDR3	Write levelling support for DDR3
	Burst Length should be 8	Burst Length should be 8
QDR	Supports QDR II+ and QDR II+ Xtreme Interface	QDR II+ SRAM device support
	Max supported frequency: 633 MHz clock	Max supported frequency: 550 MHz
	Configurable QDR data width (8, 9, 18, 36 bits)	x18 and x36 memory width support
	2, 4-word burst support	Burst of 2 and burst of 4 support (configurable)

5.5 IO Overview

This section provides an overview of the IOs in PolarFire and Kintex-7.devices.

Table 10 • **IO Features**

Feature	PolarFire	Kintex-7
Voltage range 1.1V - 1.8V	Yes. Using High Speed IO (HSIO)	Yes. Using High Performance IO (HPIO)
Voltage range 1.1V - 3.3V	Yes. Using General Purpose IO (GPIO)	Yes. Using High Range IO (HRIO)
Open drain output	Yes	No
Schmitt trigger input	Yes	No
Cold sparing	Yes	No
Hot swap	Yes	No
LVDS max speed	1.6 Gbps	1.6 Gbps
IO Gearing	Yes	Yes
Programmable IO delay	Yes, with 128-tap delay	Yes, with 32-tap delay
On-die termination	Yes	Yes
Programmable weak pull-up/down	Programmable through Libero SoC	Programmable through Vivado
Programmable slew rate	Yes	Yes
Programmable output drive strength	Yes	Yes

5.6 IO Gearing

PolarFire supports I/O gearing logic that is used to interface between the high-speed I/O buffers and lower speed FPGA fabric. Supported features include:

- Up to 10:1 input deserialization and up to 10:1 output serialization.
- Support for SDR and DDR interfaces.
- Receive slip control to facilitate word alignment.
- Fast low skew lane clocks per twelve IOs.

Each I/O gearing block consists of:

- Programmable input, output and enable delay chain
- Input, output and enable registers
- Gearbox (serial to parallel conversion and vice versa)
- Data eye monitor
- FIFO

The equivalent feature in Kintex-7 is ISERDES and OSERDES.

5.7 Security Features

The following table lists the security features supported by PolarFire and Kintex-7 devices.

Table 11 • **Comparison of Security Features**

PolarFire	Kintex-7
DPA bit stream protection.	Not available
SRAM Physically Unclonable Function (PUF).	Not available

Table 11 • **Comparison of Security Features *(continued)***

PolarFire	Kintex-7
Secure Non Volatile Memory (sNVM) is used to store the keys. All PolarFire devices have 56Kbytes of sNVM.	BBRAM/eFUSE is used for keys storage BBRAM is volatile and reprogrammable but requires an external battery source. eFUSE is permanent thus making it less secure
True random number generator is used to generate keys.	Pseudo random number generator is used to generate keys.
Integrated Athena Crypto co-processor for security encryption and decryption.	No Crypto co-processor available.
Tamper detection is a hard block. It monitors Voltage, Temperature and also detects clock and voltage glitches. After processing a detected event, user can disable the IOs, Security lock down, reset, and zeroize.	Tamper detection is achieved using a soft Security Monitor IP core.
Supports AES128/192/256 encryption and decryption.	Supports only AES256.
Keys hashed and enciphered by SRAM PUF and then reconstructed during use.	Keys encrypted and stored either in BBRAM or eFUSE. Hashed message authentication.
Supply Chain Assurance: Through a 768-byte digitally signed x.509 FPGA certificate embedded in every FPGA Supply Chain Management: Through Hardware Security Modules (HSMs) during wafer test and packaging	No No
HMAC algorithm with SHA-256 Authentication?	HMAC algorithm with SHA-256 Authentication?
Rivest-Shamir Adleman (RSA)	No
Digital Signature Algorithm (DSA)	TBD
Elliptic Curve Cryptography (ECC)	TBD

5.8 PolarFire System Services

System services are System Controller actions initiated from FPGA design using CoreSysServices_PF IP core.

System Controller hard block provides various system services.

Table 12 • **System Services**

Service Category	Services
Device and Data	Read Device Serial Number Read Device UserCode Read Device Design-Info
Design and Data Security	Read Device Certificate Read Digest Query Security

For more information about different types of supported System Services, see *UG0753: PolarFire FPGA Security User Guide.*

5.9 Transceiver Supported Protocols

The following table lists the transceiver protocol supported by PolarFire and Kintex-7 devices.

Table 13 • **Transceiver Supported Protocols**

Protocol	PolarFire	Kintex-7
PCIe (Gen1/Gen2)	Yes	Yes
PCIe (Gen3)	No	Yes (Soft Core)
XAUI	Yes	Yes
Interlaken	Yes	Yes
10BASE-R	Yes	Yes
10BASE-KR	Yes	Yes
Fibre Channel	Yes	Yes
JESD204B	Yes	Yes
RXAUI	Yes	Yes
QSGMII	Yes	Yes
CPRI	Yes	Yes
SATA	Yes	Yes
SDI-SD	Yes	Yes
SDI-HD	Yes	Yes
SDI-3GHD	Yes	Yes
SGMII	Yes	Yes
1000BASE-X	Yes	Yes
Custom Serial Protocol	LiteFast	Aurora
SRIO	Yes (Partner)	Yes
Optical channel Transport Unit support	OTU1 OTU2 and OTU2e	OTU-1, OTU-2, OTU-3, OTU-4

5.10 Transceiver Features

The following table lists the transceiver features supported by PolarFire and Kintex-7 devices.

Table 14 • **Transceiver Features**

PolarFire	Kintex-7
Supports 8, 10, 16, 20, 32, 40, 64, and 80 bits	supports 16, 20, 32, 40, 64, or 80 bits
Supports 5-tap DFE	Supports 5-tap DFE
Out-of-band (OOB), signaling capability for SAS and SATA	Out-of-band (OOB) signaling including COM signal support for SATA
8b10b encoding/decoding. 64b/66b and 64/67b support	8B/10B encoding and decoding. 64B/66B and 64B/67B support
PIPE interface support	PIPE interface support
Spread spectrum clocking support	Spread spectrum clocking support
Polarity Inversion on received data	Polarity Inversion on received data
Loss of signal	TBD

Table 14 • **Transceiver Features**

PolarFire	Kintex-7
Transceiver QUADs up to 6	Transceiver QUADs up to 8
Transceiver lanes up to 24	Transceiver lanes up to 32
PRBS generator and checker	PRBS generator and checker

5.11 Reliability

Table 15 • **Reliability**

PolarFire	Kintex-7
Zero Resources	Uses SMIP which consumes logic resources.
Built-in ECC memory	Built-in ECC memory
Fabric SEU immune	No
0 FIT/Mb	50 FIT/Mb (alpha Particle), 1.1Fit/Mb (Thermal Neuron)
CRI patented DPA bit stream protection	No
System Controller: For safety critical application, system controller will be in suspend mode. The system controller manages device programming, design security, key-management, and related operations. The system controller has both, a JTAG interface and a SPI interface.	No

5.12 Programming Features

The following table lists the programming features supported by PolarFire and Kintex-7 devices.

Table 16 • **Programming Features**

Features	PolarFire	Kintex-7
JTAG	Yes [FlashPro]	Yes
External microprocessor	Yes [Direct C]	Yes
Master SPI	Yes [Auto Update, IAP]	Yes
Select MAP	No	Yes. Single-device Slave Select MAP, Multiple-device daisy-chain Select MAP bus
SPI slave	Yes [FlashPro], Direct C]	No (Slave Serial only)
Master BPI	No	Yes

5.13 Embedded Solutions

This section describes the IDE and the soft processors available.

5.13.1 SoftConsole

SoftConsole is Microchip's Eclipse based IDE that enables the rapid production of C and C++ executables for RISC-V and Cortex-M1 applications. Libero SoC can export firmware for SoC FPGA designs that can be imported into SoftConsole. SoftConsole includes a fully integrated debugger that offers easy access to memory contents, registers, and single-instruction execution. SoftConsole provides a flexible and easy-to-use graphical user interface for managing your embedded software development projects. You can quickly develop and debug software programs and implement them in Microchip FPGAs.

5.13.1.1 Mi-V

Mi-V is a softcore processor designed to implement the RISC-V instruction set for Microchip FPGAs. Mi-V Soft Cores are freely available through Libero Catalog. It provides an on-chip debug unit with a JTAG interface.

5.13.1.2 Cortex-M1

CoreCortex M1 processor is a general purpose 32-bit microprocessor that offers high performance and small size in FPGAs. CoreCortexM1 processor runs a subset of the Thumb-2 instruction set (ARMv6-M) that includes all base 16-bit Thumb instructions and a few Thumb-2 32-bit instructions (BL, MRS, MSR, ISB, DSB, and DMB). This enables writing a very tight and efficient processor code, which is ideal for the limited memory typically found in deeply-embedded applications.

6 References

6.1 PolarFire

1. Libero SoC
2. Microchip PolarFire Power Estimator
3. DS0141: PolarFire FPGA Datasheet
4. DS0143: PolarFire FPGA MPF300XT Datasheet
5. UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide
6. UG0680: PolarFire FPGA Fabric User Guide
7. UG0684: PolarFire FPGA Clocking Resources User Guide
8. UG0686: PolarFire FPGA User I/O User Guide
9. UG0677: PolarFire FPGA Transceiver User Guide
10. UG0685: PolarFire FPGA PCI Express User Guide
11. UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
12. UG0727: Polar Fire FPGA 10G Ethernet Solutions User Guide
13. UG0676: PolarFire FPGA Memory Controller User Guide
14. UG0748: PolarFire FPGA Low Power User Guide
15. UG0743: Polar Fire FPGA Debugging User Guide
16. UG0714: PolarFire FPGA Programming User Guide
17. UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
18. UG0726: PolarFire FPGA Board Design User Guide
19. UG0753: PolarFire FPGA Security User Guide
20. UG0701: Lite Fast IP User Guide
21. ER0215: PolarFire FPGA MPF300XT Devices Errata
22. ER0207: PolarFire FPGA ES Devices Errata
23. UG0676: PolarFire FPGA Memory Controller User Guide

6.2 Kintex-7

1. DS182: Kintex-7 FPGAs Data Sheet:- (DC and AC Switching Characteristics)
2. DS855: Chip Scope Integrated Bit Error Ratio Test (IBERT) for Kintex-7 GTX (v2.01.a) Data Sheet
3. DS176: Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions v4.1 Data Sheet
4. UG475: 7 Series FPGAs Packaging and Pinout Product Specifications User Guide
5. UG470: 7 Series FPGAs Configuration User Guide
6. UG471: 7 Series FPGAs SelectIO Resources User Guide
7. UG472: 7 Series FPGAs Clocking Resources User Guide
8. UG473: 7 Series FPGAs Memory Resources User Guide
9. UG474: 7 Series FPGAs Configurable Logic Block User Guide
10. UG483: 7 Series FPGAs PCB Design Guide
11. UG479: 7 Series DSP48E1 Slice User Guide
12. UG480: 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide
13. UG476: 7 Series FPGAs GTX/GTH Transceivers User Guide
14. UG1099: Recommended Design Rules and Strategies for BGA Devices User Guide
15. UG116: Device Reliability Report, Second Half 2017
16. UG586: Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions v4.1 User Guide
17. UG769: LogiCORE IP 7 Series FPGAs Transceivers Wizard v2.6 User Guide
18. EN183: Kintex-7 FPGA CES Errata
19. EN190: Kintex-7 FPGA CES9925 Errata
20. EN171: Kintex-7 FPGA XC7K325T CES9937 Errata
21. EN179: Kintex-7 FPGAs XC7K480T CES9937 Errata
22. UG586: Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions v4.1 User Guide