DG0839
Demo Guide
PolarFire FPGA Wireless Radio Digital Front-End Design
## Contents

1 Revision History ................................................................. 1  
1.1 Revision 1.0 ................................................................. 1

2 Wireless Radio Digital Front-End Design .................................. 2  
2.1 Design Requirements ........................................................ 3
2.2 Prerequisites ................................................................. 3
2.3 Demo Design Architecture .................................................. 4  
2.3.1 Subsystem Components ................................................ 4
2.3.2 Clocking Structure ...................................................... 7
2.3.3 Reset Structure .......................................................... 9
2.3.4 Resource Utilization ..................................................... 10
2.3.5 Timing Closure in Libero .............................................. 10

3 Hardware Data Flow ............................................................ 11

4 Setting Up the Demo ............................................................. 12  
4.1 Setting up the Hardware ..................................................... 12
4.2 Programming the PolarFire Device ..................................... 15
4.3 Enabling Jitter Cleaner on CPRI TX PLL ............................... 15

5 Running the Demo ............................................................... 17  
5.1 Configuring and Monitoring the RRH Tester .......................... 17  
5.1.1 Configuring the Tester .................................................. 17
5.1.2 Monitoring the Tester ................................................... 20
5.1.3 Enabling Multicast on CPRI ........................................... 21
5.2 Executing the User Application .......................................... 23
5.3 Monitoring the Performance .............................................. 25

6 Power Measurements .......................................................... 27  
6.1 Conclusion ................................................................. 27
<table>
<thead>
<tr>
<th>Figure Number</th>
<th>Figure Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1</td>
<td>PolarFire Wireless Radio DFE Design Architecture</td>
<td>4</td>
</tr>
<tr>
<td>Figure 2</td>
<td>CPRI Interface</td>
<td>5</td>
</tr>
<tr>
<td>Figure 3</td>
<td>I and Q Patterns</td>
<td>5</td>
</tr>
<tr>
<td>Figure 4</td>
<td>DUC</td>
<td>5</td>
</tr>
<tr>
<td>Figure 5</td>
<td>DDC</td>
<td>6</td>
</tr>
<tr>
<td>Figure 6</td>
<td>JESD204B Interface</td>
<td>6</td>
</tr>
<tr>
<td>Figure 7</td>
<td>Mi-V Processor Subsystem</td>
<td>7</td>
</tr>
<tr>
<td>Figure 8</td>
<td>Clocking Structure</td>
<td>8</td>
</tr>
<tr>
<td>Figure 9</td>
<td>Reset Structure</td>
<td>9</td>
</tr>
<tr>
<td>Figure 10</td>
<td>Data Flow</td>
<td>11</td>
</tr>
<tr>
<td>Figure 11</td>
<td>SMA Connections</td>
<td>13</td>
</tr>
<tr>
<td>Figure 12</td>
<td>Hardware Setup</td>
<td>14</td>
</tr>
<tr>
<td>Figure 13</td>
<td>Device Programmed</td>
<td>15</td>
</tr>
<tr>
<td>Figure 14</td>
<td>Starting SmartDebug</td>
<td>15</td>
</tr>
<tr>
<td>Figure 15</td>
<td>Execute Script</td>
<td>16</td>
</tr>
<tr>
<td>Figure 16</td>
<td>The Import button</td>
<td>16</td>
</tr>
<tr>
<td>Figure 17</td>
<td>Execution Report</td>
<td>16</td>
</tr>
<tr>
<td>Figure 18</td>
<td>User Interface</td>
<td>17</td>
</tr>
<tr>
<td>Figure 19</td>
<td>Instrument Detected</td>
<td>18</td>
</tr>
<tr>
<td>Figure 20</td>
<td>Connection Established</td>
<td>18</td>
</tr>
<tr>
<td>Figure 21</td>
<td>Config Window</td>
<td>18</td>
</tr>
<tr>
<td>Figure 22</td>
<td>CPRI Tx and Rx Config Screen</td>
<td>19</td>
</tr>
<tr>
<td>Figure 23</td>
<td>RF Rx Config Screen</td>
<td>19</td>
</tr>
<tr>
<td>Figure 24</td>
<td>RF Tx Config Screen</td>
<td>20</td>
</tr>
<tr>
<td>Figure 25</td>
<td>Commit Configuration</td>
<td>20</td>
</tr>
<tr>
<td>Figure 26</td>
<td>CPRI 1 Rx Plot Window</td>
<td>20</td>
</tr>
<tr>
<td>Figure 27</td>
<td>RF Rx Plot Window</td>
<td>21</td>
</tr>
<tr>
<td>Figure 28</td>
<td>PuTTY Connection Config</td>
<td>21</td>
</tr>
<tr>
<td>Figure 29</td>
<td>Connection Established</td>
<td>22</td>
</tr>
<tr>
<td>Figure 30</td>
<td>Multicast Commands</td>
<td>22</td>
</tr>
<tr>
<td>Figure 31</td>
<td>Multicast Enabled</td>
<td>23</td>
</tr>
<tr>
<td>Figure 32</td>
<td>Start Tester traffic</td>
<td>23</td>
</tr>
<tr>
<td>Figure 33</td>
<td>Launch Debugger</td>
<td>24</td>
</tr>
<tr>
<td>Figure 34</td>
<td>Resume Application Execution</td>
<td>24</td>
</tr>
<tr>
<td>Figure 35</td>
<td>CPRI Diagnostics</td>
<td>25</td>
</tr>
<tr>
<td>Figure 36</td>
<td>CPRI 1 and 2 Windows</td>
<td>26</td>
</tr>
<tr>
<td>Figure 37</td>
<td>RF Rx1 and Rx2 Windows</td>
<td>26</td>
</tr>
<tr>
<td>Figure 38</td>
<td>Power Consumption of the DFE Wireless Radio</td>
<td>27</td>
</tr>
</tbody>
</table>
Tables

Table 1  Design Requirements ................................................................. 3
Table 2  Clocks ........................................................................................ 8
Table 3  Resource Utilization ................................................................. 10
Table 4  RRH RF Tx to MIMO RF Rx Connections ............................... 12
Table 5  MIMO RF Tx to RRH RF Rx Connections ............................... 12
Table 6  Jumper Settings ...................................................................... 13
1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0
The first publication of this document.
2 Wireless Radio Digital Front-End Design

This document describes the Microsemi PolarFire® wireless radio digital front-end (DFE) design and how to run the demo using the PolarFire Evaluation Board, Microsemi Wireless MIMO Daughter Card, and a Remote Radio Head (RRH) Tester.

The demo design features:

- Baseband interface using the CPRI IP
- Signal processing, Digital Up-Conversion (DUC) and Digital Down-Conversion (DDC)
- RFIC interface using the JESD204B IP
- Mi-V soft processor and its peripheral interfaces — SPI, GPIO, and UART
  Microsemi offers the Mi-V processor IP core and software toolchain to support RISC-V processor-based designs.

This fully integrated demo design is created using Microsemi Libero SoC PolarFire® to help customers build prototypes quickly.

The PolarFire Evaluation Board features:

- A 300K LE FPGA (MPF300TS, FCG1152) with 12.7 Gbps transceiver interface
- DDR3 and DDR4 interfaces
- A high pin count FMC connector for plugging in expansion boards

For more information, see the PolarFire Evaluation Kit page.

The wireless MIMO daughter card features:

- Two AD9371 RFIC chips for four transmit and four receive paths. Each chip supports:
  - 300 MHz to 6 GHz frequency range
  - Dual transmit and Dual receive paths
  - JESD204B digital interface
- AD9528, a two stage PLL with a JESD204B sysref generator
- A high pin count (HPC) FMC connector to connect to an FPGA base board

The RRH tester features:

- One-box solution including a Common Public Radio Interface (CPRI) and Tx/Rx paths
- Send and receive digital IQ data to and from the RRH using CPRI optical connection
- Software options for LTE FDD & TDD signal generation and analysis

For more information, see http://www.keysight.com/find/E6610A.
2.1 Design Requirements

The following table lists the design requirements for running the demo.

Table 1 • Design Requirements

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Host PC</td>
<td>with Windows 10 OS</td>
</tr>
<tr>
<td>Serial Terminal Emulation Program</td>
<td>PuTTY</td>
</tr>
<tr>
<td>Design Software</td>
<td></td>
</tr>
<tr>
<td>Libero SoC PolarFire</td>
<td>v2.2</td>
</tr>
<tr>
<td>SoftConsole</td>
<td>v5.2</td>
</tr>
<tr>
<td>Hardware</td>
<td></td>
</tr>
<tr>
<td>PolarFire Evaluation Kit</td>
<td>Rev C</td>
</tr>
<tr>
<td>MiMO Daughter Card</td>
<td></td>
</tr>
<tr>
<td>SFP+ transceiver modules</td>
<td>Wavelength: 1310 nm Class 1 DFB laser</td>
</tr>
<tr>
<td>Fiber patch</td>
<td>Cable Type: single mode fiber with yellow 2 mm jacket</td>
</tr>
<tr>
<td>RF SMA cables</td>
<td>PASTERNACK SMA Female to SMA Female Cables</td>
</tr>
<tr>
<td>Power Splitters</td>
<td></td>
</tr>
<tr>
<td>Test Hardware and Software</td>
<td></td>
</tr>
<tr>
<td>Remote Radio Head Tester</td>
<td>E6610A (700 MHz to 2.7 GHz)</td>
</tr>
<tr>
<td>E6610A User Interface</td>
<td>v2.9.5 (2x2 LTE)</td>
</tr>
</tbody>
</table>

2.2 Prerequisites

Before you start:

1. Download the design files from:
   http://soc.microsemi.com/download/rsc/?f=mpf_dg0839_liberosocpolarfirev2p2_df
2. Download and install Libero SoC PolarFire v2.2 from:
   https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polar-fire#downloads
3. Download and install SoftConsole v5.2 from:
   https://www.microsemi.com/product-directory/design-tools/4879-softconsole#downloads
4. Download and install Microsemi PowerMonitor from:
   http://soc.microsemi.com/download/rsc/?f=polarfire_power_monitor
5. Download and install KEYSIGHT E6610A User Interface from:
   http://www.keysight.com/find/E6610A_Software
2.3 Demo Design Architecture

The demo design supports a 4x4 MIMO, single carrier LTE 20 MHz bandwidth in the FDD mode. The basic system architecture consists of three main data modules—the CPRI IP, DUC and DDC blocks, and the JESD204B IP. The Mi-V soft processor is used for controlling and monitoring functions. The following figure shows the system architecture of the demo design.

Figure 1 • PolarFire Wireless Radio DFE Design Architecture

The following points describe the high-level data flow in the design:

1. The transmit IQ data from the baseband module is received on the Rx port of the CPRI IP and is de-mapped to four antenna carriers. This data is time-division multiplexed in the format required by the DUC chain.
2. The DUC block up-samples and up-converts the received data and then sends it to the JESD204B transmit interface.
3. Similarly, the JESD204B receive interface receives the data from the RFIC module and sends it to DDC for down-conversion and down-sampling.
4. The down-sampled data is then mapped to the four antenna carriers and sent to the Tx port of the CPRI IP.

2.3.1 Subsystem Components

The following sections describe the subsystems used in the design.

2.3.1.1 CPRI Interface

The CPRI IP is configured as a slave at 4.9 Gbps line rate with 4 antenna carriers (AxC), each carrying 20 MHz LTE bandwidth.

Figure 2, page 5 shows the CPRI interface.
The following points describe the port configurations of the CPRI IP:

- The TX and RX AxC data plane ports are enabled.
- The Ethernet TX and RX ports are disabled.
- The vendor specific data and AxC control data ports are looped back.
- The I and Q samples of each AxC are fixed at 15 bits.
- The user interface width is fixed at 32-bits. With zero appending on MSB, 15-bit wide I and Q samples are bit-stuffed in the 32-bit user interface width as shown in the following figure.

The transceiver data rate is set to 4.9 Gbps.

For more information about the CPRI IP, see UG0822: CPRI IP User Guide from Libero Catalog.

2.3.1.2 DUC and DDC

The DUC and DDC blocks are designed to support a single carrier LTE with 20 MHz bandwidth. These blocks are clocked at 245.76 MHz. The following figure shows the DUC structure for two antenna carriers. The same structure is replicated for the other two antenna carriers.

DUC contains a cascaded series of filters, which up-convert a 30.72 Msp sample rate to 122.88 Msp as per the following process.

1. The channel filter is a multi-channel FIR structure with 8 channels sampled at 30.72 Msp.
2. The two 4-channel half-band interpolation filters double the sample rate to 61.44 Msp.
3. The complex mixer and direct digital synthesizer (DDS) are used for up-conversion.
4. The output of the complex mixer is passed to the two 2-channel half-band interpolation filters to increase the sample rate to 122.88 Msps.

The following figure shows the DDC structure.

![DDC Diagram](image)

The DDC contains a cascaded series of filters, which down-convert a 122.88 Msps sample rate to 30.72 Msps as per the following process:

1. The two 2-channel half-band decimation filters convert the sample rate from 122.88 Msps to 61.44 Msps.
2. The complex mixer and direct digital synthesizer (DDS) blocks are used for down-conversion.
3. The output of the complex mixer is passed to the next two 4-channel half-band decimation filters to reduce the sample rate to 30.72 Msps.
4. The output of the decimation filters is passed to the multi-channel FIR structure with 8 channels sampled at 30.72 Msps.

### 2.3.1.3 JESD204B Interface

The JESD204B subclass 1 transmit and receive IPs are used at 4.9 Gbps rate. The JESD204B interface is configured to interface with the AD9371 RFIC. The following figure shows the JESD204B blocks.

![JESD204B Interface Diagram](image)

For each AD9371, the design includes a pair of JESD204B TX and RX blocks. The transceiver is configured for:

- Two lanes at 122.88 MHz clock—each lane carries 32-bit IQ data for a mixed signal converter.
- A 32-bit PCS interface.

For more information about the JESD204B TX and RX IPs, see [CoreJESD204BTX Handbook](#) and [CoreJESD204BRX Handbook](#).
2.3.1.4 Processor Subsystem

The Mi-V soft processor operates at 111.111 MHz and executes the user application code from an external DDR3. The following figure shows the Mi-V based processor system and its interfaces.

*Figure 7* • Mi-V Processor Subsystem

As shown in *Figure 7*, page 7, the Mi-V subsystem is used to initialize and monitor the CPRI IP via the AHB bus, and the external RFICs via the SPI interface. CoreSPI_0 is used to configure AD9528 and one RFIC chip (AD9371). CoreSPI_1 is used to configure the other RFIC chip. The CoreGPIO interface is used for the soft reset of the JESD204B interface. The CoreUART interface is reserved for internal design debugging.

For more information about how to build the Mi-V subsystem, see *TU0775: PolarFire FPGA: Building a Mi-V Processor Subsystem Tutorial*.

2.3.2 Clocking Structure

The clocking structure in the demo design is shown in the following figure.
As shown in Figure 8, page 8, the following points summarize the clocking structure:

- In the CPRI interface, the transceiver clock settings are as follows:
  - TX clock is set to Regional (TX_CLK_R) and the RX clock is set to Global (shared). As a result, both the RX regional (RX_CLK_R) and RX global (RX_CLK_G) clocks are enabled.
  - The jitter cleaner feature is enabled in the Tx PLL. The jitter cleaner derives its reference from the transceiver recovered clock to synchronize the TX_CLK clock.
  - The global RX clock serves as the reference to all the data modules in the system.
  - The CPRI interface uses the RX_CLK_R and TX_CLK_R (122.88 MHz) clocks.
  - The DUC and DDC blocks use the 245.76 MHz clock generated from the CCC0_1.
  - CCC0_1 also generates a 30.72 MHz fabric clock that is used as the reference clock by AD9528.
  - Using the 30.72 MHz reference clock, AD9528 generates the 122.88 MHz reference clock for JESD204B.
  - The Mi-V subsystem uses the 111.111 MHz clock generated from CCC0_0.
  - Using 111.111 MHz as the reference, the CCC0_2 block generates 666.666 MHz and 166.666 MHz clocks for the DDR3 block.

The following table lists all of the clocks used in the design, their source, frequency, and purpose.

<table>
<thead>
<tr>
<th>Clock Name</th>
<th>Source</th>
<th>Frequency</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mi-V_CLK</td>
<td>CCC0_0</td>
<td>111.111 MHz</td>
<td>Mi-V processor clock</td>
</tr>
<tr>
<td>DDR3-CLK</td>
<td>CCC0_2</td>
<td>666.666 MHz</td>
<td>DDR3 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td>166.666 MHz</td>
<td></td>
</tr>
<tr>
<td>RX_CLK_G</td>
<td>Transceiver RX recovered clock</td>
<td>122.88 MHz</td>
<td>CPRI RX</td>
</tr>
<tr>
<td>TX_CLK_G</td>
<td>Transceiver TX PLL</td>
<td>122.88 MHz</td>
<td>CPRI TX</td>
</tr>
</tbody>
</table>
2.3.3 Reset Structure

The reset structure in the demo design is shown in the following figure.

**Figure 9 • Reset Structure**

As shown in Figure 9, page 9, the following points summarize the reset structure of the design:

- The reset signal from the RISC-V top module drives the reset of all the other modules in the design.
- The onboard push button reset, device initialization init_done, and the PLL lock signals generate the reset signal (Reset) for all the components of the Mi-V subsystem.
- TX_PLL and transceiver RX_Ready signals in CPRI are ANDed with the Mi-V Reset to generate the reset signal (Cpri_ready) for all of the components of the CPRI top module.
- The Mi-V reset signal also resets the CPRI transceiver.
- Cpri_ready and PLL lock signals generate the reset signal for the DDCDUC_TOP module.
- Mi-V reset, PLL lock, and soft reset signals generate the reset for all the components in the JESD_TOP module.
2.3.4 Resource Utilization

The following table lists the resource utilization of the design on the MPF300TS_ES device (FCG1152, speed grade -1).

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>79298</td>
<td>299544</td>
<td>26.47</td>
</tr>
<tr>
<td>DFF</td>
<td>73655</td>
<td>299544</td>
<td>24.59</td>
</tr>
<tr>
<td>µSRAM</td>
<td>1315</td>
<td>2772</td>
<td>47.44</td>
</tr>
<tr>
<td>LSRAM</td>
<td>116</td>
<td>952</td>
<td>12.18</td>
</tr>
<tr>
<td>Math</td>
<td>326</td>
<td>924</td>
<td>35.28</td>
</tr>
<tr>
<td>PLL</td>
<td>3</td>
<td>8</td>
<td>37.5</td>
</tr>
<tr>
<td>Transceiver Lanes</td>
<td>5</td>
<td>16</td>
<td>31.25</td>
</tr>
</tbody>
</table>

2.3.5 Timing Closure in Libero

In Libero SoC PolarFire, the timing constraints are derived for the top module of the design from Design Flow > Constraint Manager. The generated SDC file includes clock definitions based on the PLLs used in the design and constraints specific to IP cores.

Timing issues can be analyzed and cross-probed using SmartTime and ChipPlanner. These applications are integrated in Libero SoC PolarFire.

To close the timing of the wireless radio DFE design at 245 MHz, the following options and guidelines were followed.

- Input and output data registers of hard blocks such as MACC and RAM were enabled in the RTL. Also, used dedicated CDIN and CDOUT lines for the MACC blocks.
- The syn_preserve directive was used in the RTL of repetitive modules inside DUC and DDC subsystems. This directive avoids the usage of shared nets across modules and duplicates nets for each module to give better timing.
- Asynchronous resets were used in the design.
- The required synchronizer circuitry was used for clock domain crossings. And then, all of the asynchronous clock groups were defined (set_clock_groups) in an SDC file for faster Place and Route cycles.
- Using SmartTime results, the maximum fanout limit was set on individual nets instead of setting the fanout for the overall design.

Note: The Place and Route configuration options, High Effort Layout and Repair Minimum Delay Violations must be enabled only when the timing paths have a lower negative slack with respect to the clock timing constraint. The smart time analysis must be done with these options disabled during initial runs.
3 Hardware Data Flow

The following figure shows the high-level data flow between the RRH tester, MIMO card, and the PolarFire evaluation board.

*Figure 10 • Data Flow*
4 Setting Up the Demo

This section describes steps to successfully program the FPGA, its Non-volatile memory (sNVM), and run scripts to configure Jitter attenuator PLLs.

Setting up the demo involves the following steps:

1. **Setting up the Hardware**, page 12
2. **Programming the PolarFire Device**, page 15
3. **Enabling Jitter Cleaner on CPRI TX PLL**, page 15

4.1 Setting up the Hardware

This section describes how to connect all of the components required to run the demo.

Follow these steps:

1. Connect the Host PC and the RRH tester to the same LAN using RJ45 cables.
2. Connect the USB cable from the Host PC to J5 (FTDI port) on the evaluation board. On the evaluation board, DS15, DS24, DS23, DS25, and DS26 LEDs glow.
3. Plug in one SFP module into the SFP1 port of the RRH tester and the other SFP module into J35 (SFP case) on the evaluation board. Connect both these SFP modules using the fiber patch.
4. Connect the MIMO card to the evaluation board using the J34 FMC connector.
5. Connect the two RRH RF Tx ports to the 4 RF Rx ports of the MIMO using power splitters as listed in the following table.

<table>
<thead>
<tr>
<th>RRH Tx Port</th>
<th>MIMO Card Rx Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx1</td>
<td>J500 (RX1 of U12) and J522 (RX1 of U15)</td>
</tr>
<tr>
<td>Tx2</td>
<td>J501 (RX2 of U12), J519 (RX2 of U15)</td>
</tr>
</tbody>
</table>

6. Connect the two RF TX ports of the MIMO card to the two Rx ports of the RRH tester as listed in the following table.

<table>
<thead>
<tr>
<th>MIMO Card Tx Port</th>
<th>RRH Rx Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX1 (J508) of U12</td>
<td>Rx1</td>
</tr>
<tr>
<td>TX2 (J509) of U12</td>
<td>Rx2</td>
</tr>
</tbody>
</table>

**Note:** To see the RF output from the TX1 and TX2 ports U15 of the MIMO card, connect TX1 (J524) and TX2 (J526) to Rx1 and Rx2 ports.

**Figure 11**, page 13 shows the complete SMA connections.
7. Ensure that the following jumper settings are made on the evaluation board.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>J39</td>
<td>Short 1 and 2 for enabling the Tx port of the SFP</td>
</tr>
<tr>
<td>J46</td>
<td>Open 1 and 2 for enabling the 122.88 MHz oscillator</td>
</tr>
<tr>
<td>J47</td>
<td>Open 1 and 2</td>
</tr>
<tr>
<td>J12</td>
<td>short 5 and 6 for 1.8V</td>
</tr>
</tbody>
</table>

8. Connect the power supply cable to the J9 connector on the evaluation board.
9. Connect the RRH tester to the power supply using the power adapter.
10. Power-up the evaluation board using the SW3 slide switch.
    On the evaluation board, the power regulator LEDs (DS3 - DS14) glow. And, LEDs DS4 and DS8 on the MIMO card also glow.
11. Power-up the RRH tester using the POWER switch at the back chassis.
    After the RRH tester initialization, LEDs SYS PLL, AxC Tx and Rx glow, RF Tx and Rx glow, and STS blinks.

The complete setup is shown in the following figure.
Figure 12 • Hardware Setup
### 4.2 Programming the PolarFire Device

After setting up the hardware, you must program the device.

To program the device:

1. Start Libero SoC PolarFire v2.2.
2. Open the PRJX file from the following location:
   ```text
   mpf_dg0839_liberosocpolarfirev2p2_df\Libero_Project
   ```
3. From the Libero design flow, double-click the **Run PROGRAM Action** option.
   The following message appears after the device is successfully programmed.

   ![Device Programmed](image)

   **LED 10 glows and LED 11 blinks after the device is successfully programmed.**

   **Note:** Keep Libero SoC PolarFire v2.2 open to enable jitter cleaner as described in the following section.

### 4.3 Enabling Jitter Cleaner on CPRI TX PLL

The design files includes a TCL script file, which enables jitter cleaner on CPRI TX PLL. The script must be executed using SmartDebug.

To execute the script:

1. From the Libero design flow, double-click the **SmartDebug Design** option.

   ![Starting SmartDebug](image)

2. Select **File > Execute Script** as shown in **Figure 15**, page 16.
3. Click the **Import** button to import the TCL file as shown in the following figure.

4. Double-click the `CPRI_JA_Enable.tcl` file from the following location, and click **Run**.
   
   mpf_dg0839_liberosocpolarfirev2p2/Libero_Project

   After the successful execution of the script, the log window shows the following report.

5. Close SmartDebug.

   **Note:** Run the script every time the evaluation board is power cycled.
5 Running the Demo

This section describes steps to successfully run the demo and observe the 64 QAM constellation of a 2x2 20 MHz MIMO system.

Running the demo involves the following steps:

1. Configuring and Monitoring the RRH Tester, page 17
2. Executing the User Application, page 23
3. Monitoring the Performance, page 25

5.1 Configuring and Monitoring the RRH Tester

The E6610A user interface is used to configure the carrier technology and bandwidth, CPRI parameters like line rate, bit width, and IQ mapping, and to configure the RF parameters like frequency, waveform, and power levels (for Tx and Rx). The user interface is also used to monitor the RRH tester. Monitoring the tester involves observing the analog and digital data at RF Rx and CPRI Rx respectively.

This section is divided into the following steps:

1. Configuring the Tester, page 17
2. Monitoring the Tester, page 20
3. Enabling Multicast on CPRI, page 21

5.1.1 Configuring the Tester

To configure the RRH tester:

1. From the host PC desktop, start the E6610A user interface.
   The main window of the user interface is displayed as shown in the following figure.

   Figure 18 • User Interface

2. Click Search to detect the RRH tester connected to the LAN.
The IP address of the RRH tester and the following message is displayed as shown in the following figure.

**Figure 19 • Instrument Detected**

![Instrument Detected](image)

**Note:** The IP address of the RRH tester varies from one LAN to the other.

3. Click **Connect** to connect to the RRH tester.
   The following message is displayed after a successful connection.

**Figure 20 • Connection Established**

![Connection Established](image)

4. Configure the carrier technology, bandwidth, and CPRI parameters as shown in the following figure.

**Figure 21 • Config Window**

![Config Window](image)

5. Configure the CPRI Tx and Rx parameters as shown in the following figure.
6. Configure the RF Rx parameters as shown in the following figure.

*Figure 22 • CPRI Tx and Rx Config Screen*

*Figure 23 • RF Rx Config Screen*
7. Configure the RF Tx parameters as shown in the following figure.

*Figure 24 • RF Tx Config Screen*

8. Click **Commit to E6610A** to commit the configuration.

*Figure 25 • Commit Configuration*

### 5.1.2 Monitoring the Tester

The time domain, frequency domain, and the EVM constellation plots of the data received at the CPRI Rx and RF Rx ports must be observed. These windows must be opened to view the various plots.

Follow these steps:

1. Select **New Window > CPRI 1 > Time Domain IQ** as shown in the following figure.

*Figure 26 • CPRI 1 Rx Plot Window*

2. Similarly, open the CPRI 1 Rx frequency domain, and EVM constellation plot windows.
3. Similarly, open the CPRI 2 Rx time and frequency domain, and EVM constellation plot windows.
4. Select **New Window > RF Rx1 > Time Domain IQ** as shown in the following figure.
5. Similarly, open the RF Rx1 frequency domain, and EVM constellation plot windows.
6. Similarly, open the RF Rx2 time and frequency domain, and EVM constellation plot windows.
7. Select **New Window > CPRI Diagnostics** to monitor the CPRI link.

### 5.1.3 Enabling Multicast on CPRI

The RRH tester supports Multicast in the down link. The multicast feature creates copies of the CPRI 1 and CPRI 2 IQ data streams and places them in the additional antenna containers that the RRH can use to map to other antenna ports. Multicast is used in the demo to get the CPRI 1 and 2 IQ data on the other 2 antennas.

From the host PC, PuTTY must be used to connect to the tester. After connecting, multicast must be enabled on CPRI.

To enable multicast:

1. From the host PC desktop, start PuTTY.
2. Enter the hostname, port number, and select the **Connection Type** as shown in the following figure.

#### Figure 28 • PuTTY Connection Config

3. Type the commands shown in the following figure and click **Enter** to connect to the Tester. After connecting, the return code 1 is displayed as shown in the following figure.
4. Copy multicast commands shown in the following figure and paste it on PuTTY.

**Figure 30 • Multicast Commands**

```
CLS
SOURCE:PLAYback:STATE OFF
CONFIGure:RAT:TYPE LTE
CONFIGure:RAT:MODE FDD
CONFIGure:RAT:Btn 29,Consecutive
CONFIGure:CPU:BTWidth 15
SOURCE:CPU:Noise consecutive
SOURCE:CPU:ARB:Multicast ON
SOURCE:Radio:ARB:MODE TM31
SOURCE:Radio:Mode:Multicast ON
SOURCE:Radio:ARB:STATE ON
CONFIGure:SEMPCR:CAT0PT2
SOURCE:Radio:ARB:Trigger -0.000000
SOURCE:Radio:Connection 30.000000
SOURCE:Radio:FREQuency 2140000
SOURCE:Radio:POWER 55.000000
CONFIGure:TXPulse:Len1:RBW 1
SENSe:Radio:FREQuency 1730000
SENSe:Radio:Level 30.000000
SENSe:Radio:CAPture:DEpth 11.000000
SENSe:Radio:CAPture:TRigger -0.500000
SENSe:Radio:CAPture:MODEL TM31
SENSe:CPU:ARB:IDLEvEl -21.000000
SENSe:CPU:ARB:TRigger -0.500000
SENSe:CPU:ARB:CONversion? 0
SOURCE:Radio:ARB:MODE TM31
SOURCE:Radio:ARB:STATE ON
CONFIGure:SEMPCR:CAT0PT2
SOURCE:Radio:ARB:TRigger -0.000000
SOURCE:Radio:Connection 30.000000
SOURCE:Radio:FREQuency 2140000
SOURCE:Radio:POWER 55.000000
CONFIGure:TXPulse:Len2:RBW 1
SENSe:Radio:FREQuency 1730000
SENSe:Radio:Level 30.000000
SENSe:Radio:CAPture:DEpth 11.000000
SENSe:Radio:CAPture:TRigger -0.300000
SENSe:Radio:CAPture:MODEL TM31
SENSe:CPU:ARB:IDLEvEl -21.000000
SENSe:CPU:ARB:TRigger -0.500000
SENSe:CPU:ARB:CONversion? 0
SOURCE:Radio:ARB:STATE ON
SENSe:CPU:ARB:CAPture:TRigger -0.500000
SENSe:Radio:CONversionFactor?
TRigger:SYNC:OUT:STATE OFF
TRigger:SRC:SOURCE AUTO
SOURCE:PLAYback:STATE ON
SENSe:CPU:CAPture:STATE ON
SENSe:CPU:CAPture:STATE ON
SENSe:Radio:CAPture:STATE ON
SENSe:Radio:STATE:STATE ON
SOURCE:Radio:STATE ON
SOURCE:Radio:STATE ON
SENSe:Radio:STATE ON
SENSe:Radio:STATE ON
SYSTEM:ERROR:COMM?
SENSe:CPU:ARB:Multicast?
SENSe:CPU:ARB:IDLEvEl?
```

The following figure shows the status and return codes displayed after multicast is successfully enabled.
5. Click Run to start the CPRI and RF traffic from the tester.

5.2 Executing the User Application

Using SoftConsole, the user application must be launched in the debug mode. CPRI registers and devices on the MIMO card are initialized after the debugger executes the main function. The main function also monitors the CPRI link.

To execute the user application:

1. From the host PC desktop, start SoftConsole v5.2.
2. In the workspace launch window, enter the following location and click Launch.
   
   mpf_dg0839_liberosocpolarfirev2p2\Libero_Project\SoftConsole

3. The user application is launched in the debug mode.
4. Click the debug option as shown in the following figure.
5. In the debug window, click the Resume option to execute the main function.

**Figure 33 • Launch Debugger**

The application is executed and LED 4, 5, 6, 7, 8, and 9 on the evaluation board glow. On the MIMO card LEDs, DS6 and DS7 glow. This indicates that the wireless radio DFE design is up and running.

The CPRI diagnostics window shows the link up status as shown in the following figure.
5.3 Monitoring the Performance

After the wireless design is up and running, the RF and baseband plot windows display the data as shown in Figure 36, page 26 and Figure 37, page 26.

The plots show the 20 MHz occupied bandwidth data correctly decoded for the 64 QAM constellation on LTE TM3.1.
Running the Demo

Figure 36 • CPRI 1 and 2 Windows

Figure 37 • RF Rx1 and Rx2 Windows
6 Power Measurements

This section describes how to monitor the real-time power consumption of the wireless radio DFE design using PowerMonitor.

PolarFire Evaluation Board comes with a power monitoring solution implemented using the on-board SmartFusion A2F 200 device and the PowerMonitor application. The PowerMonitor application connects to the power monitoring program running on the A2F 200 device to measure power.

For more information about PowerMonitor, see UG0747: PolarFire FPGA Evaluation Kit User Guide.

Follow these steps:

1. On the host PC desktop, click Start and select PowerMonitor.
2. In the COMPort Setup dialog box, select the highest COM port from the drop-down and click Connect.

   The PowerMonitor application successfully connects to the board and starts displaying the Core Fabric (VDD) power, Fabric PLL (VDD25) power, Transceiver Core (VDDA) power, and Transceiver PLL (VDDA25) power as shown in the following figure.

**Figure 38 • Power Consumption of the DFE Wireless Radio**

As shown in Figure 38, page 27, the power consumed by a 2x2 20 MHz MIMO application running on a PolarFire device is only 2.66 W.

6.1 Conclusion

This demo shows that PolarFire FPGA designs can be successfully used in wireless communication applications such as small cell and RRH. The demo also demonstrates the low power advantages of using PolarFire FPGAs in such applications.