UG0830
User Guide
PolarFire FPGA Low Voltage Differential Signaling 7:1

Microsemi
Power Matters.™

Microsemi
Power Matters.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

The first publication of this document.

2 Low Voltage Differential Signaling 7:1

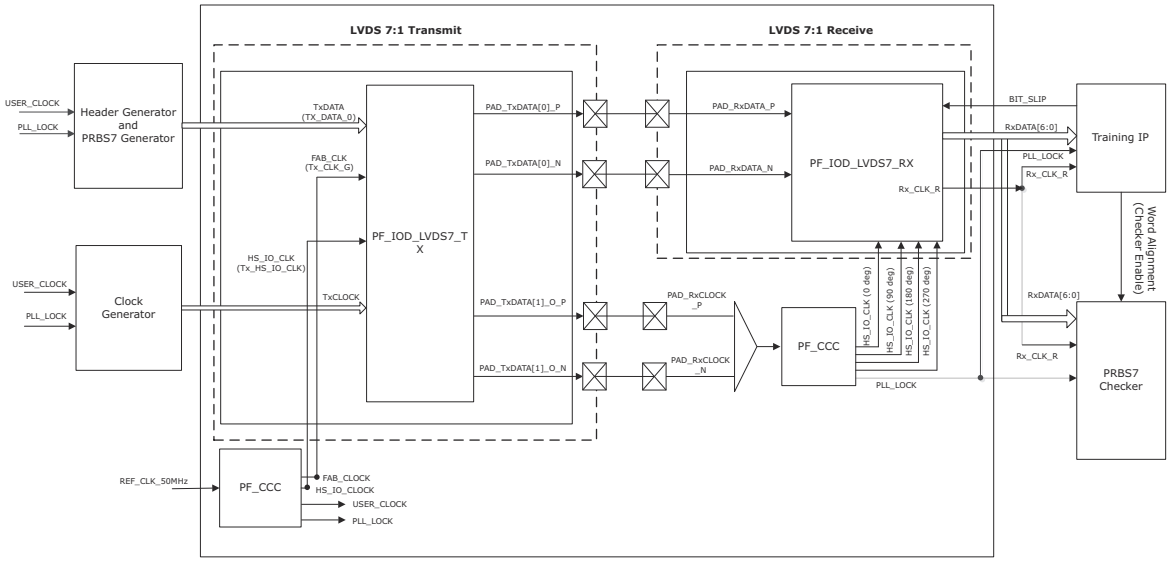
Low-voltage differential signaling (LVDS) is a high-speed, low-power, general-purpose interface standard. Also known as the ANSI/TIA/EIA-644 standard, LVDS was approved in March 1996. LVDS uses differential signaling with a nominal signal swing of 350 mV differential. The low signal swing decreases rise and fall times to achieve the maximum transmission rates specified in the LVDS standard. LVDS signal swing does not depend on the voltage of any specific supply. LVDS uses current mode drivers, which limit power consumption. The differential signals are immune to ±1 V common voltage noise. The Channel-Link technology was originally developed as a solution for flat panel displays, using LVDS for the physical layer (PHY). The technology was then extended into a method for general purpose data transmission. Channel-Link consists of a driver pair and a receiver pair. The application note performs a loop back test on Microsemi PolarFire Evaluation Kit to validate the LVDS 7:1 functionality.

The LVDS 7:1 solution uses PF_IOD_LVDS7_TX and PF_IOD_LVDS7_RX macros from Libero catalog to handle parallel to serial and serial to parallel conversion respectively. IOD configured for transmit, serializes the parallel data and transfers low-speed parallel data from the fabric to high-speed output clock domain. IOD configured for receive, receives high-speed clock domain serial data and de-serializes the data.

The Transmit user logic includes a header pattern generator and pseudo and random pattern generator - 7 (PRBS7). The user logic transmits header pattern followed by a PRBS7 pattern. The header pattern is used by receive logic to achieve word alignment. The user logic also generates a clock with a 4:3 duty cycle. The LVDS 7:1 solution consists of two LVDS pairs: a data pair and a clock pair. Each cycle of the transmit clock output includes seven bits of serialized data.

The following figure depicts high-level functional block diagram.

Figure 1 • **LVDS 7:1 Block Diagram**



The LVDS 7:1 transmit and receive blocks perform the following functions:

1. The transmit user data is interfaced to PF_IOD_LVDS7_TX, which serializes the data. Transmit IOD multiplies the parallel clock by 3.5 and transmits seven serial bits of data in one parallel clock cycle.
2. PF_IOD_LVDS7_RX receives the phase-shifted HSIO clocks and de-serializes the received data. The Training IP generates a bit slip pulse. PF_IOD_LVDS7_RX receives the pulse for the word alignment.
3. After the word alignment, the PRBS7 auto checks and provides the PRBS lock signal. The PRBS lock and word alignment signal are promoted to top-level for monitoring.

3 Hardware Implementation

This section describes the implementation LVDS 7:1 transmit and receive modules.

3.0.1 LVDS 7:1 Transmit Module

The LVDS 7:1 transmit module generates the header data followed by PRBS7 data. The clock generator logic generates a clock with 4:3 duty cycle. Transmit module output consists of one data and a clock pair. Transmit IOD multiplies the parallel clock by 3.5 and transmits seven serial bits of data in one parallel clock cycle. The IO features are set by Libero configurator with in Libero SoC PolarFire. PF_IOD_LVDS_TX is configured for two outputs, one for data and one for clock. PF_IOD_LVDS_TX has two parallel data inputs, the first input is interfaced with header and PRBS7 generator and an another is interfaced with clock generator. PF_IOD_LVDS7_TX ports and lane controller must be assigned to the same physical lane. The port assignment for the interface must meet this requirement.

Figure 2 • **LVDS 7:1 Transmitter Block Diagram**

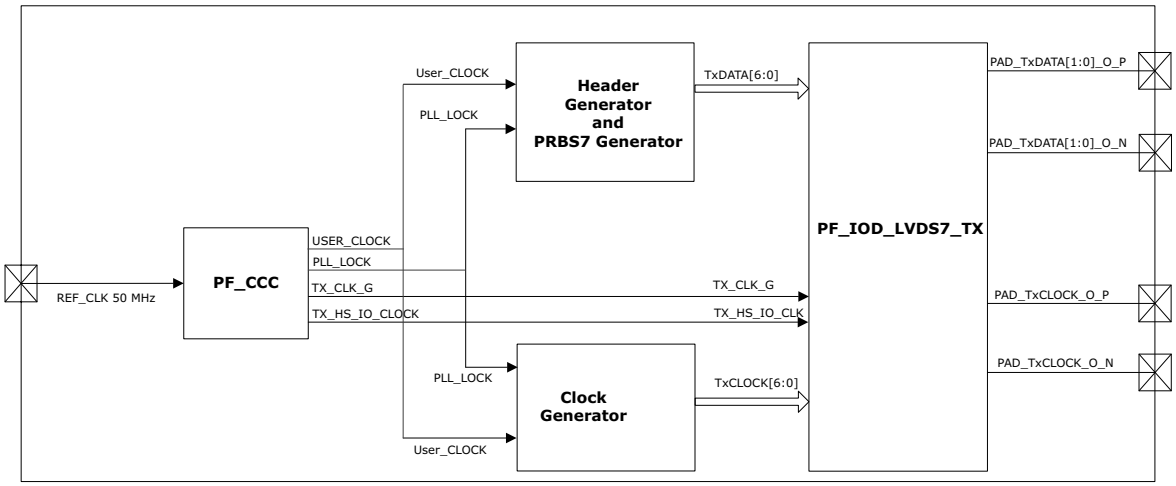
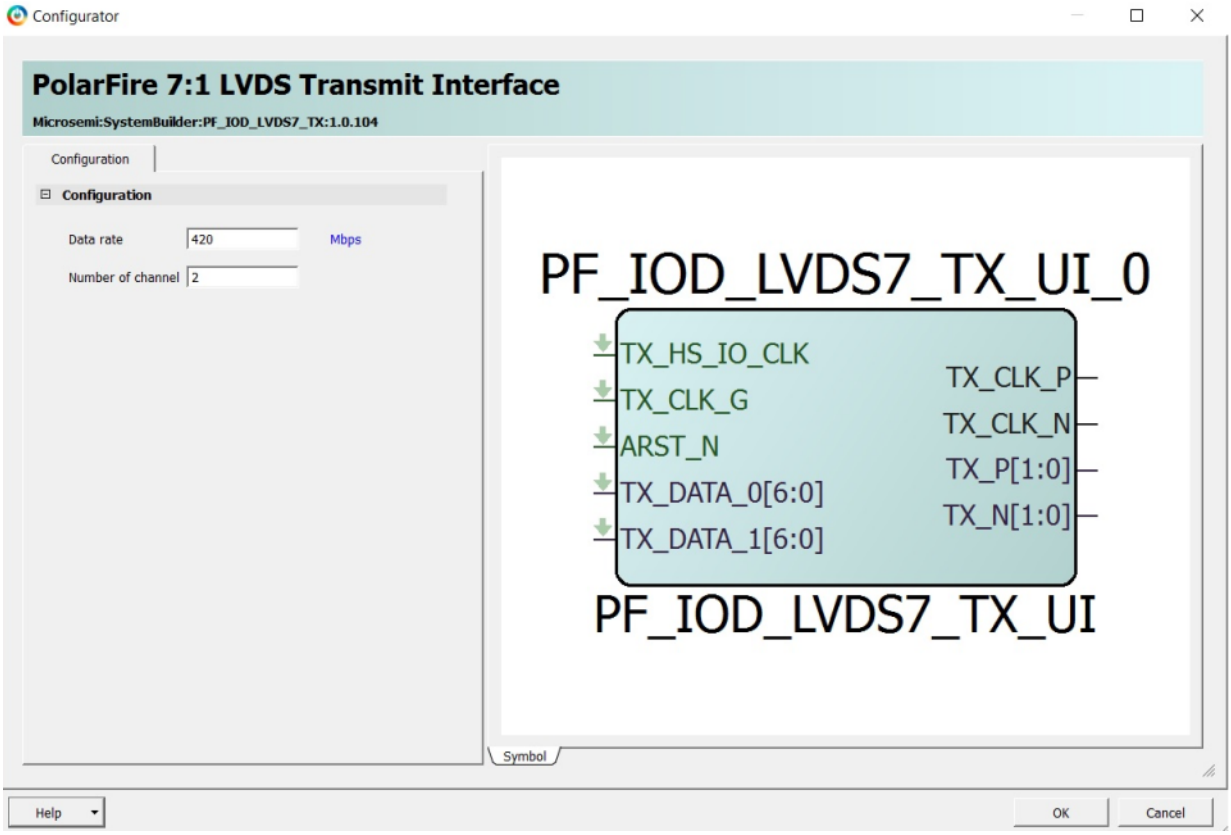


Figure 3 • **PF_IOD_LVDS7_TX Configurator**



3.0.2 LVDS 7:1 Receive Module

The LVDS 7:1 receive module receives serial data and source synchronous parallel clock. The serial data is input to receive PF_IOD_LVDS7_RX. The serial data is received on an IOA pair and sent to associated IOD block. For more information, see *UG0686: PolarFire FPGA User I/O User Guide*. Receive IOD block includes an input delay function, IO registers and digital logic blocks. IOD block also includes several high speed low skew clock networks. The IO features are set by Libero configurator with in Libero SoC PolarFire. Eye monitor and bit slip are enabled.

The Fabric CCC block generates four serial bank clocks (HS_IO_CLK) with phase shifts of 0 degree, 90 degree, 180 degree and 270 degree respectively. The frequency of each serial clock is 3.5 times the input received clock. The four generated serial bank clocks are inputs to receive PF_IOD_LVDS7_RX and used for generating recovered clock (RX_CLK_R). The downstream IP and logic blocks use the recovered clock. PF_IOD_LVDS_RX7 ports and lane controller must be assigned to the same physical lane. The port assignment for the interface must meet this requirement.

The Training IP in receive block accepts the parallel data from receive IOD and uses it to generate bit slip pulses to achieve word alignment with respect to the transmit header pattern. Each bit slip pulse input from Fabric, slips two bits at a time. After achieving word alignment the Training IP asserts word alignment signal which is interfaced to PRBS7 checker block. The PRBS7 checker starts auto checking

after word alignment signal is asserted. The word alignment and PRBS7 signals are promoted to FPGA top for observing the signal on scope.

Figure 4 • **LVDS 7:1 Receiver Block Diagram**

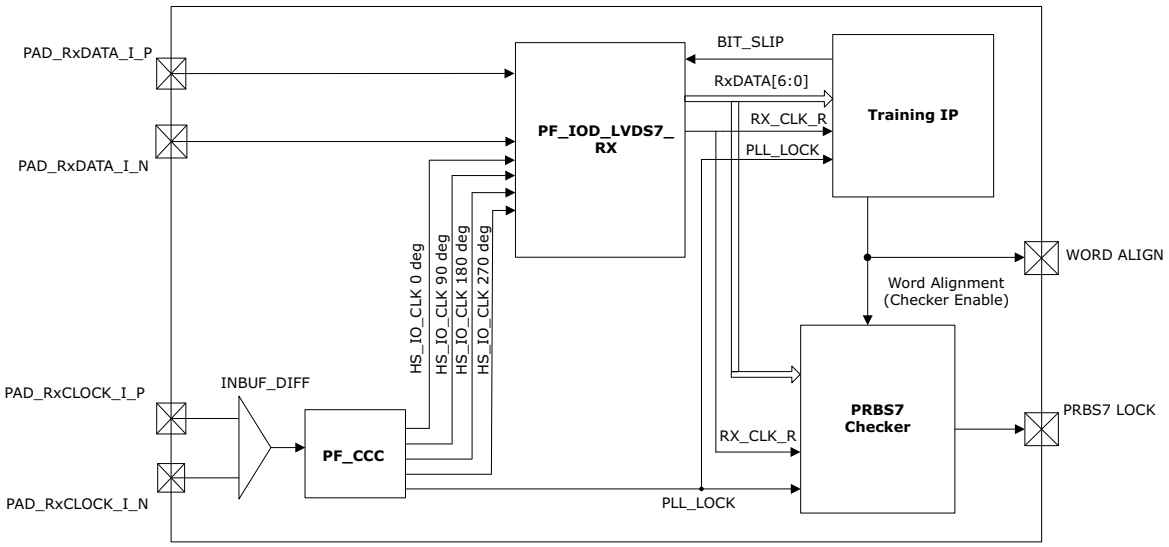
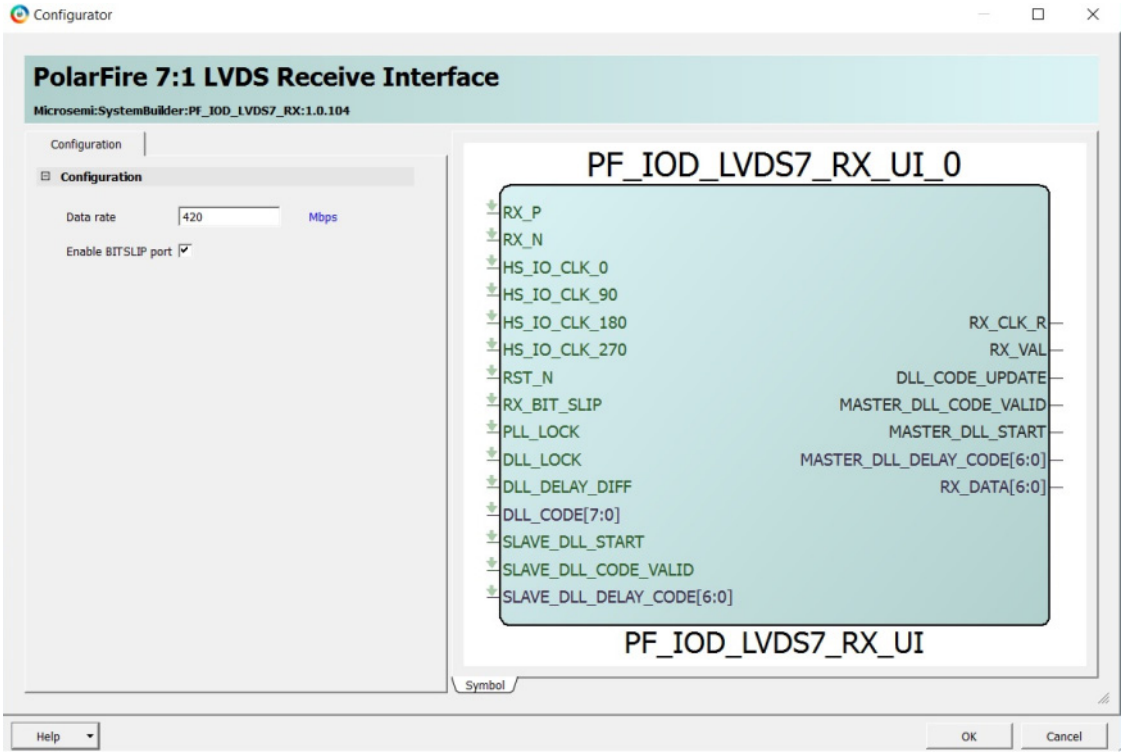


Figure 5 • **PF_IOD_LVDS7_RX Configuration**



3.1 Inputs and Outputs

The following table lists the LVDS 7:1 receiver interface input and output ports.

Table 1 • **LVDS 7:1 Receiver Interface Ports**

Signal Name	Direction	Width (bits)	Description
PAD_RxDATA_I_P	In	1	Differential DDR Receive Serial DATA - P
PAD_RxDATA_I_N	In	1	Differential DDR Receive Serial DATA - N
PAD_RxCLOCK_I_P	In	1	Differential DDR Receive Parallel CLOCK - P
PAD_RxCLOCK_I_N	In	1	Differential DDR Receive Parallel CLOCK - N
WORD ALIGN	Out	1	Word Align Signal. Training IP uses bit slip signal to achieve word alignment. Asserted when IOD RxData[6:0] is word aligned with transmit header.
PRBS7LOCK	Out	1	Asserted when PRBS7 checker achieves lock.

The following table lists the LVDS 7:1 transmit interface input and output ports.

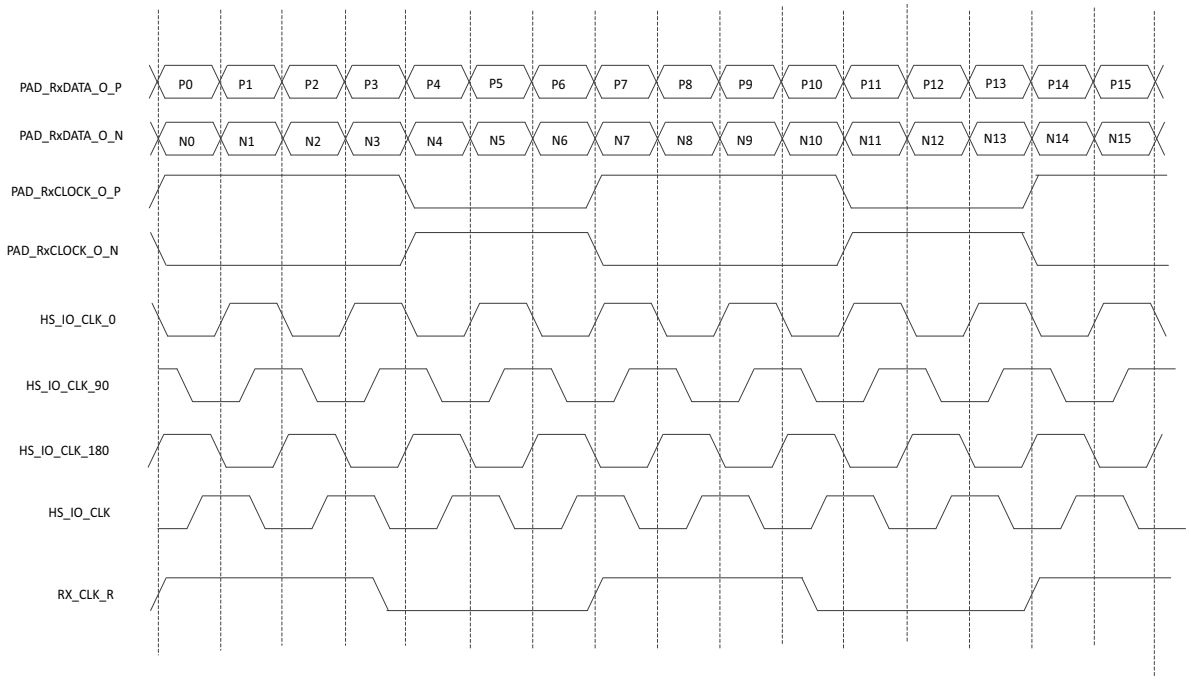
Table 2 • **LVDS 7:1 Transmitter Interface Ports**

Signal Name	Direction	Width (bits)	Description
REF_CLK_50MHz	In	1	Reference Clock 50 MHz
PAD_TxDATA[1:0]_O_P	Out	2	Differential DDR transmit Serial DATA - P
PAD_TxDATA[1:0]_O_N	Out	2	Differential DDR transmit Serial DATA - N
PAD_TxCLOCK_O_P	Out	1	Differential DDR transmit Parallel CLOCK - P
PAD_TxCLOCK_O_N	Out	1	Differential DDR transmit Parallel CLOCK - N

3.2 Timing Diagrams

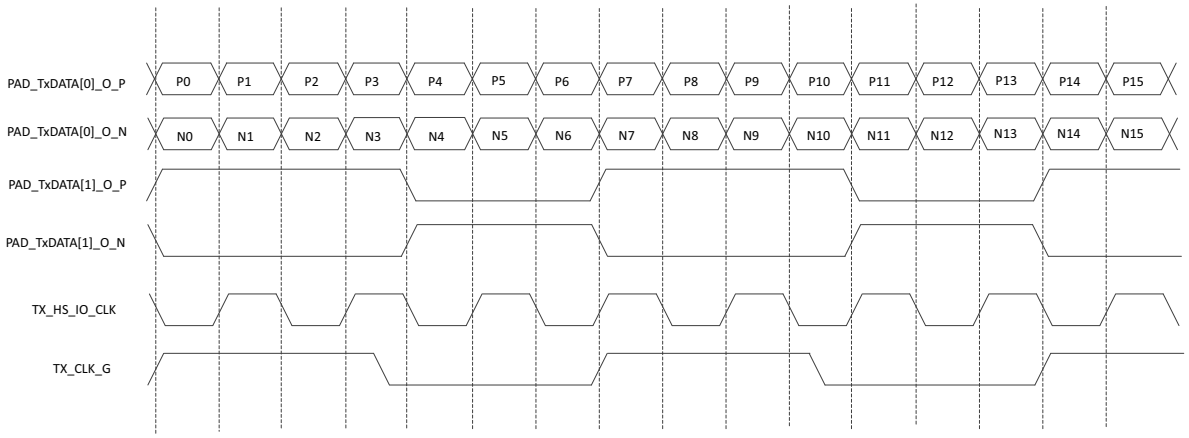
The following figure shows the timing diagram for the LVDS 7:1 receiver.

Figure 6 • **LVDS 7:1 Receiver Timing Diagram**



The following figure shows the timing diagram for the LVDS 7:1 transmitter.

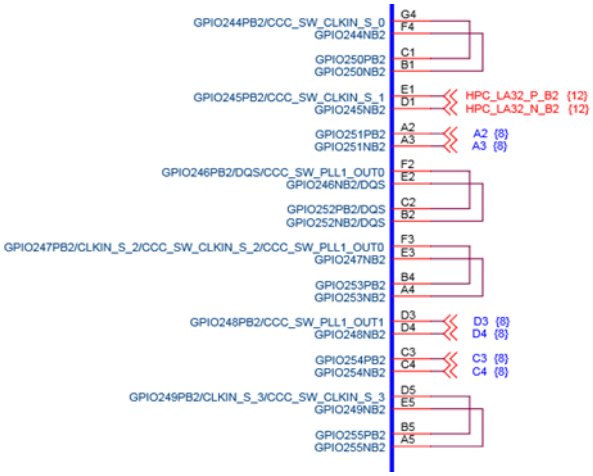
Figure 7 • **LVDS 7:1 Transmitter Timing Diagram**



3.3 Loopback Test

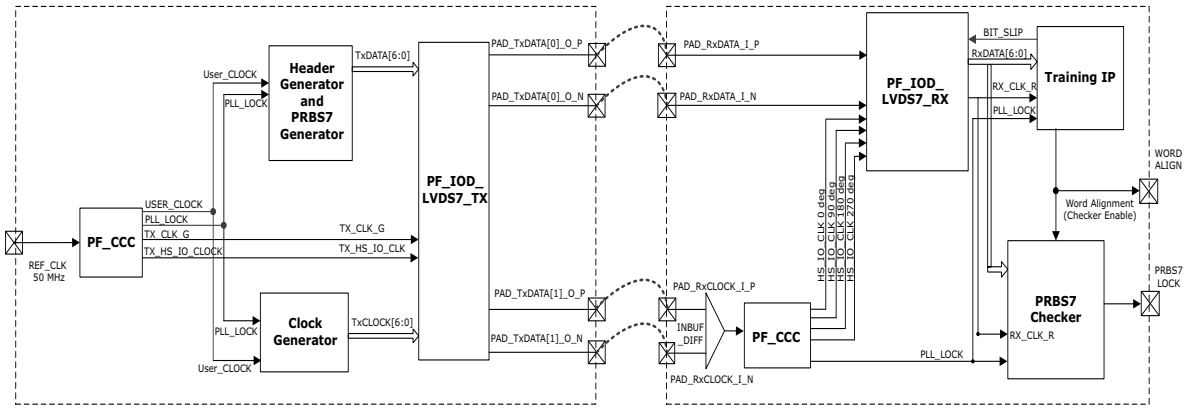
A loopback test is performed on the Microsemi PolarFire Evaluation Kit - MPF300TS to validate the LVDS 7:1 functionality. The test setup consists of one parallel transmit and receive channels (one data channel and one clock channel). The PolarFire Evaluation Kit provides four length-matched PCB trace loop back pairs for IO Bank 2 as shown in Figure 8, page 8. For more information on board schematics, see *Polarfire Evaluation Kit Schematics*.

Figure 8 • **PCB Trace Loopback**



The following figure shows the test setup for the LVDS 7:1 loopback test.

Figure 9 • **LVDS 7:1 Loopback Test Setup**



3.4 Performance Statistics

The performance details of the LVDS 7:1 design will be updated in the next revision.

3.5 Resource Utilization

The following tables lists the resource utilization of the LVDS 7:1 design on a MPF300TS device.

Table 3 • **LVDS 7:1 Transmit Resource Utilization**

Resource	Usage
Fabric 4 LUT	37
Fabric DFF	68
PLL	1

Table 4 • **LVDS 7:1 Receiver Resource Utilization**

Resource	Usage
Fabric 4 LUT	365
Fabric DFF	191
PLL	1
DLL	1

3.5.1 Clocking Scheme

The following table lists the PLLs configuration utilized in the design.

Table 5 • **Configuration**

PolarFire PLLs	Ref. Input Clock	PLL Outputs
Receiver module PLL PF_CCC_0	70 MHz	OUT0_HS_IO_CLK (HS_IO_CLK with 0 deg phase) = 245MHz OUT1_HS_IO_CLK (HS_IO_CLK with 90 deg phase) = 245MHz OUT2_HS_IO_CLK (HS_IO_CLK with 180 deg phase) = 245 MHz OUT3_HS_IO_CLK (HS_IO_CLK with 180 deg phase) = 245 MHz
Transmitter module PLL PF_CCC_0	50 MHz	OUT0_FABCLK (FAB_CLK) = 70 MHz OUT2_HS_IO_CLK (HS_IO_CLK) = 245 MHz OUT3_FABCLK (USER_CLK) = 35 MHz
PF_IOD_LVDS7_RX	70 MHz	Rx_CLK_R (Rx downstream recovered clock) = 70 MHz