AC474
Application Note
Metastability Characterization Report for RTG4

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

The first publication of this document.

2 Metastability Characterization Report For RTG4 FPGAs

Whenever asynchronous data is registered by a clocked flip-flop, there is a probability of setup or hold time violation on that flip-flop. In applications such as synchronization or data recovery, due to the asynchronous nature of the data input to the flip-flops, the data transition time is unpredictable with respect to the active edge of the clock. The susceptibility of a circuit to reach this metastable state can be described using a probabilistic equation. Setup or hold violations cause the output of the flip-flop to enter a symmetrically balanced transient state, called a metastable state. The metastable state is manifested in a bistable device by the outputs glitching, going into an undefined state somewhere between a "1" and "0," oscillating, or by the output transition being delayed for an indeterminable time. Once the flip-flop has entered the metastable state, the probability that it will still be metastable later has been shown to be an exponentially decreasing function of time. Because of this property, a designer should simply wait for additional time after the specified propagation delay before sampling the flip-flop output so that the designer can be assured that the likelihood of metastable failure is remote enough to be tolerable. The additional time of waiting becomes shorter, even though still more than zero, as the technology improves and semiconductor devices reach higher ranges of speed.

This document describes the metastability equations followed by the metastability characterization of Microsemi RTG4 FPGAs. This application note also provides an example on the usage of the metastability equations.

2.1 Theory of Metastability

In general, the mean time between failures (MTBF) should be defined statically. Figure 1 on page 2 depicts a simple circuit, used to synchronize asynchronous data with the system clock. EQ1 shows the relation between MTBF and the clock-to-out settling time of a flip-flop:

$$MTBF = \left(e^{(T_s/\tau)}\right)/(T_o \cdot f_d \cdot f_c)$$

EQ1

$$T_s = T_{co} + T_{met}$$

EQ2

In EQ1 and EQ2:

T_s = Total flip-flop output settling time.

T_{co} = Flip-flop clock-to-out delay.

T_{met} = Additional settling time added to the normal clock-to-out delay of the flip-flop before sampling the output of the flip-flop.

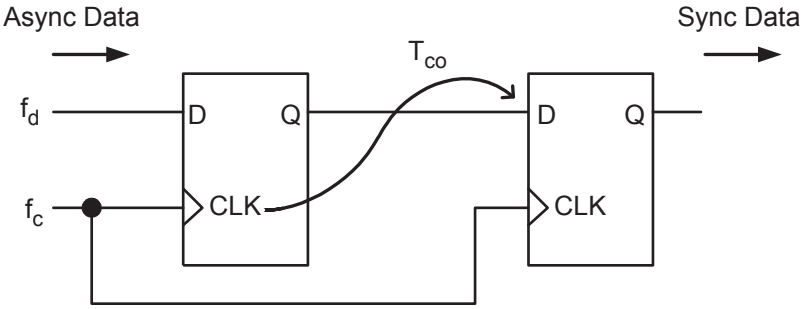
t = Metastable decay constant.

T_0 = Metastability aperture at Tco = 0 ns (This parameter represents the likelihood that a flip-flop will enter a metastable state).

f_d = Data transition rate (Twice the data frequency for periodic signals since there are two transitions per one period).

f_c = Clock frequency

Figure 1 • **Example of Synchronization Circuit**



As mentioned earlier, the aperture represents the likelihood of the flip-flop to enter a metastable state. The aperture is defined as a time window within the clock period. Data transitioning inside the aperture will cause the flip-flop output settling time to be greater than $T_{co} + T_{met}$. The aperture is calculated by recording the number of instances in which the settling time exceeds the specified $T_{co} + T_{met}$. The metastability aperture decreases exponentially as the allowed settling time ($T_{co} + T_{met}$) increases:

$$\text{Aperture} = T_0 \bullet \left(e^{(-((T_{co} + T_{met})/\tau))}\right)$$

EQ3

If the data transition occurs within the aperture, the flip-flop will stay metastable beyond the allocated settling time ($T_{co} + T_{met}$); and therefore, the second flip-flop would register invalid data (Figure 1, page 3). The probability of an asynchronous data transition is uniformly distributed over the clock period. Therefore, the probability of a single data transition occurring in the metastable aperture is calculated by the following:

$$p = (\text{aperture})/T_c$$

EQ4

Where T_c is the clock period.

In each clock cycle, the failure occurs if the data transition time is within the aperture. Therefore, the number of failures in one clock cycle can be derived by the following:

$$n_e = n \cdot p = (n \cdot (\text{aperture})/T_c)$$

EQ5

Where n_e represents the number of errors per clock cycle, and n is the number of data transitions per clock period (f_d / f_c).

The number of clock cycles in the operation time (N) is the total time divided by the clock period or

$$N = T_{operation}/T_c$$

EQ6

Combining EQ5 and EQ6 results in the total number of failures per operation time (N_e):

$$N_e = N \cdot n_e = ((T_{operation} / T_c) \cdot ((f_d / f_c) \cdot ((aperturte) / T_c))$$

EQ7

Since $T_c = 1/f_c$, EQ7 can be simplified to:

$$N_e = T_{operation} \cdot f_d \cdot f_c \cdot aperture$$

EQ8

MTBF is defined as the operation time divided by the number of failures or:

$$MTBF = 1/(f_d \cdot f_c \cdot aperture) = 1/\left(T_0 \cdot e^{(-(T_{co} + T_{met}))/\tau)} \cdot f_d \cdot f_c\right)$$

EQ9

2.2 FPGA Metastability Characterization

Like other FPGA manufacturers, in order to absorb the fixed value of the e^{Tco} term, Microsemi simplifies EQ9 to the following form:

$$MTBF = e^{(C2 \cdot Tmet)} / (C1 \cdot fd \cdot fc)$$

EQ10

Where C2 is a constant inversely proportional to the metastability decay constant, and C1 is the proportionality constant that is similar to aperture.

The FPGA metastability characterization is a series of tests that are conducted in order to identify the value of C1 and C2. There are several environmental and test condition factors that influence the characterization. These factors include but are not limited to the rise time of data and clock signals, input voltage levels and operating voltage and temperature. Moreover, increased system noise due to switching of both internal nodes and I/Os can influence the metastability results. Therefore, it is essential to provide a suitable environment for testing.

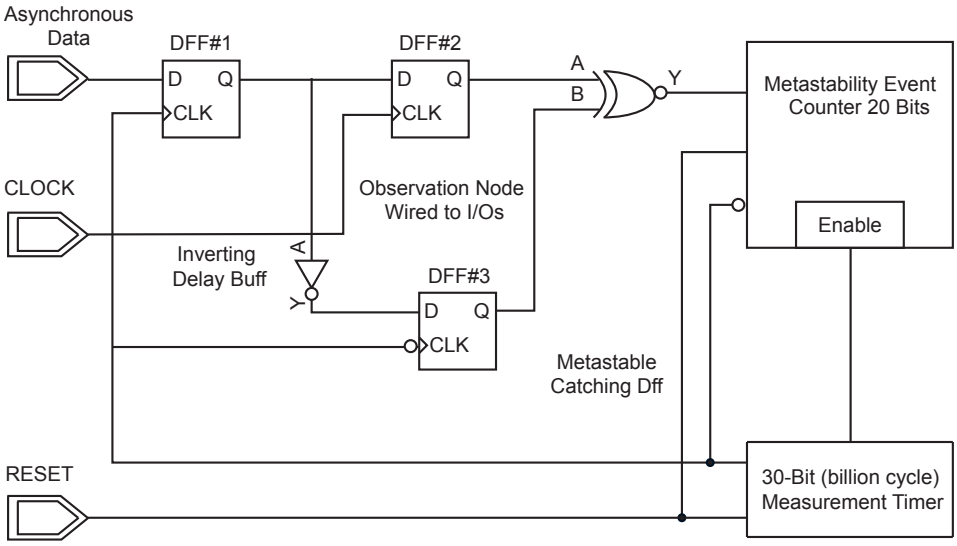
2.3 Test Design Description

Figure 2, page 5 shows a schematic of the test circuit used to characterize the metastability in Microsemi devices. The propagation delay, operating under specified setup and hold time, is measured from the output of flip-flop DFF#1 to the input of flip-flop DFF#3. This value is denoted by:

$$T_{min} = T_{cof} \cdot (DFF1) + T_{delay} + T_{su} \cdot (DFF3)$$

EQ11

Figure 2 • **Test Circuit**



Where T_{delay} is the propagation delay from output of DFF#1 to input of DFF#3, Tcof is the clock-to-out delay of DFF#3 and T_{su} represents the setup time requirement of DFF#3. T_{min} corresponds to the Tco in EQ9, page 4 and is the reference time to which the additional settling time, T_{met}, is added for characterization of metastability.

DFF#2 is clocked on the same edge as DFF#1. Conversely, DFF#3 must resolve the signal driven from the metastable DFF#1 before the falling clock edge. As it can be seen in the design in Figure 2, page 5, T_{min} + T_{met} is the difference between the rising and falling edge of the clock. Therefore, it can be easily set or measured by adjusting the duty cycle of clock signal. A detectable metastable event occurs whenDFF#2 and DFF#3 are in the SAME state. In the expected operation, DFF#2 and DFF#3 are in opposite states due to the inverter in the DFF#3 input data path. The XNOR gate allows the event counter to record these metastable events. After a billion clock cycles, the counter is read and the MTBF is calculated.

In this test, T_{min} was resolved to within ±0.01% of the duty cycle at 10 MHz. This translates to an error of ±10 ps.

The other test setup parameters are as follows:

- Clock and data inputs are driven from independent pulse generators (<1 nS Rise time)
- The clock input levels range from 0V to 2.5V. These levels were required due to impedance matching requirements of our test fixture. Data input is driven from 0V to 2.5V.
- Power supply settings were as follows:
  - VDD at 1.2V
  - VPP at 2.5V
  - VDDI at 2.5V

2.4 Metastability Measurement Results

EQ10 can be reformed into the following:

$$\ln(MTBF) = C2 \cdot T_{met} - \ln(C1 \cdot f_d \cdot f_c)$$

EQ12

The plot of EQ12 is a linear relationship between ln(MTBF) and T_{met} where C2 is the slop of the line. Figure 3, page 6 shows the plot of EQ 12 for Microsemi RTG4 family. C1 and C2 can be calculated from any two data points.

The metastability theory indicates that C1 and C2 are independent of the test clock and data frequency. The test results concur within experimental tolerances. The calculation of C1 and C2 is listed in Table 1, page 6.

Figure 3 • **RTG4 Metastability Plot**

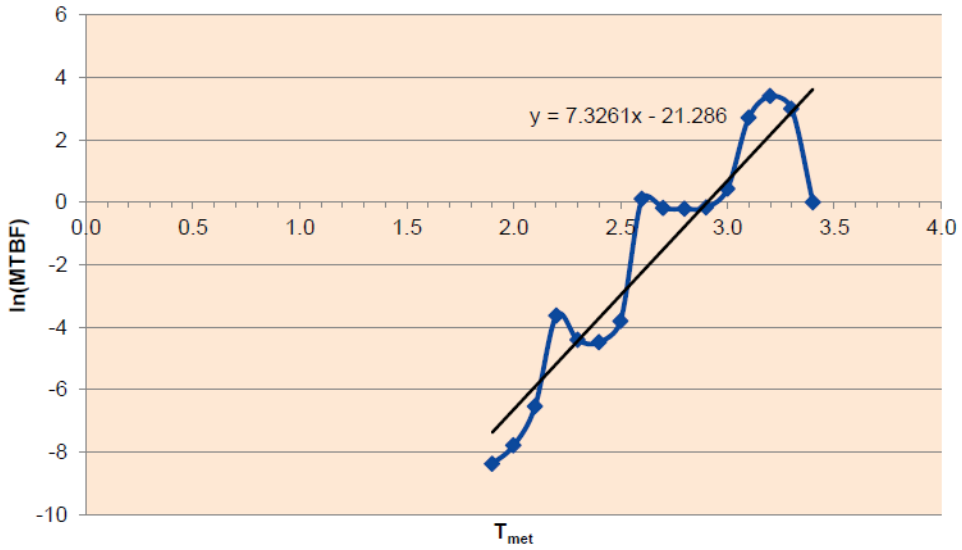


Table 1 • **RTG4 Metastability data**

M	B	C1	C2
7.33	-21.29	2.877E - 05	7.326E + 09

2.5 Examples of Metastability Coefficients Usage

Metastability shows a statistical nature and designers should allow enough additional time (T_{met}), so that the likelihood of metastable failure is remote enough to be tolerable by the design specification.

For example, consider that the simple circuit in Figure 1, page 3 is implemented in a RTG4 device in order to synchronize an asynchronous data input to the FPGA. The following parameters are given to the designer by either design specification or post-layout timing analysis:

Consider a design which uses a system clock rate (f_c) of 100 MHz to capture the asynchronous events.

Asynchronous data transition rate = 12.5 MHz

Tolerable MTBF = 20 years

If the designer does not allow additional sampling time (T_{met} = 0) and runs the clock at the rate of 100 MHz, EQ12, page 5 results in MTBF = 27.81 ps. This means that a metastability error will occur at the output of the second flip-flop every 27.81 ps. This value exceeds the required MTBF of 20 years indicated in the design specification. In order to meet this requirement, the designer must allow additional T_{met} in the settling time, which can be calculated as follows:

20 years = 20 * 365 * 24* 3600 = 630,720,000 seconds

$\ln(630{,}720{,}000) = 7.326E{+}09 * T_{met} - \ln(2.877E{-}05 * 100E6 * 12.5E6) \geq T_{met} = 6.08$ ns

Therefore, an additional 6.08 ns settling time will fulfill the required MTBF.

Per *DS0131: RTG4 FPGA Datasheet*, when using the SET filter on the fabric flip-flops (FF), the worst-case clock-to-Q, T_{CLKQ} is 0.243 ns and the worst-case data setup time, T_{SUD} is 1.3 ns. For the 2-FF synchronizer circuit shown in Figure 1, page 3, assume the worst-case $T_{co} = T_{CLKQ} + T_{SUD}$ = 1.543 ns with SET filter enabled. Without SET filter enabled, the worst-case T_{SUD} is 0.505 ns, implying a T_{co} = 0.748 ns.

This implies that the circuit in Figure 1, page 3 has a max achievable settling time equal to T_c (clock period) - T_{co}. With SET filter enabled, the max T_{met} achievable is 10 ns - 1.543 ns = 8.45 ns. Without SET filter enabled, the max T_{met} achievable is 10 ns - 0.748 ns = 9.25 ns.

Therefore, the 2-FF synchronizer shown in Figure 1, page 3 should be suitable to meet the required 6.08 ns of additional settling time required in this design example.

As another example, consider if the clock rate used in the example above was increased to 160 MHz.

The T_{met} can be calculated as follows:

ln(630,720,000) = 7.326E+09 * T_{met} - ln(2.877E-05 * 160E6 * 12.5E6)

Solving for T_{met} results in T_{met} = 6.15 ns

Therefore, with f_c = 160 MHz, an additional 6.15 ns of settling time will fulfill the required MTBF.

However, for the 2-FF synchronizer circuit in Figure 1, page 3, the max achievable settling time depends on the clock frequency. The max T_{met} achievable at 160 MHz is:

With SET filter: Max T_{met} = 6.25 ns - 1.543 ns = 4.70 ns

Without SET filter: Max T_{met} = 6.25 ns - 0.748 ns = 5.50 ns

The designer must consider that the 2-FF synchronizer circuit shown in Figure 1, page 3 would not allow sufficient settling time to reliably capture the asynchronous input signal. A 3rd FF stage could be added to the synchronizer to allow additional settling time before the asynchronous signal is sampled by the rest of the user design. To generalize for RTG4, when the design clock frequency exceeds 125 MHz, it is recommended to increase the number of synchronizer flip-flops used beyond the typical 2-FF design used in Figure 1, page 3.

In general, another point to consider is the total number of such synchronizer circuits used in the design.The overall MTBF of the entire design decreases as the number of these synchronizer circuits used increases. For example, if a 20 year MTBF is used in the calculations above for 1 synchronizer instance, then a 200 year MTBF can be used for a design containing 10 such synchronizer instances.