TR0043

Test Report

PolarFire Neutron Test Results

June 2018

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in June 2018. It was the first publication of this document.

2 Testing Conditions

The first phase of neutron testing was performed on Microsemi's new PolarFire® family of devices (G5) MPF300XT. The main objective was to test the product for latch-up behavior as well as to get soft error data on the fabric.

2.1 Sample Preparation

Five devices were irradiated during the test. The samples were prepared by removing packaging material to expose the dice. Resistive heaters were placed on the parts to heat the devices. Maximum achievable temperature was approximately 80 °C.

The following table shows the testing configuration of PolarFire devices.

Table 1 • Testing Configuration

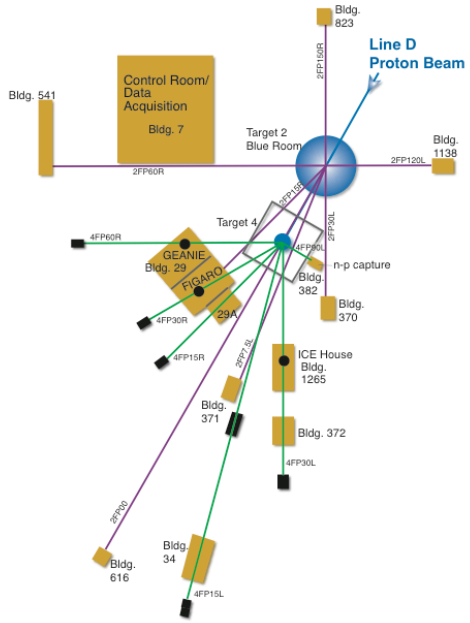
Part Serial Number	Revision	Patch	Board	Focus
81	D+	Proton latest	Daughterboard and motherboard	Soft error and latch-up
82	D+	Proton latest	Daughterboard and motherboard	Soft error and latch-up
87	D+	Avionics	TID	Latch-up
88	D+	Avionics	Daughterboard	Latch-up
89	D+	Avionics	Daughterboard	Latch-up

2.2 Beam

Los Alamos Weapons Neutron Research target Irradiation of Chips Electronics house was used for this experiment. The fluence was calculated based on neutron energies > 10 MeV. The flight path length is approximately 20 m from the source to the fission chamber.

The following figure shows the flight path setup at Los Alamos Neutron Science Center (LANSCE).

Figure 1 • Flight Paths at LANSCE



2.2.1 Voltage Bias and Temperature

The five boards were placed one behind the other. Four of the boards ran at higher voltage biases to run worst case conditions for latch-up (based on the recommended maximum operating conditions taken from the PolarFire FPGA data sheet). For soft errors, the devices were run at nominal voltage biases. The biases recorded are provided in the following table.

Table 2 • Voltage Configurations

Channel	Bias 1 – Nominal (Soft Errors)	Bias 2 -Maximum Recommended Operating Conditions (Latch-Up)
1	1.05	1.08
2	1.8	1.89
3	2.5	2.575
4	3.3	3.465

The following table outlines the power domain connections to the respective channels during the test setup.

Table 3 • Power Domain Configuration

Channel	DUT Power Domain
1	VDD and VDDA
2	VDD18, VDDI0, VDDI1, VDDI6, and VDDI7
3	VDD25, VDDA25, and VDDSREF
4	VDDI3, VDDI2, VDDI4, VDDI5, VDDAUX2, VDDAUX4, and VDDAUX5

Four boards were run at temperature range between 30 °C to 80 °C. The reason for the change in temperature range is due to burning heaters and changes made during the test to accommodate for the heater damage.

Note: The entire test was performed with the device in non avionics mode (System Controller Active).

2.3 Testing Procedure

The following steps detail the testing procedure.

1. Program device under test (DUT) and master chips with respective designs and verify the functionality.
2. Place resistive heaters and sensors on the DUTs. Ramp-up the temperature slowly (takes about 20 minutes or more to achieve 85 °C to 90 °C, depending on the design, heaters, and environment). Ramping up too quickly results in burning of heaters.
3. Align the boards to the beam path. Ensure there is no tilting (that is boards are perpendicular to the beam).
4. Ensure once again that all boards are functioning for soft errors, and all powers are being monitored and have values as expected.
5. Open shutter to start beam.
6. Monitor the results.
7. In case of latch-up, stop beam, record soft errors, and fluence at which the beam was stopped/latch-up occurred. Perform a power down and up sequence, to see if the current returns back to its nominal operating point.
8. Irradiate parts for maximum fluence.

3 Latch-Up Analysis

This section provides the details of the latch-up analysis.

There were no observable latch-up events for the entirety of this test.

The following table provides the latch-up summary.

Table 4 • Latch-Up Summary

Temp + Bias	Total	~80°C + High bias	~50°C + High Bias	Room Temp + High Bias	Room Temp + Nominal Bias
XS	< 8.64857E–13	< 3.23501E–12	< 2.1446E–12	< 6.94532E–12	< 4.22169E–12
FIT/Device [NYC]	< 0.01	< 0.04	< 0.03	< 0.09	< 0.05
Fluence Tested [n/cm^2]	1.16E+12	3.09E+11	4.66E+11	1.44E+11	2.37E+11

See the following current vs. time graphs. The set-up powers are as follows.

Device 1 – Setup 1 focuses on soft errors powered at nominal bias and room temperature.

Device 2 – Setup 2 focuses on soft errors and latch-up powered at recommended max operating bias and high temperature.

Device 3 – TID board and two latch-up boards are chained together, powered at recommended maximum operating bias and high temperature.

3.1 Run 1

This was the first run for the test campaign. There was no unusual current behavior. The initial ramp on the device 2 and the device 3 is due to the ramping in temperature while collecting data to save time. During the ramping period, the temperature on boards 2,3,4, and 5 is increased from 30 °C to approximately 50 °C. The following illustrations are current plots of all the devices during run 1.

Figure 2 • Run 1 Device 1

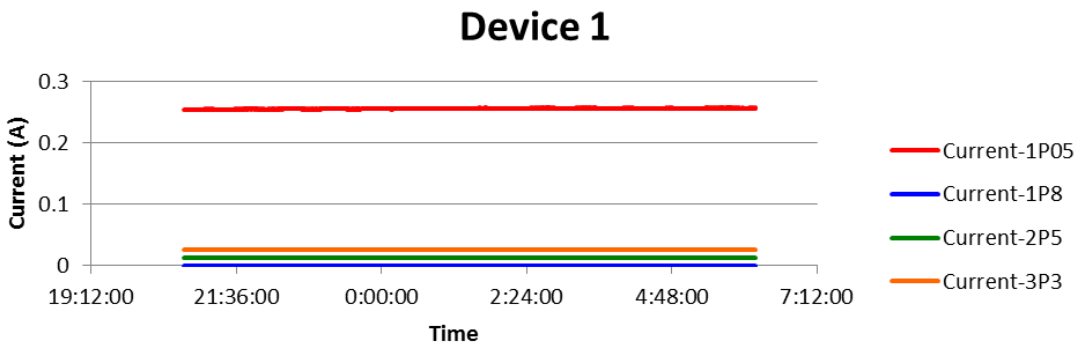


Figure 3 • Run 1 Device 2

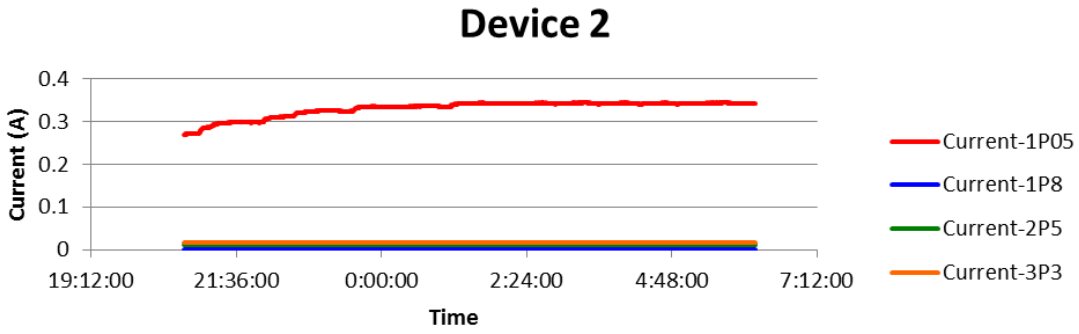
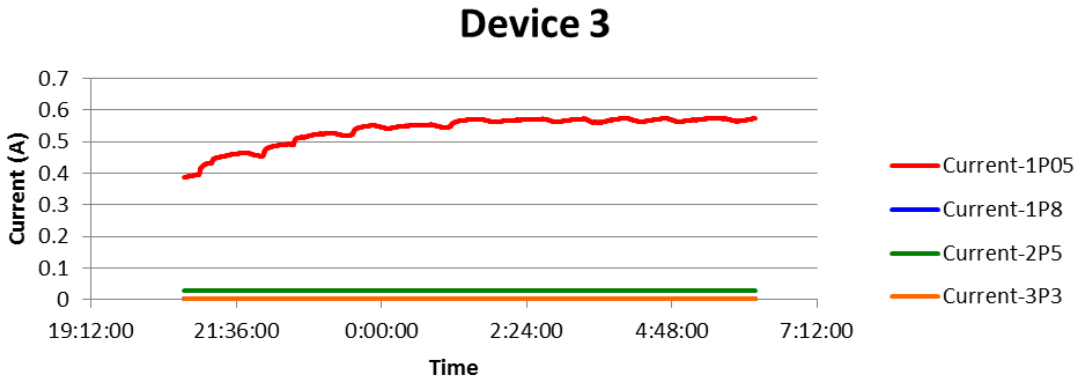


Figure 4 • Run 1 Device 3



3.2 Run 2

During this run, the temperatures were relatively stable. A minor oscillation in current was observed due to turn on and turn off of the ambient room heating.

The following illustrations are current plots of all the devices during run 2.

Figure 5 • Run 2 Device 1

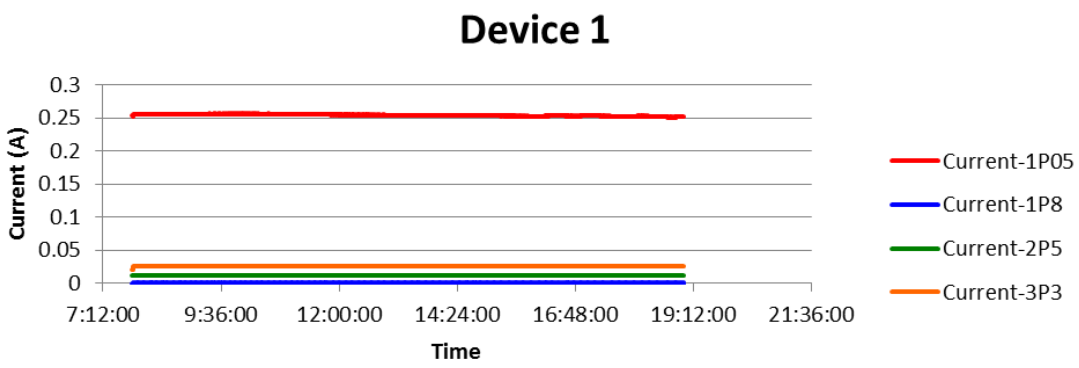


Figure 6 • Run 2 Device 2

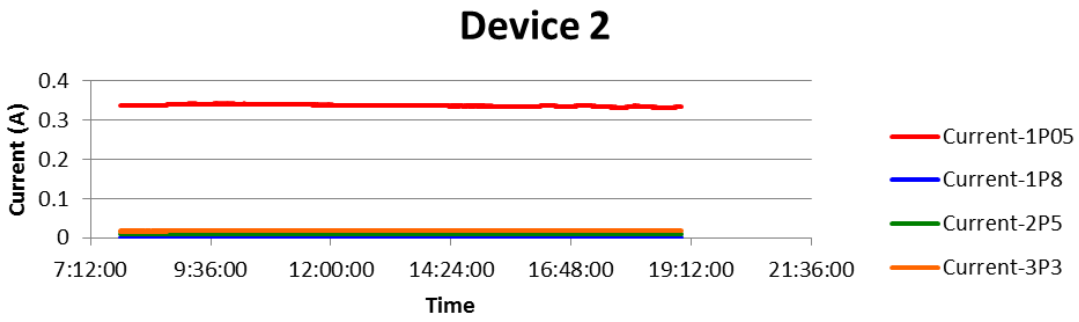
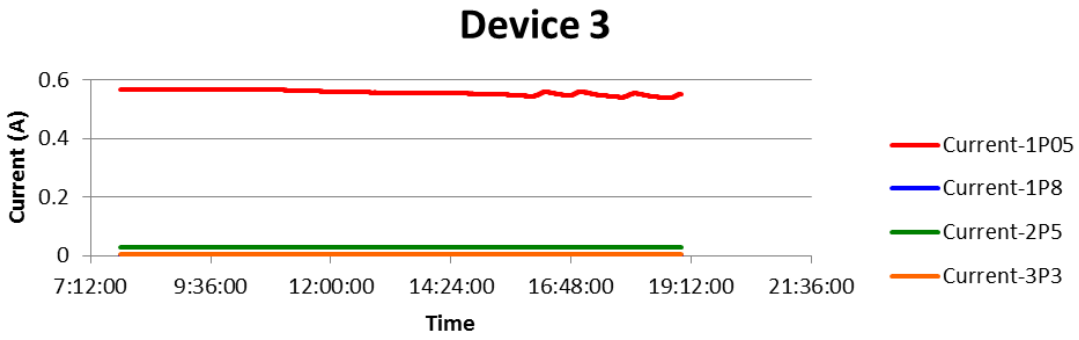


Figure 7 • Run 2 Device 3



3.3 Run 3

It is observed that the apparent oscillation in current on the device 2 and the device 3 occurs primarily overnight due to the heating system in the most active building. There are no other significant observations during this run.

The following illustrations are current plots of all the devices during run 3.

Figure 8 • Run 3 Device 1

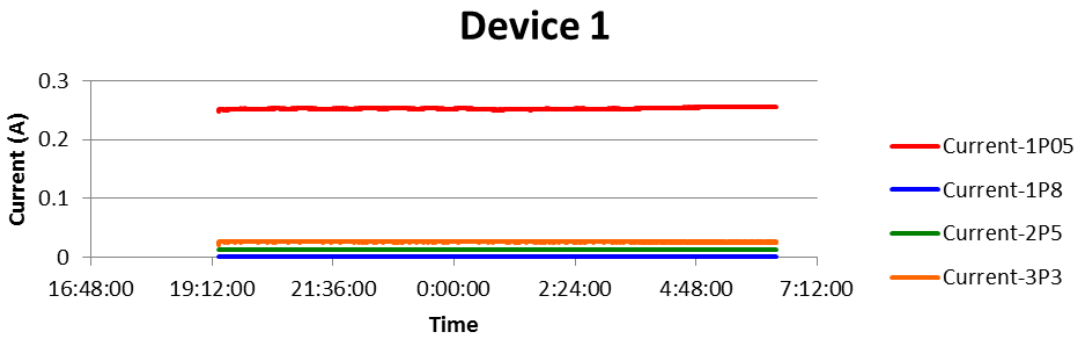


Figure 9 • Run 3 Device 2

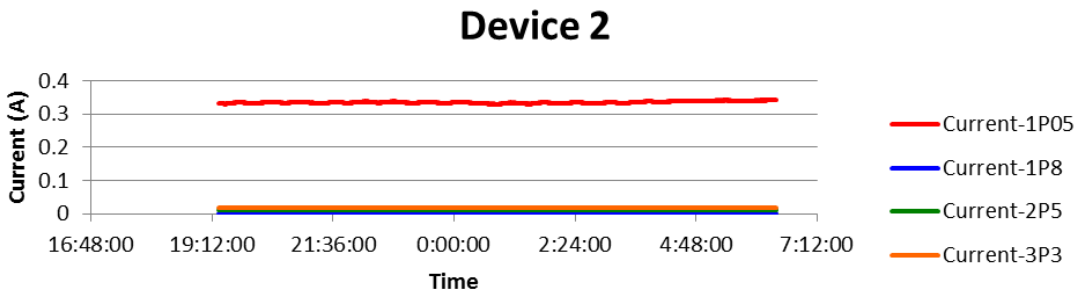
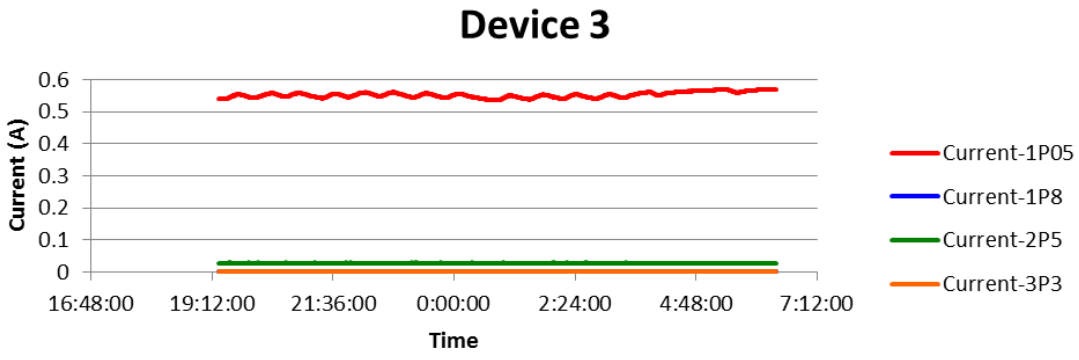


Figure 10 • Run 3 Device 3



3.4 Run 4

Towards the end of this run, a small modification had to be made and temperature was turned off. As a result there is a current drop on the device 2 and 3 around the same time. The heater wires were stripped, and replaced with banana cables, to reduce resistance, therefore increasing the current flow to achieve a higher temperature.

The following illustrations are current plots of all the devices during run 4.

Figure 11 • Run 4 Device 1

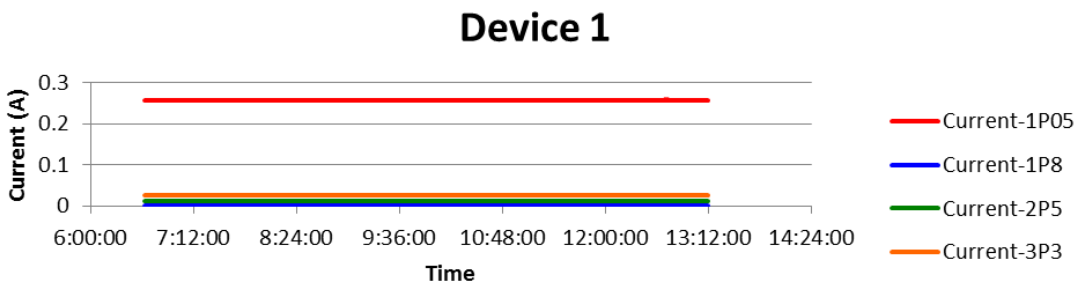


Figure 12 • Run 4 Device 2

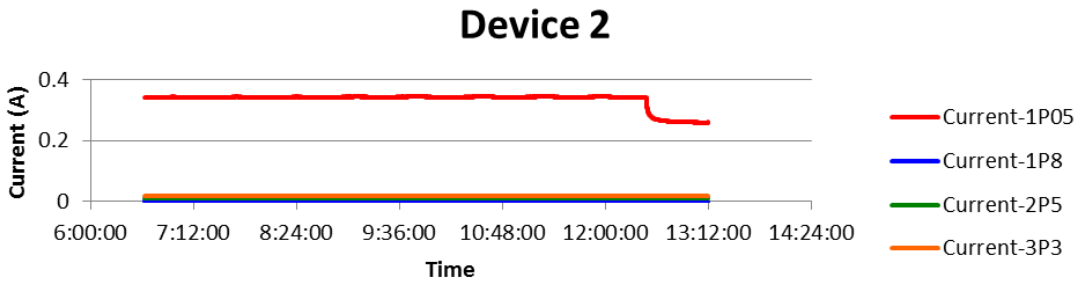
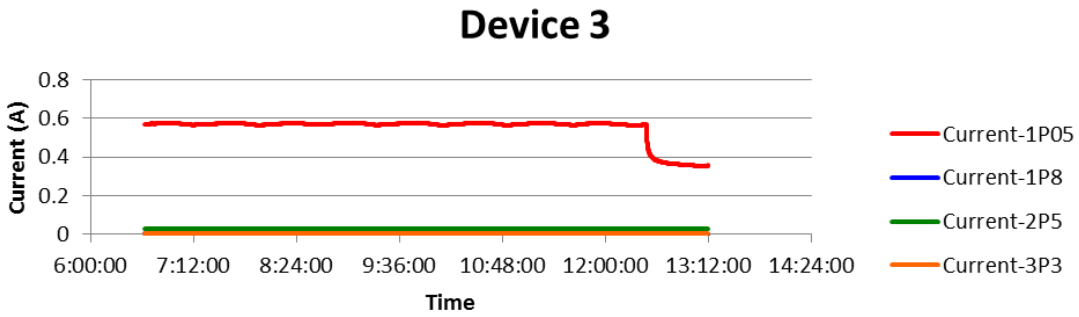


Figure 13 • Run 4 Device 3



3.5 Run 5

After making the modifications, heat was ramped up and a rise in current was observed.

The following illustrations are current plots of all the devices during run 5.

Figure 14 • Run 5 Device 1

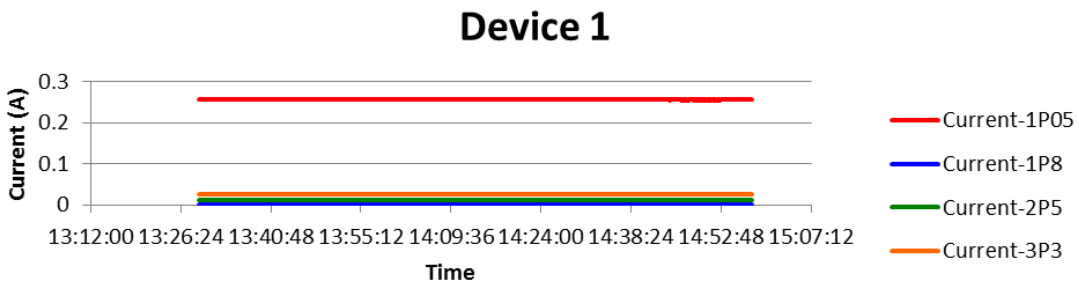


Figure 15 • Run 5 Device 2

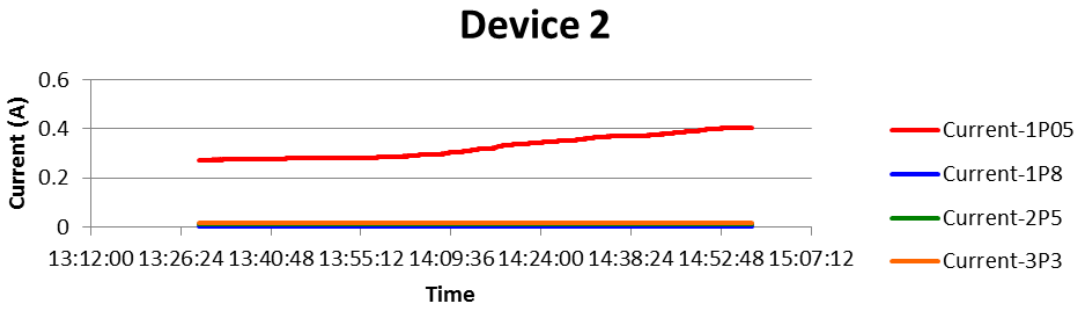
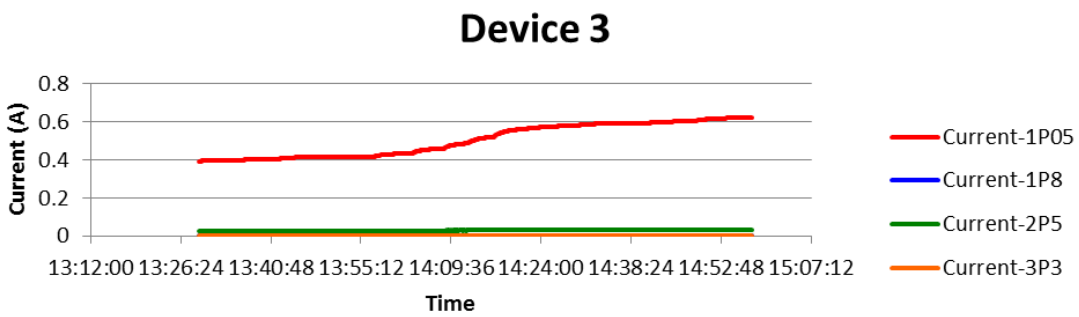


Figure 16 • Run 5 Device 3



3.6 Run 6

During this run, the heat was ramped up to approximately 95 °C on board 2 and 90 °C on boards 3, 4, and 5. The heater on board 2 burned out, and as a result, sharp current drop was observed on the device 2. To prevent this from happening on the other heaters, the temperature was ramped-down to approximately 80 °C on boards 3, 4, and 5.

The following illustrations are current plots of all the devices during run 6.

Figure 17 • Run 6 Device 1

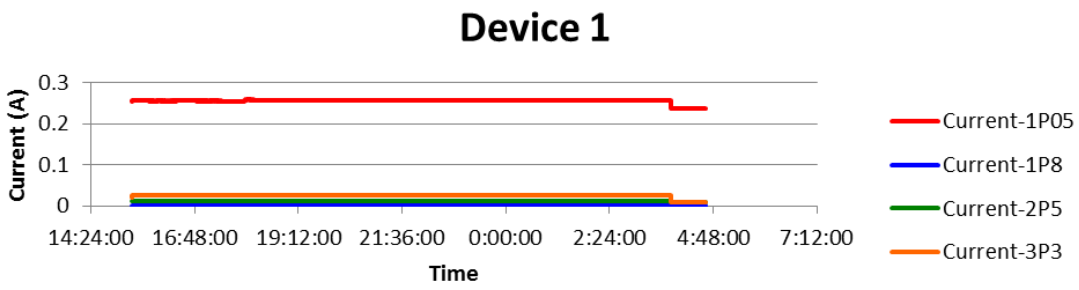


Figure 18 • Run 6 Device 2

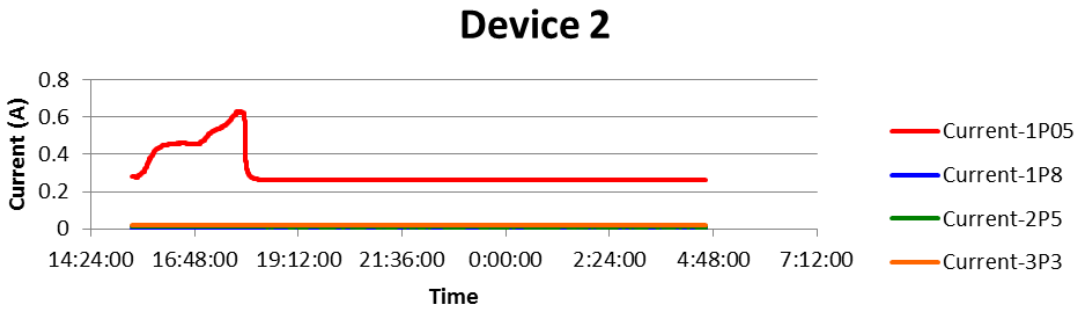
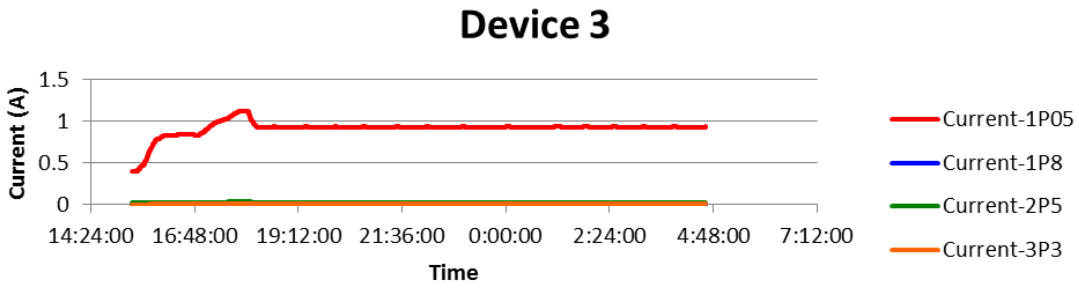


Figure 19 • Run 6 Device 3



3.7 Run 7

Towards the end of the run, the heater on the board 4 burned out resulting in a current drop.

The following illustrations are current plots of all the devices during run 7.

Figure 20 • Run 7 Device 1

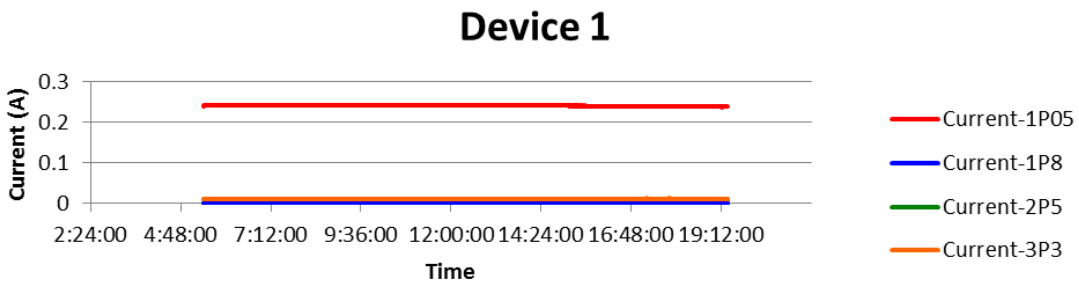


Figure 21 • Run 7 Device 2

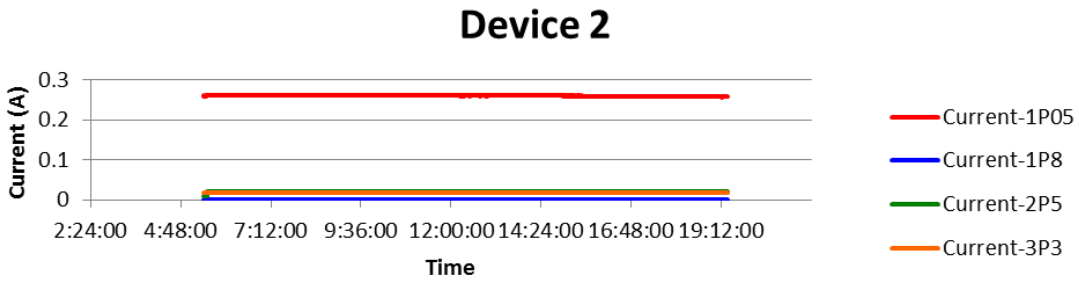
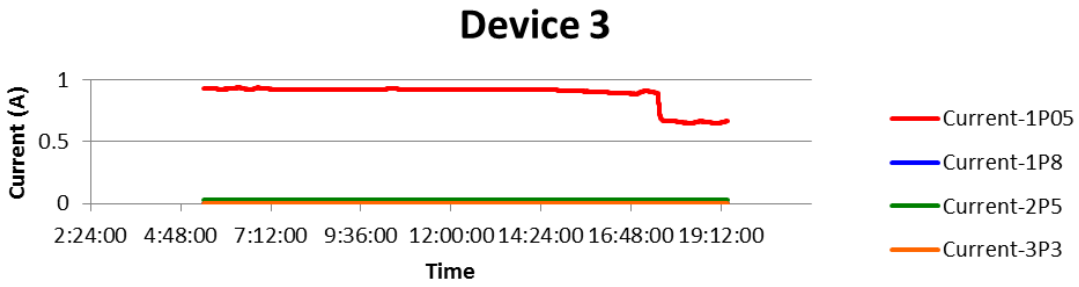


Figure 22 • Run 7 Device 3



3.8 Run 8

This was a relatively short run. It was stopped due to occurrance of a reset. Since it was the first reset observed during the test, it was restarted.

The following illustrations are current plots of all the devices during run 8.

Figure 23 • Run 8 Device 1

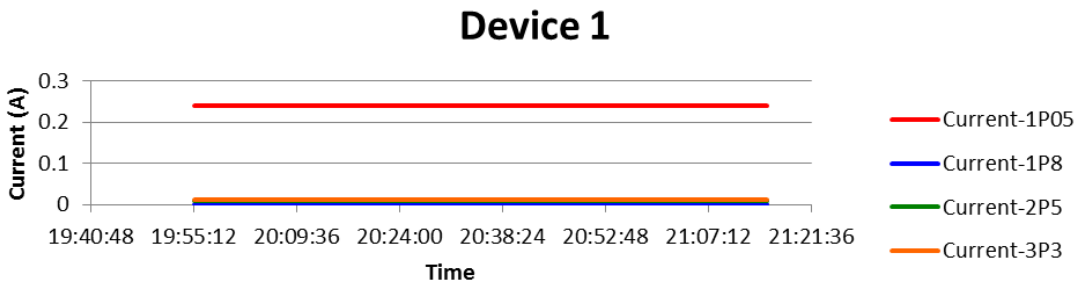


Figure 24 • Run 8 Device 2

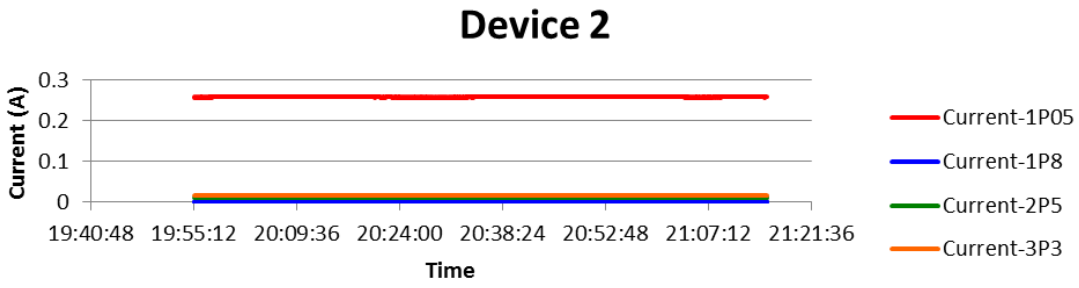
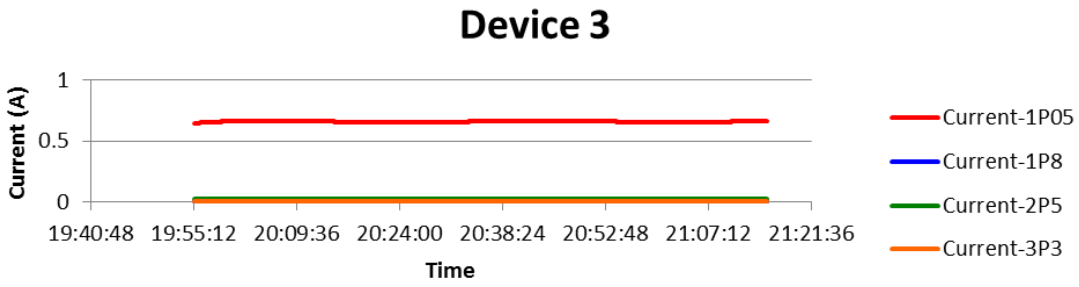


Figure 25 • Run 8 Device 3



3.9 Run 9

This was the last run for the test. A minor noise was noticed on channel 4 of device 1. The current clamp was then increased on the master power supply to be safe. After this modification, the behavior mentioned above was not observed. Therefore, that event can be ignored.

The following illustrations are current plots of all the devices during run 9.

Figure 26 • Run 9 Device 1

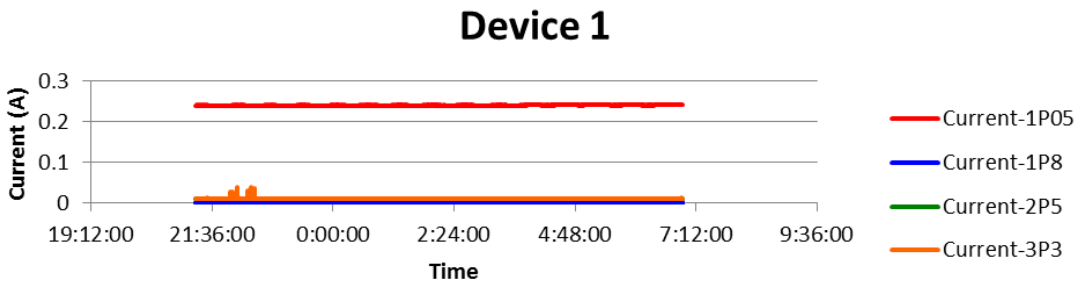


Figure 27 • Run 9 Device 2

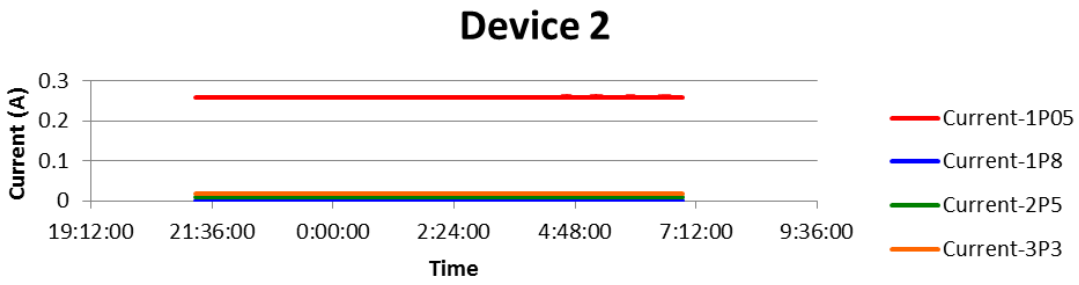
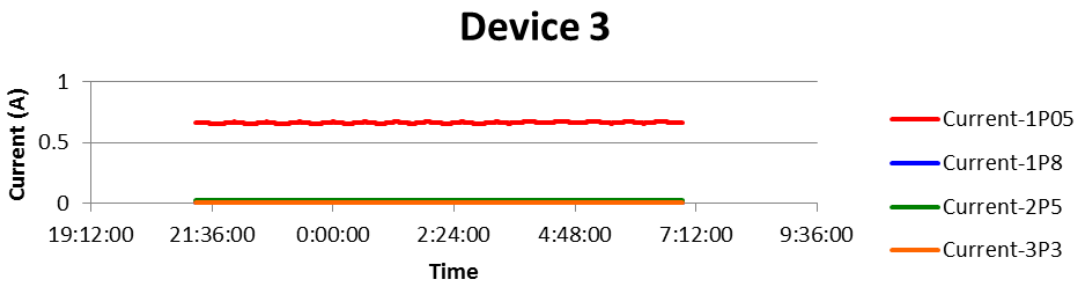


Figure 28 • Run 9 Device 3



4 Fabric Soft Error Designs

Soft error data was collected on flip flops, uSRAM, LSRAM, and math blocks. The following is a brief description of the designs used to obtain preliminary data on each respective block.

4.1 Flip Flop Design

Four shift register chains with 4000 stages in each chain are used. The output is compared to a golden functional model on the master G3 chip. This ensures a bit by bit comparison of the return data with the expected data.

Each flip flop chain uses a different data input pattern to identify potential differences.

Chain 1 — input 0 with toggling clock at 10 MHz
Chain 2 — input 1 with toggling clock at 10 MHz
Chain 3 — input checkerboard with clock at 10 MHz
Chain 4 — slowed down checkerboard with clock at 10 MHz

4.2 LSRAM Design

69 Large SRAM blocks were instantiated, 64 words × 18 bits is the length of each word. The RAM driver writes the value of the address to each address it accesses (fill state). Following the fill state, the RAM FSM on the master reads the data continuously, and compare it to a model on the master (expected data) to identify if there were any errors. If an error is detected, a flag is raised and following the read of the entire memory, the FSM rewrites the memory so that the error is corrected and not counted twice. This is a legacy algorithm that has been used for testing other Microsemi FPGAs including G4 and RTG4. The algorithm completely rewrites both the LSRAM and uSRAM simultaneously.

4.3 uSRAM Design

69 micro SRAM blocks were instantiated, 64 words × 12 bits is the length of each word. The RAM driver writes the value of the address to each address it accesses (fill state). Following the fill state, the RAM FSM on the master reads the data continuously, and compare it to a model on the master (expected data) to identify if there were any errors. If an error is detected, a flag is raised and following the read of the entire memory, the FSM rewrites the memory so that the error is corrected and not counted twice. This is a legacy algorithm that has been used for G4 and RTG4 testing. The algorithm completely rewrites both the LSRAM and uSRAM simultaneously.

4.4 Math Block Design

The design has two parallel math block chains with fixed coefficients A and B, and C is equal to the input of the previous stage. The input C to the first math block is a simple counter that is fed into both chains simultaneously. The output at the last stage of the math blocks is then compared with each other to identify an upset. 10 stages of math blocks were used in each chain performing the operation
P = A*B + C.

5 Soft Error Summary

This section provides the details on the soft error summary.

The following table provides the failures-in-time (FIT) rate summary for PolarFire fabric blocks.

Table 5 • FIT Rate Summary

	Neutron Combined B1 + B2 FIT/Mb [NYC - Sea]	Neutron Nominal Bias B1 FIT/Mb [NYC - Sea]	Neutron High bias and temperature B2 FIT/Mb [NYC - Sea]
FF All 0s	101.369	129.4827328	72.8849698
FF All 1s	130.332	143.8697031	116.6159517
FF Checkerboard	398.237	460.3830498	335.2708611
FF Checkerboard Slow	217.22	230.1915249	204.0779154
LSRAM	209.51	216.470618	202.4582494
uSRAM	134.45	149.864274	118.8341899
Math Blocks	Further analysis required[1]	Further analysis required	Further analysis required
Fluence Tested [n/cm^2]	4.71E+11	2.37E+11	2.34E+11

The following table provides the cross section summary details for PolarFire fabric blocks.

Table 6 • Cross Section Summary

	Neutron Combined B1 + B2 XS/bit	Neutron Nominal Bias B1 XS/bit	Neutron High bias and temperature B2 XS /bit
FF All 0s	7.44E-15	9.50E-15	5.35E-15
FF All 1s	9.56E-15	1.06E-14	8.56E-15
FF Checkerboard	2.92E-14	3.38E-14	2.46E-14
FF Checkerboard Slow	1.59E-14	1.69E-14	1.50E-14
LSRAM	1.54E-14	1.59E-14	1.49E-14
uSRAM	9.86E-15	1.10E-14	8.72E-15
Math Blocks	Further analysis required[1]	Further analysis required	Further analysis required
Fluence Tested [n/cm^2]	4.71E+11	2.37E+11	2.34E+11

Note:

1. Incorrect counting of math block errors occurred. Further analysis of the design and heavy ion testing is required to validate these observations.
   All 0 s and all 1 s flip-flop (FF) data patterns are insensitive to clock glitches. The contribution of clock glitches in the checkerboard and checkerboard slow data patterns explains the different error rates calculated for the respective patterns.

The following table provides the FIT rate adjusted for nyc 40k ft and north pole 50k ft.

Table 7 • FIT Rate

Block	FIT/Mb [NYC - Sea]	FIT/Mb [NYC – 40k ft]	FIT/Mb [North Pole – 50k ft]
FF All 0 s	101.369	52253.69	100956.43
FF All 1 s	130.332	67183.54	129801.55
FF Checkerboard	398.237	205281.66	396616.17
FF Checkerboard slow	217.22	111972.56	216335.91
LSRAM	209.51	107998.21	208657.29
uSRAM	134.45	69306.29	133902.78

FIT rate is calculated using the formula as provided in the following table.

Table 8 • Formulae for FIT Rate Calculations

Formulae	σ(PerBit) = Total Bit Upsets/Fluence/Total Num Bits
	σ(Mb) = σ(PerBit) * 2 ^ 20 bits
	FIT/Mb[NYC] = σ(Mb) * f(NYC) * 10^9 (errors per 10^9 hour), where f(NYC) = 13 n/cm^2/hour
	FIT/Mb[NYC-40k ft] = FIT/Mb[NYC] *515.48
	FIT/Mb[North Pole- 50k ft] = FIT/Mb[NYC]*995.93

Fluence adjustment is based on the geometry of the beam path to account for the change in flux as a function of distance. As confirmed by the instrument scientist at the LANL facility, the distance from the source to the fission chamber is 20 m. The ratio of beam intensity is therefore, [(20m)/(20m+R)]^2, where R is the distance measured from the fission chamber to the respective boards.

6 SEFI Summary

This section describes the single event functional interrupt (SEFI) summary.

The following table provides the SEFI FIT rate summary.

Table 9 • SEFI FIT Rate Summary

	Neutron Combined B1 + B2 FIT/Chip – [NYC]	Neutron Nominal Bias B1 FIT/Chip – [NYC]	Neutron High Bias and Temperature B2 FIT/Chip – [NYC]
Chip Reset FIT/Chip[1] [NYC - Sea]	0.055	0.109	< 0.0556
PLL FIT/Chip[2] [NYC- Sea]	< 0.221	< 0.439	< 0.448
Fluence Tested [n/cm^2]	4.71E+11	2.37E+11	2.34E+11

Notes:

1. Chip reset is assumed as a single block.
2. PLL FIT rate upper bound is calculated with an assumption that the chip has eight PLLs.

The following table provides the formulae to calculate SEFI FIT rate summary.

Table 10 • Formulae to Calculate SEFI FIT Rate Summary

Formulae	σ(block) = Total Upsets/Fluence /Total blocks used
	FIT/Chip[NYC] = σ(Chip) * #of blocks on device * f(NYC) * 10^9 (errors per 10^9 hour), where f(NYC) = 13 n /cm^2/hour
	FIT/Mb[NYC-40k ft] = FIT/Mb[NYC] *515.48

In this test, only two events of resets are recorded. Since the fluence is relatively low, more data needs to be collected, to make the preceding claims more substantial.

7 Conclusion

There were no instances of latch-up (SEL) observed for a total fluence of 1.15626E+12 across varying biases (see Latch-Up Summary (see page 4)). Cross sections and equivalent FIT rates were obtained for the flip flops, LSRAM, and uSRAM blocks on Microsemi's Polarfire FPGA which are reported in FIT Rate Summary (see page 15), Cross Section Summary (see page 15), and FIT Rate (see page 15). Additional testing will be performed in the future to test the math blocks. There was no loss of functionality on the PLL block, and a chip level reset with a FIT rate < 1 was observed, as shown in SEFI FIT Rate Summary (see page 17).

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