Total Ionizing Dose Test Report

No. 18T-RT4G150-LG1657-K61F4

May 22, 2018

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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 1. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K61F4
Quantity Tested	5
Serial Number (Dose)	18013 (125 krad), 18018 (125 krad), 18031 (125 krad), 18033 (125 krad), 18038 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

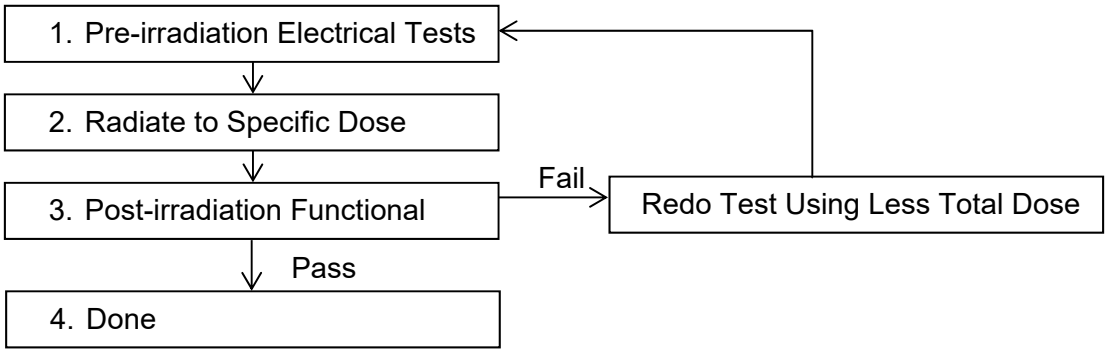

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 2. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 3. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
18013	125 krad	0.3870	0.4075	5.30
18018	125 krad	0.4215	0.4350	3.20
18031	125 krad	0.3870	0.4155	7.36
18033	125 krad	0.4298	0.4488	4.42
18038	125 krad	0.3916	0.4158	6.18

Table. 4. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
18013	125 krad	0.0098	0.0121	23.47
18018	125 krad	0.0095	0.0118	24.21
18031	125 krad	0.0105	0.0128	21.90
18033	125 krad	0.0108	0.0133	23.15
18038	125 krad	0.0105	0.0128	21.90

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
18013	125 krad	0.0340	0.0367	7.94
18018	125 krad	0.0337	0.0364	8.01
18031	125 krad	0.0345	0.0376	8.99
18033	125 krad	0.0346	0.0375	8.38
18038	125 krad	0.0340	0.0372	9.41

Table. 6. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
18013	125 krad	0.0154	0.0178	15.58
18018	125 krad	0.0152	0.0160	5.26
18031	125 krad	0.0154	0.0179	16.23
18033	125 krad	0.0153	0.0162	5.88
18038	125 krad	0.0153	0.0163	6.54

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

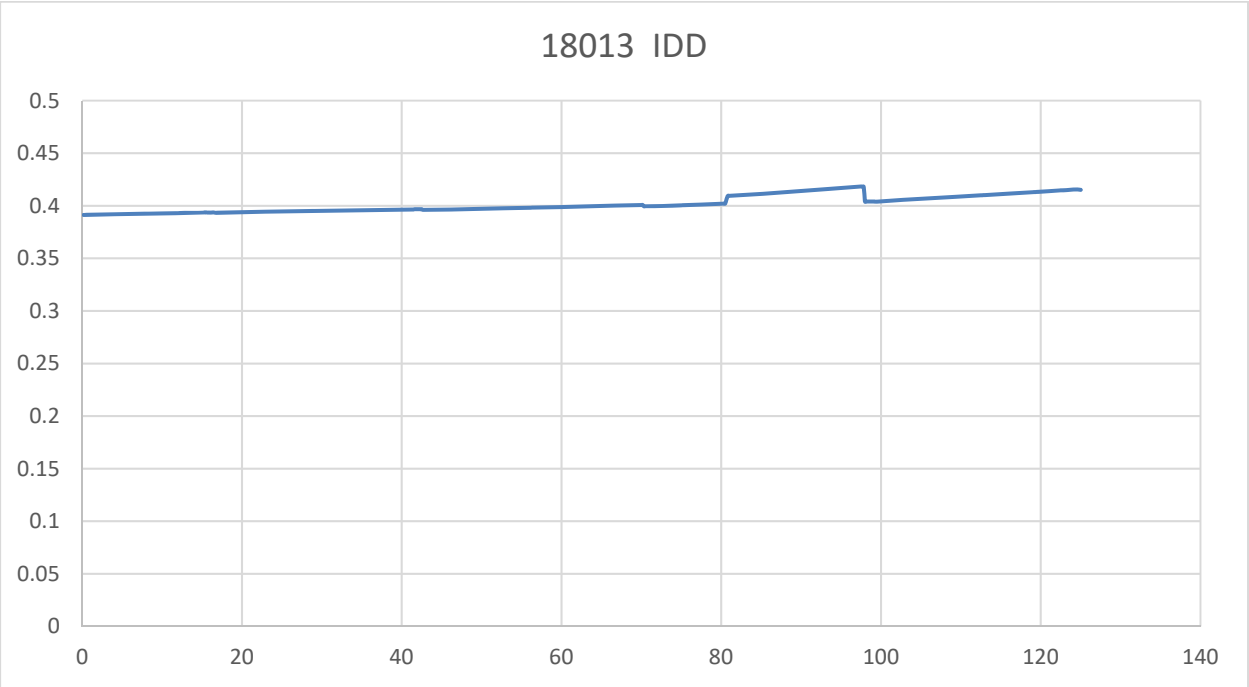

Fig. 2. DUT 18013 core power supply current (I_{DD}) versus TID

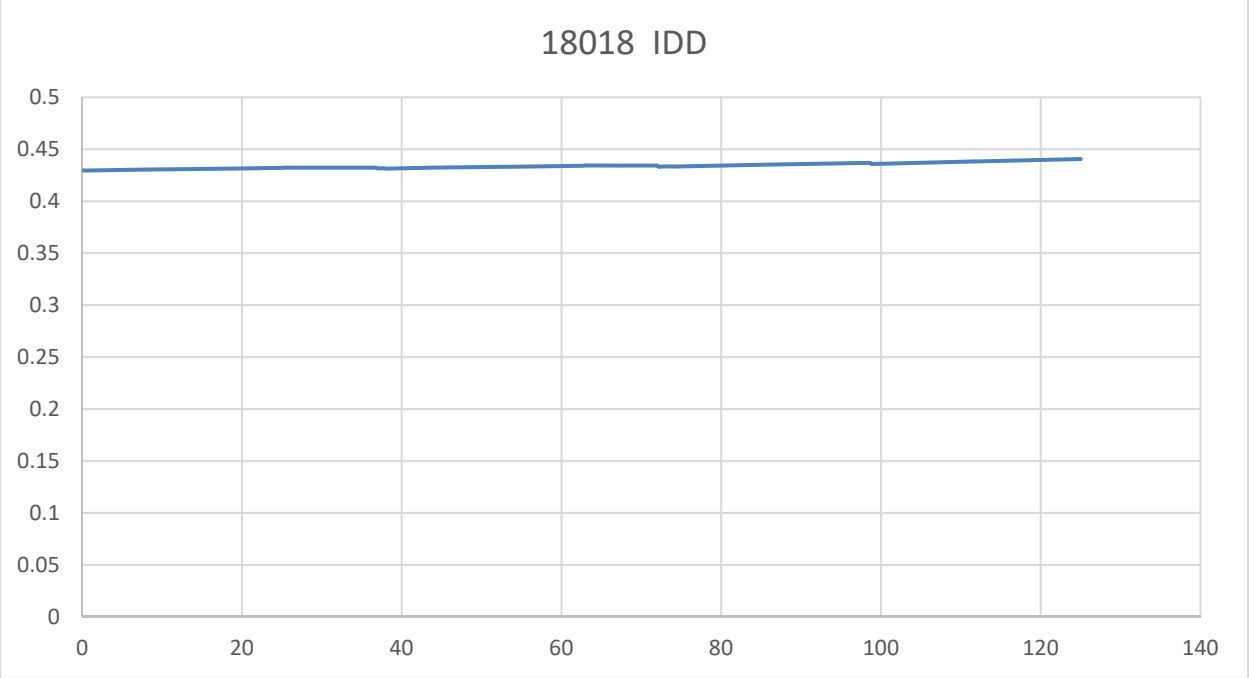

Fig. 4. DUT 18018 core power supply current (I_{DD}) versus TID

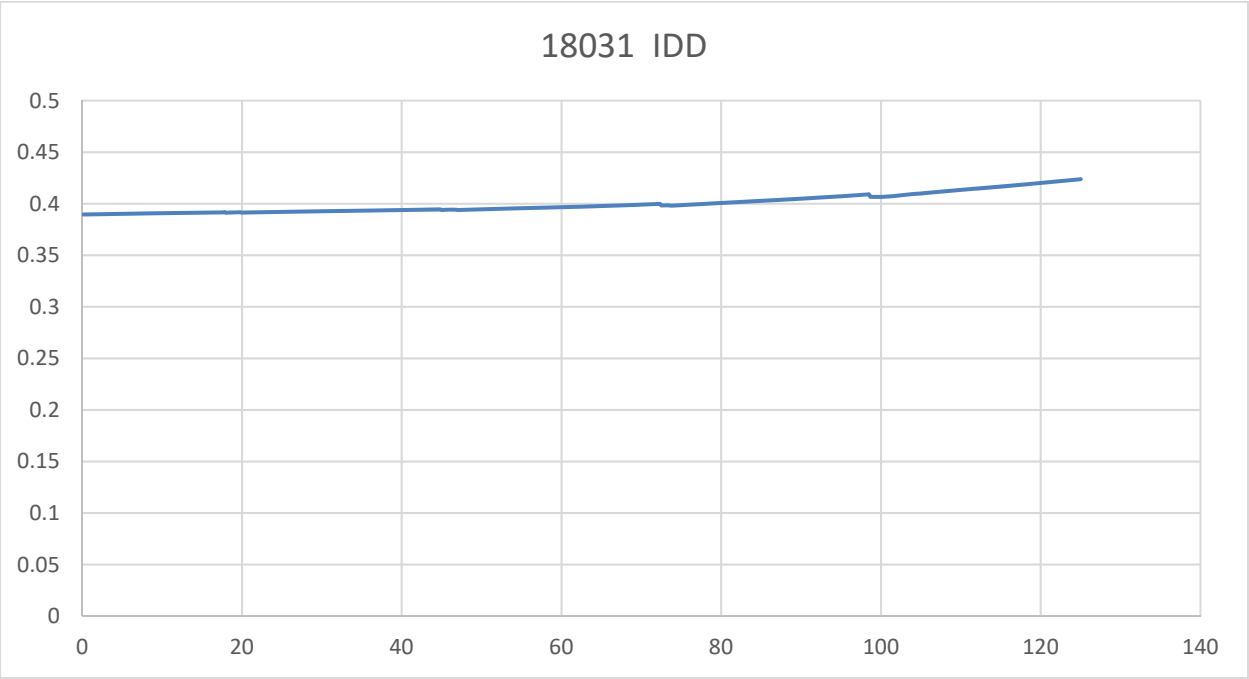

Fig. 5. DUT 18031 core power supply current (I_{DD}) versus TID

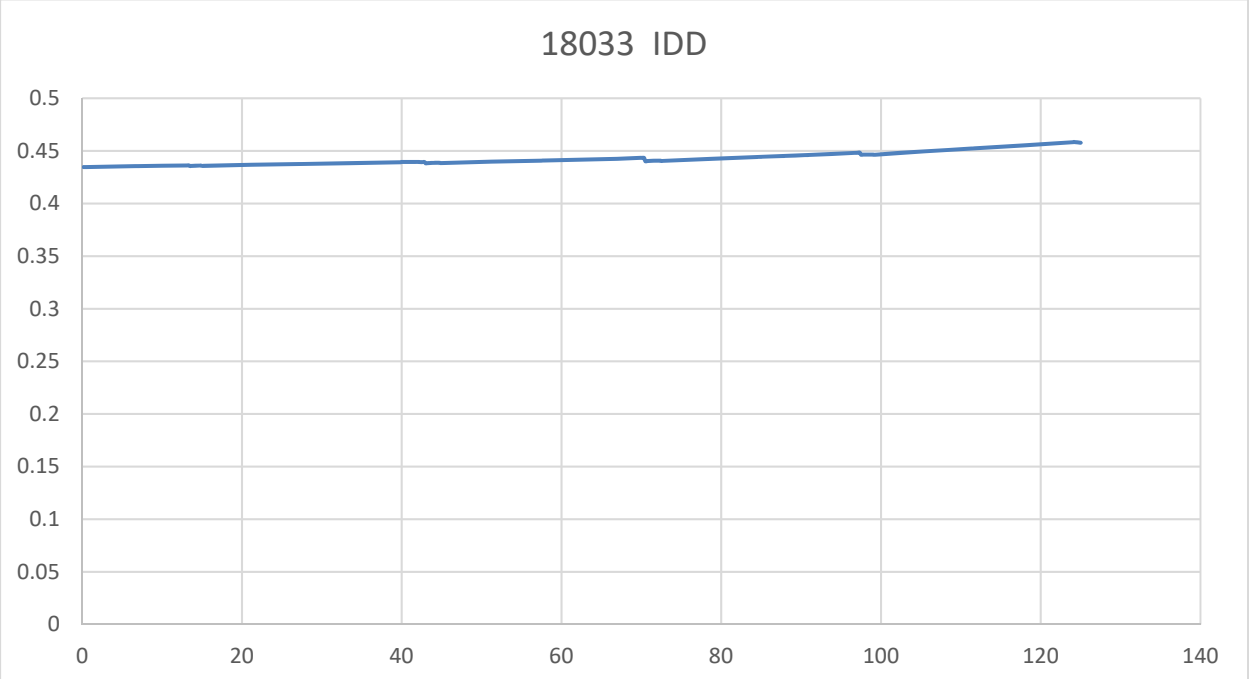

Fig. 6. DUT 18033 core power supply current (I_{DD}) versus TID

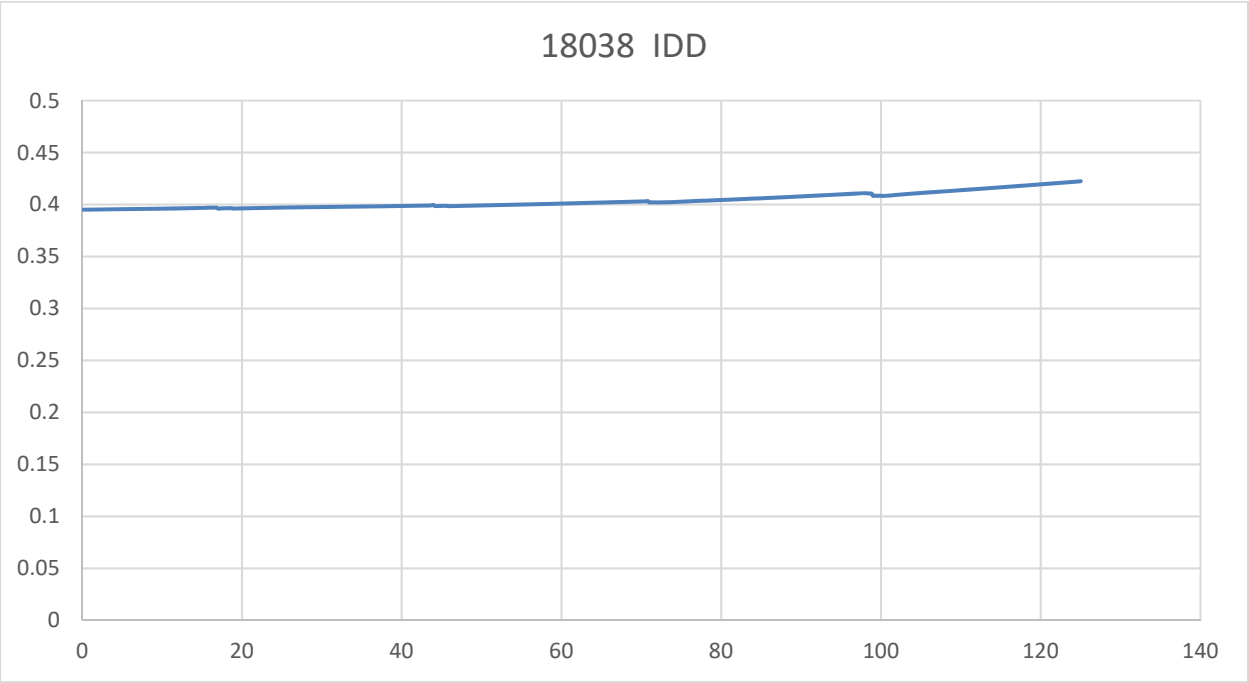

Fig. 7. DUT 18038 core power supply current (I_{DD}) versus TID

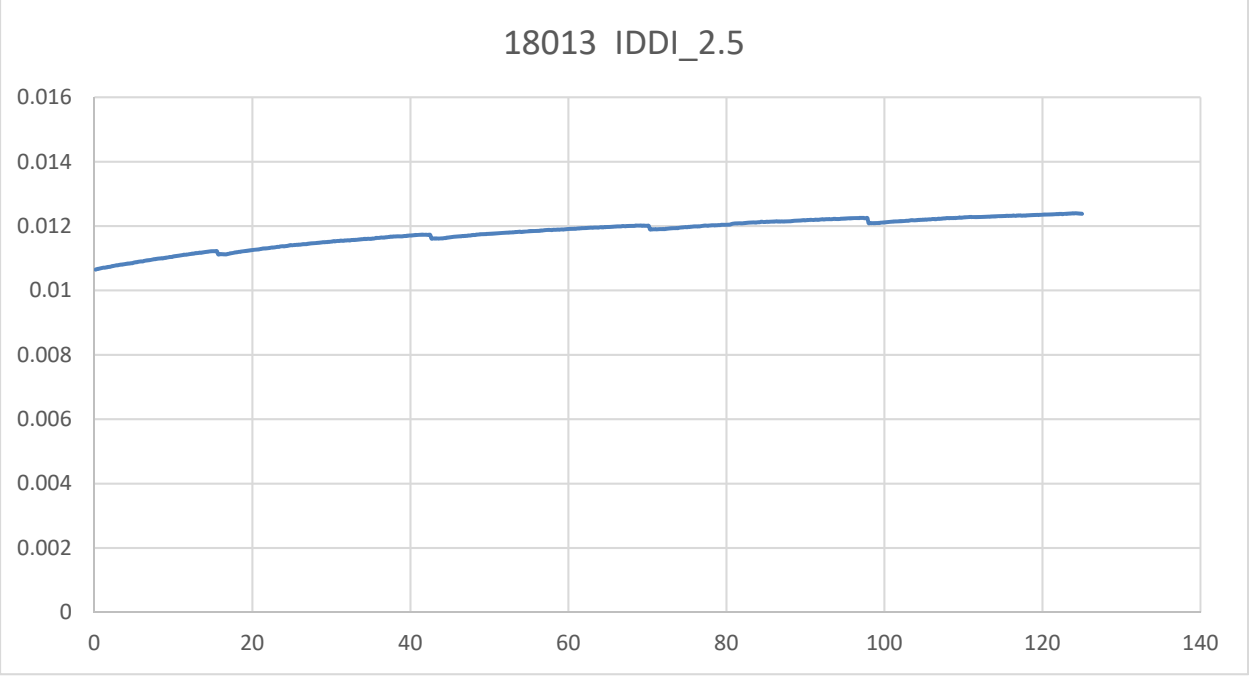

Fig. 9. DUT 18013 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

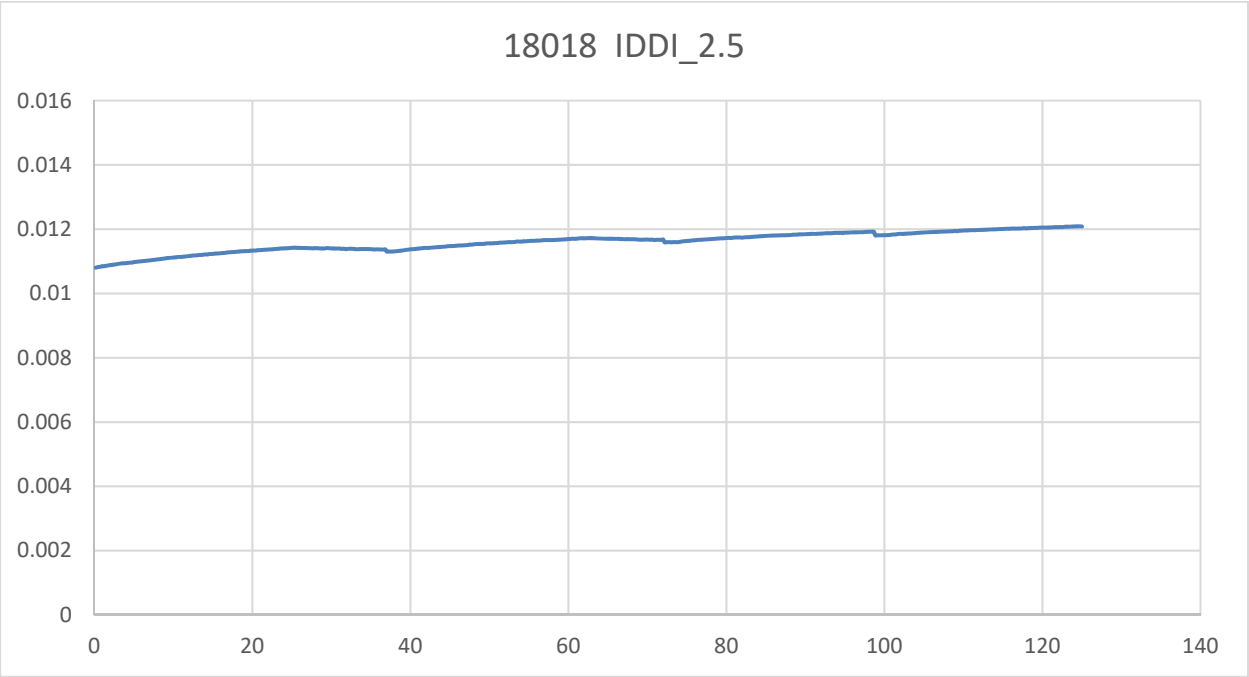

Fig. 10. DUT 18018 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

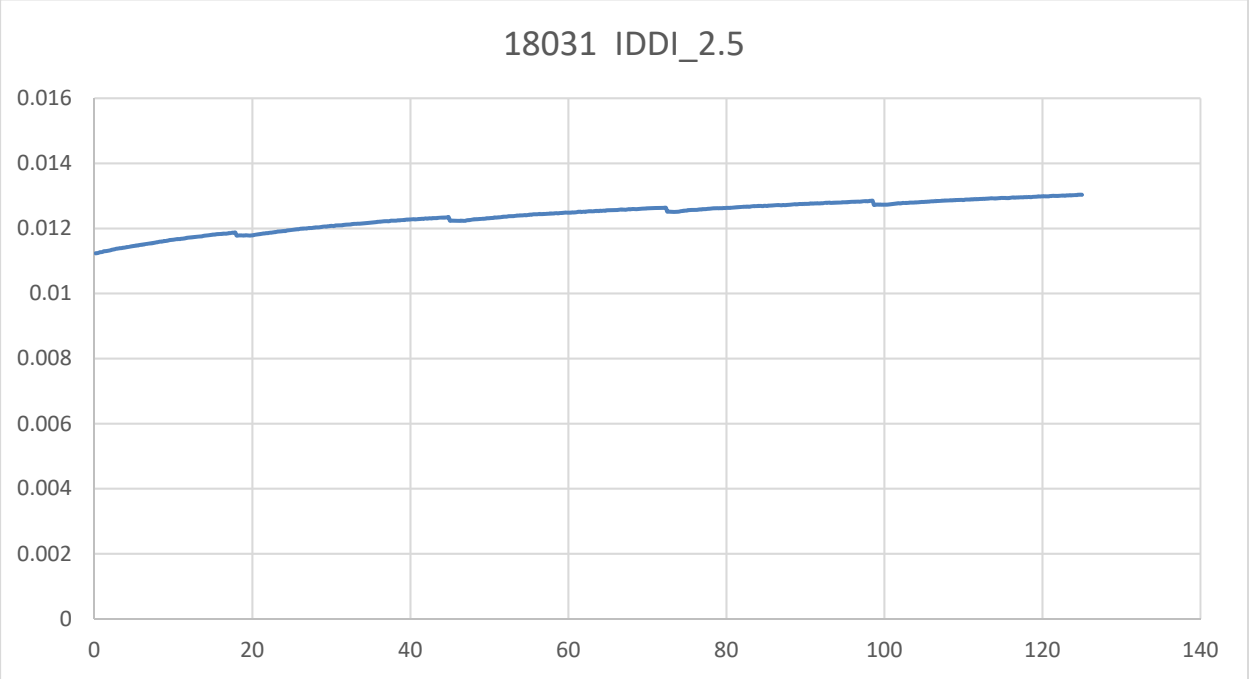

Fig. 11. DUT 18031 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

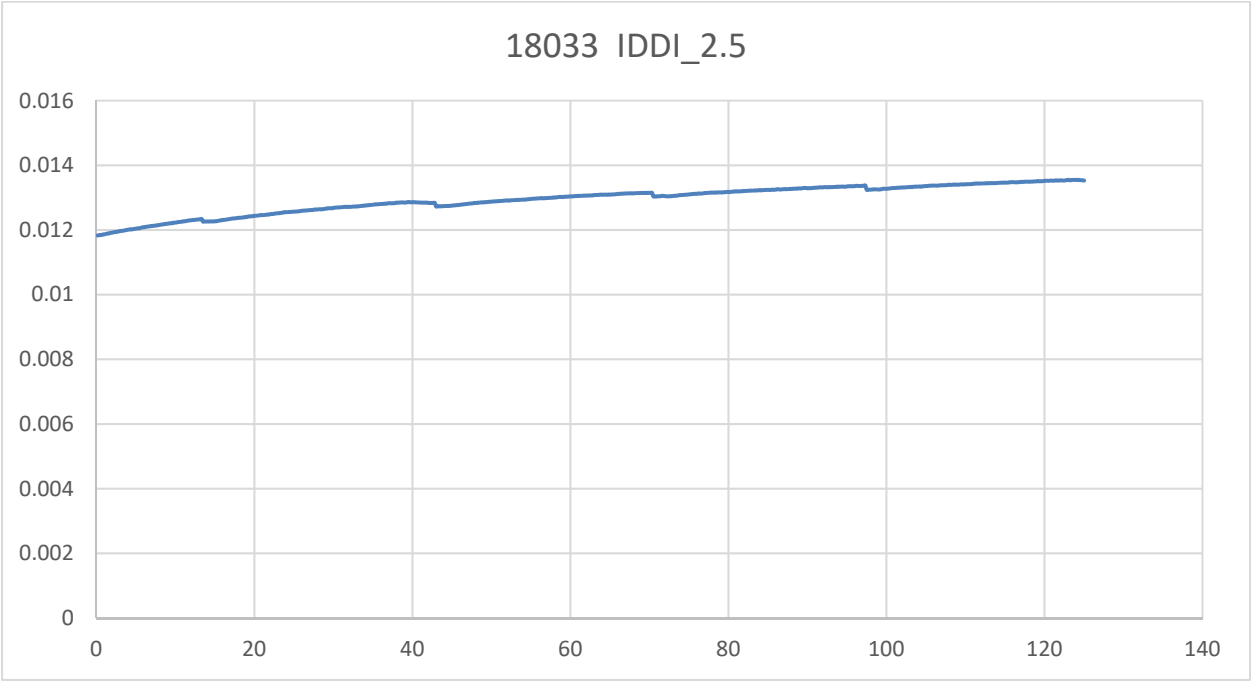

Fig. 12. DUT 18033 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

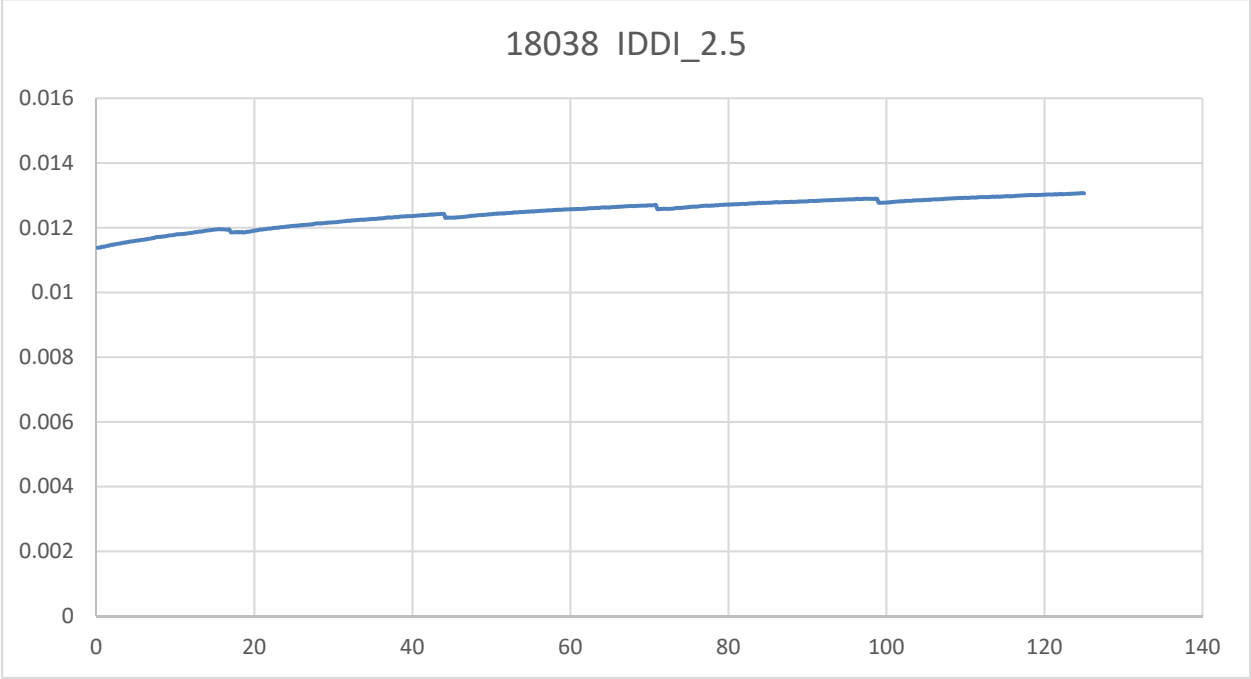

Fig. 13. DUT 18038 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

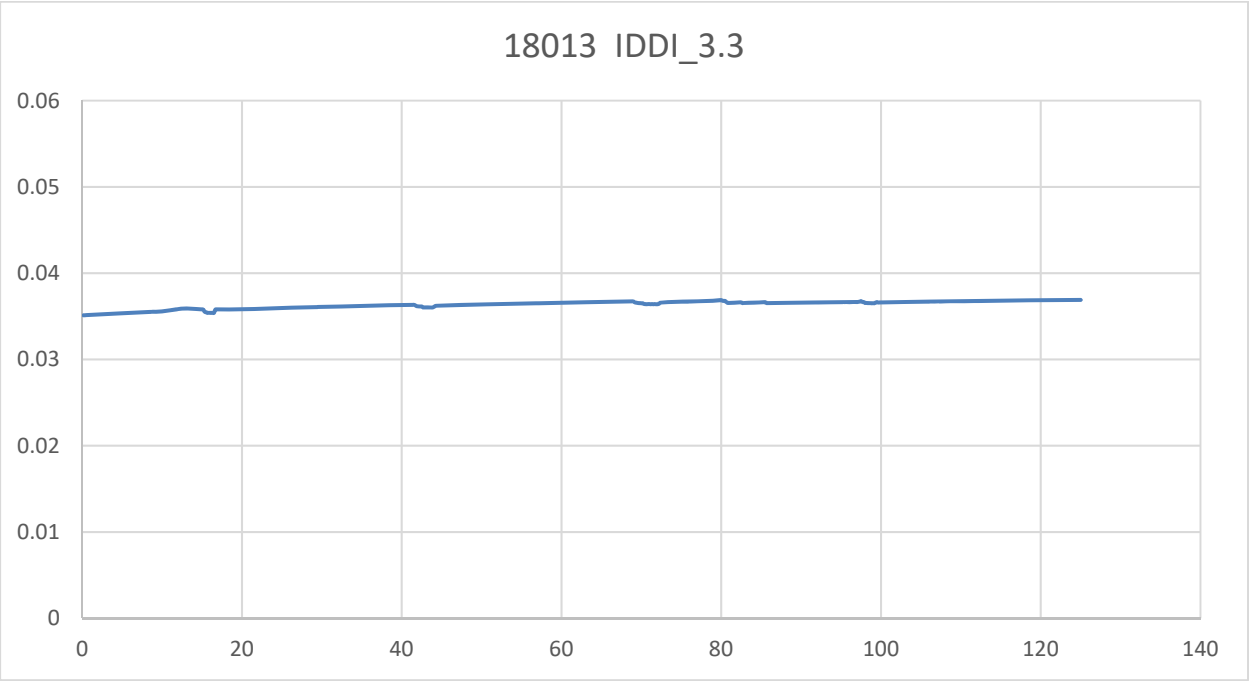

Fig. 15. DUT 18013 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

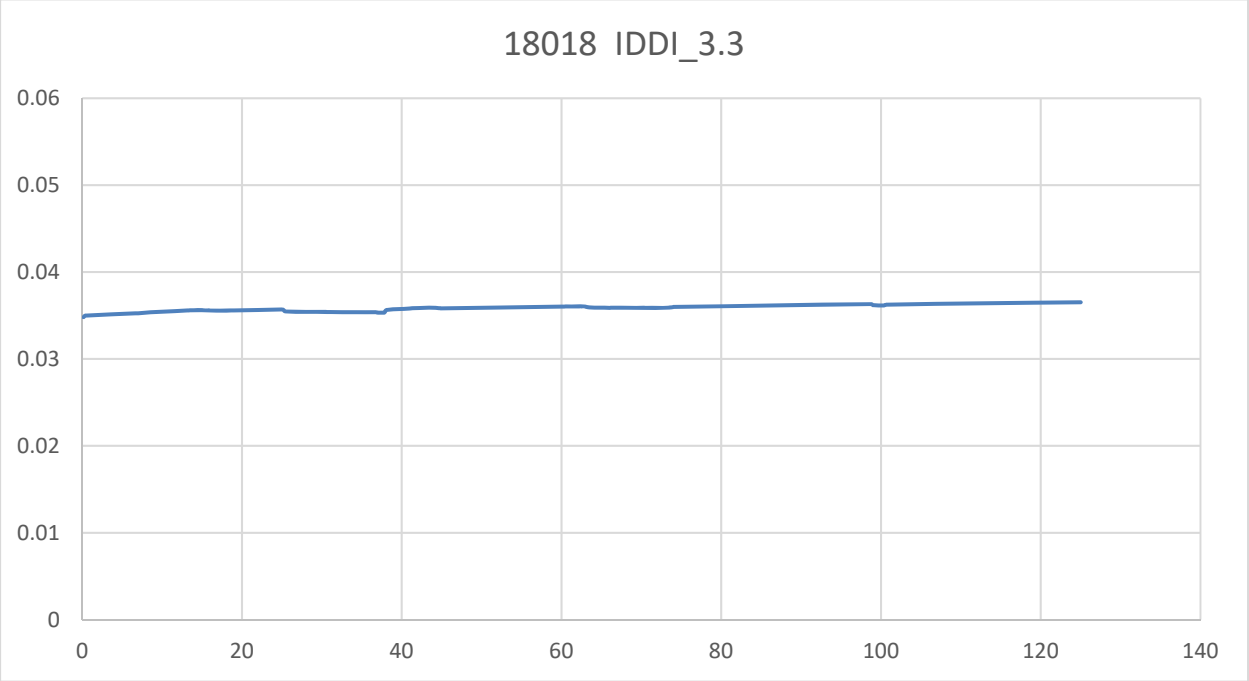

Fig. 16. DUT 18018 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

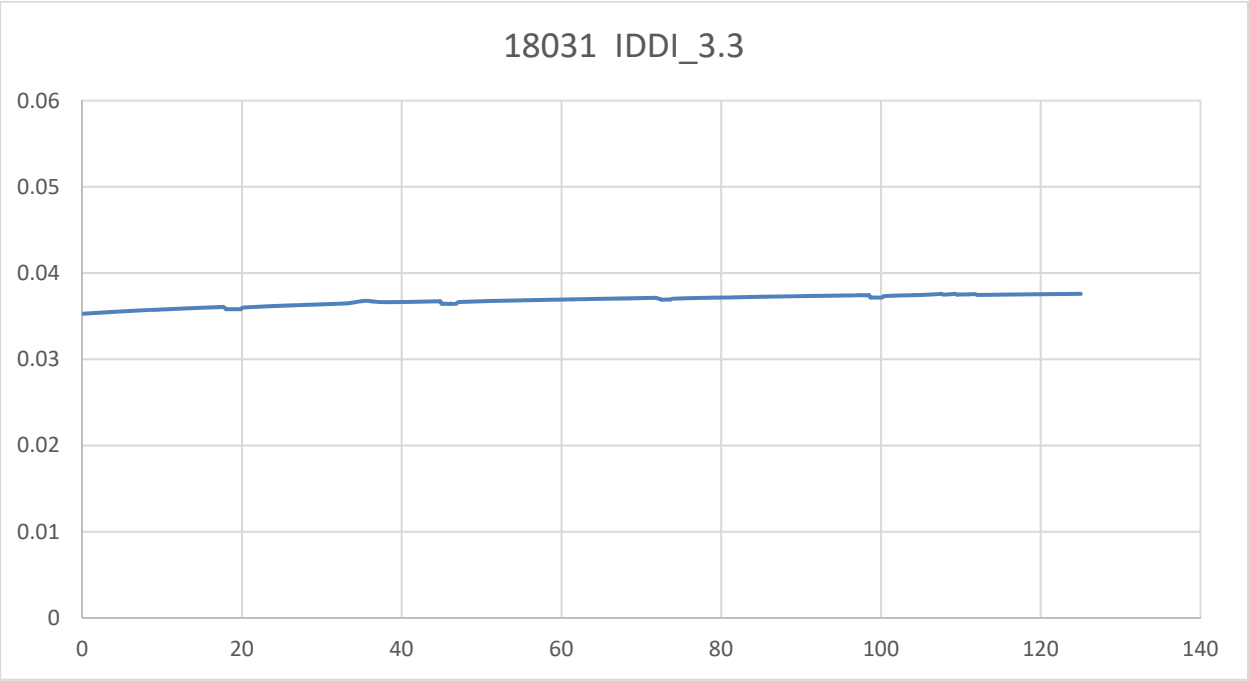

Fig. 17. DUT 18031 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

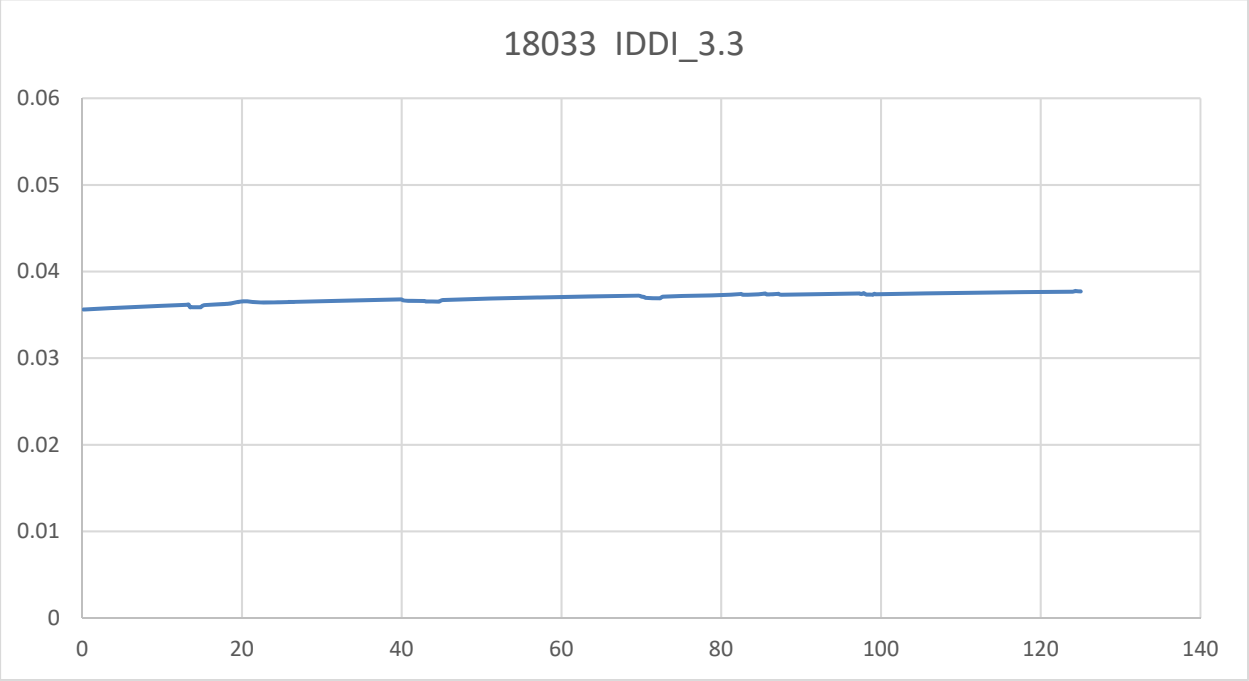

Fig. 18. DUT 18033 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

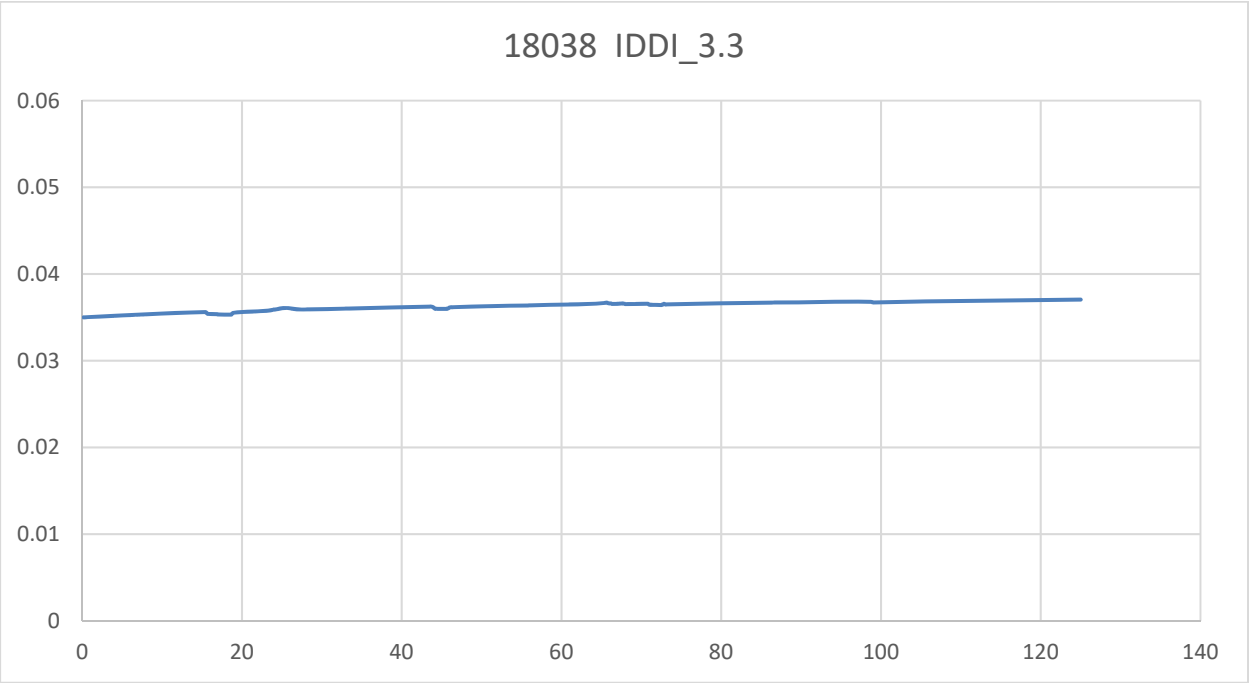

Fig. 19. DUT 18038 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

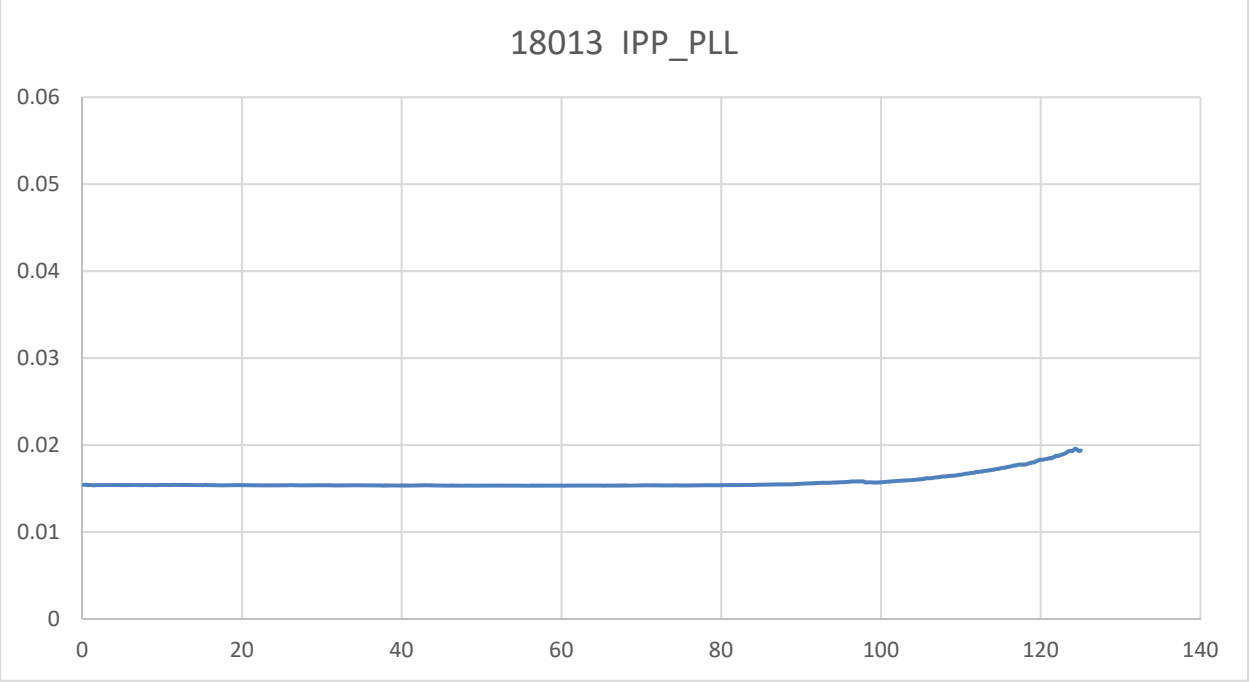

Fig. 21. DUT 18013 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

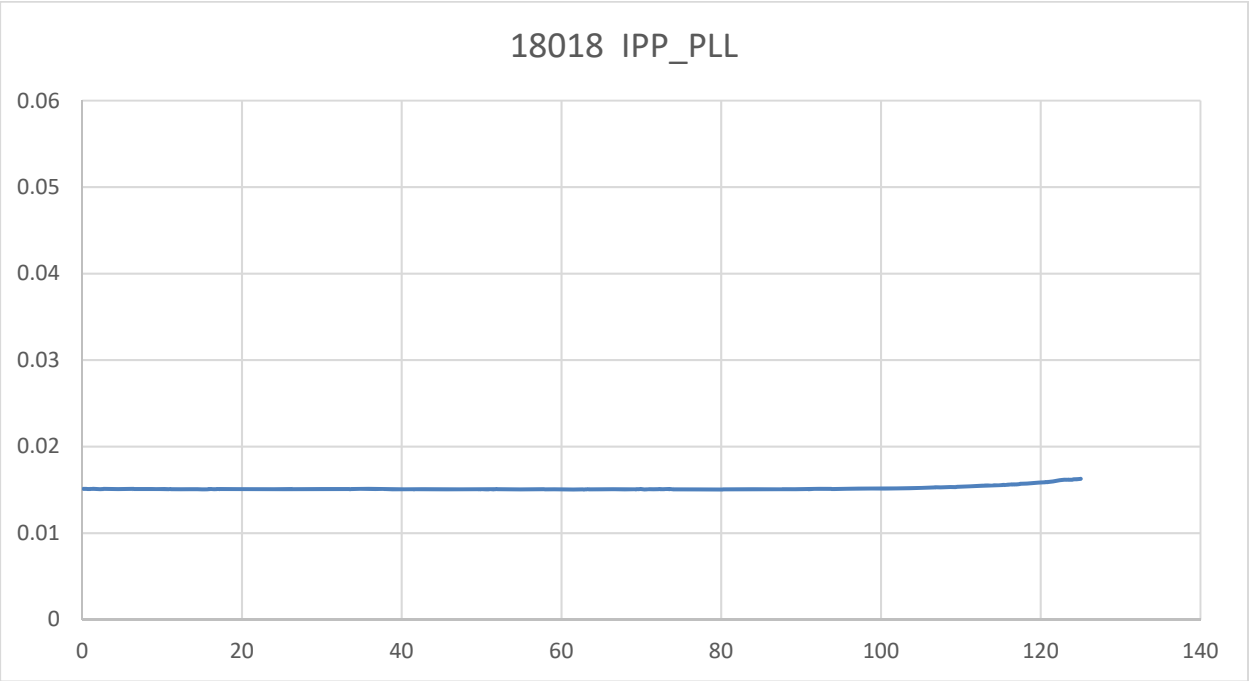

Fig. 22. DUT 18018 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

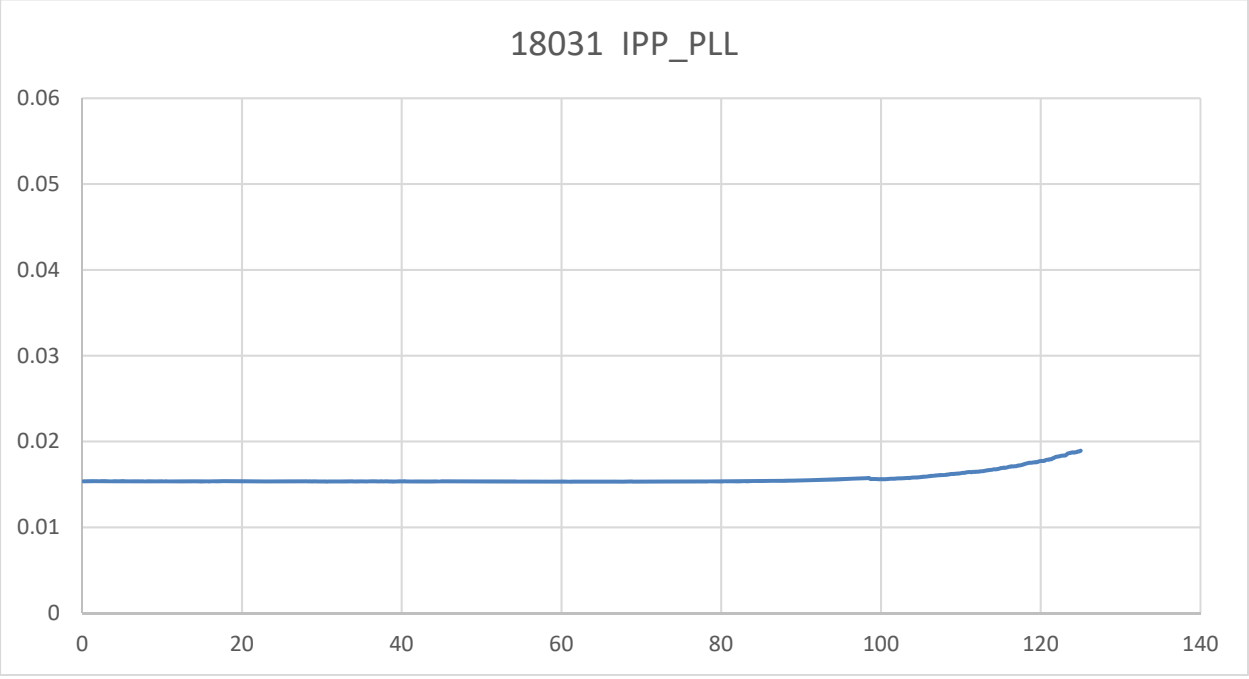

Fig. 23. DUT 18031 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

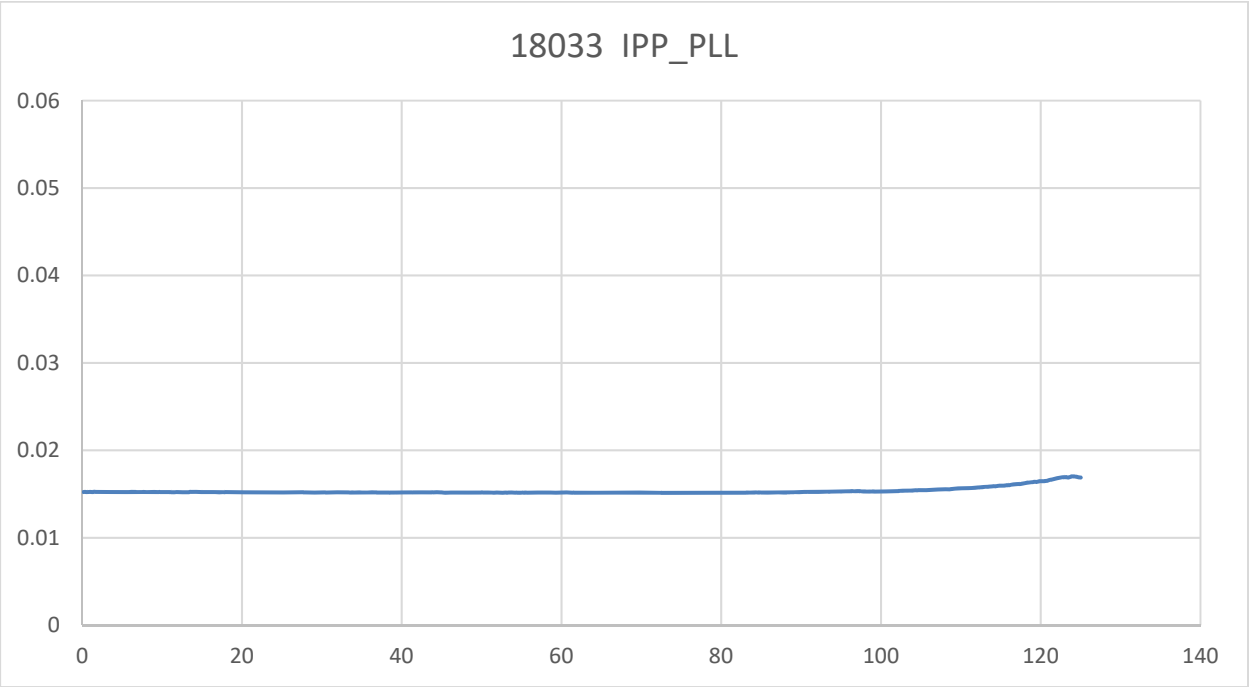

Fig. 24. DUT 18033 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

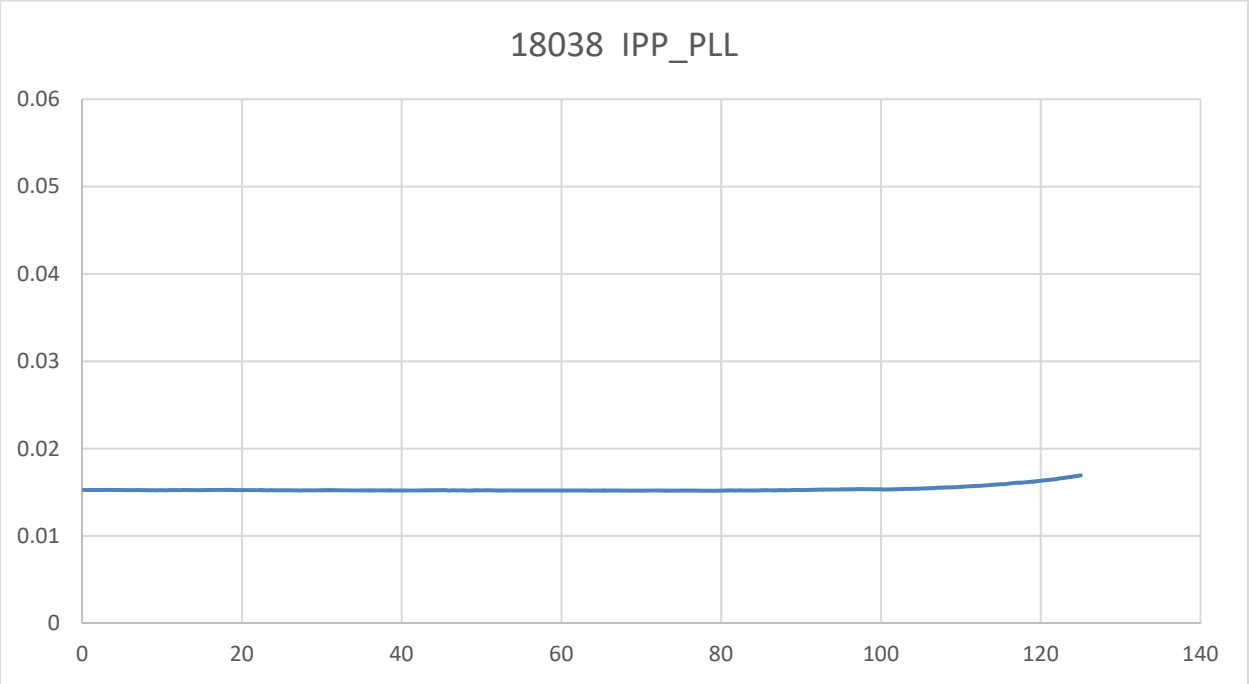

Fig. 25. DUT 18038 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 7. VIH Summary

DUT	Pre-irradiation	Post-irradiation
18013	Passed	Passed
18018	Passed	Passed
18031	Passed	Passed
18033	Passed	Passed
18038	Passed	Passed

Table. 8. VIL Summary

DUT	Pre-irradiation	Post-irradiation
18013	Passed	Passed
18018	Passed	Passed
18031	Passed	Passed
18033	Passed	Passed
18038	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 9 through 32 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 18013

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.135	2.133	2.202	2.200	2.173	2.170	2.151	2.150	2.118	2.115	2.104	2.100
EPCSRST_N_0	B31	2.136	2.134	2.203	2.200	2.173	2.170	2.151	2.150	2.118	2.115	2.103	2.100
EPCSRST_N_1	B32	2.137	2.135	2.205	2.202	2.176	2.173	2.155	2.152	2.123	2.120	2.109	2.106
EPCSRST_N_2	B34	2.136	2.134	2.203	2.201	2.174	2.172	2.153	2.150	2.119	2.117	2.106	2.103
EPCSRST_N_3	B35	2.137	2.135	2.205	2.202	2.176	2.174	2.155	2.153	2.124	2.121	2.111	2.107
EPCSRST_N_4	B36	2.136	2.133	2.202	2.200	2.173	2.170	2.151	2.148	2.116	2.113	2.102	2.098
EPCSRST_N_5	B37	2.137	2.134	2.204	2.201	2.175	2.172	2.154	2.151	2.121	2.117	2.107	2.103
MONITOR	K23	2.136	2.137	2.205	2.205	2.176	2.177	2.156	2.157	2.125	2.127	2.111	2.114
PLL_MON	L20	2.137	2.136	2.207	2.205	2.180	2.177	2.162	2.158	2.134	2.127	2.122	2.114
TOGGLE_MON	L22	2.137	2.136	2.206	2.206	2.179	2.179	2.159	2.159	2.130	2.129	2.117	2.117

Table. 11. LVCMOS 25 VOH – DUT 18018

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.135	2.132	2.202	2.199	2.173	2.169	2.151	2.149	2.118	2.115	2.104	2.100
EPCSRST_N_0	B31	2.135	2.132	2.202	2.200	2.173	2.170	2.151	2.149	2.118	2.114	2.103	2.100
EPCSRST_N_1	B32	2.137	2.134	2.205	2.202	2.176	2.173	2.155	2.152	2.123	2.120	2.110	2.106
EPCSRST_N_2	B34	2.135	2.132	2.203	2.200	2.174	2.171	2.152	2.149	2.119	2.116	2.105	2.102
EPCSRST_N_3	B35	2.136	2.133	2.204	2.202	2.176	2.173	2.155	2.152	2.123	2.120	2.110	2.107
EPCSRST_N_4	B36	2.135	2.133	2.202	2.199	2.172	2.169	2.150	2.147	2.116	2.112	2.101	2.097
EPCSRST_N_5	B37	2.135	2.133	2.203	2.200	2.174	2.171	2.152	2.150	2.120	2.116	2.106	2.102
MONITOR	K23	2.135	2.135	2.204	2.204	2.176	2.176	2.155	2.156	2.123	2.125	2.110	2.113
PLL_MON	L20	2.137	2.136	2.207	2.206	2.180	2.179	2.162	2.161	2.134	2.132	2.122	2.120
TOGGLE_MON	L22	2.136	2.136	2.205	2.205	2.177	2.178	2.157	2.158	2.127	2.128	2.115	2.116

Table. 12. LVCMOS 25 VOH – DUT 18031

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.133	2.130	2.201	2.198	2.171	2.168	2.150	2.148	2.117	2.113	2.103	2.098
EPCSRST_N_0	B31	2.133	2.131	2.201	2.198	2.171	2.169	2.150	2.148	2.116	2.113	2.102	2.098
EPCSRST_N_1	B32	2.135	2.132	2.203	2.201	2.175	2.172	2.154	2.151	2.121	2.118	2.108	2.105
EPCSRST_N_2	B34	2.133	2.131	2.202	2.199	2.172	2.170	2.151	2.149	2.118	2.115	2.104	2.101
EPCSRST_N_3	B35	2.134	2.132	2.203	2.201	2.175	2.172	2.154	2.152	2.122	2.119	2.109	2.106
EPCSRST_N_4	B36	2.133	2.131	2.201	2.199	2.171	2.168	2.149	2.146	2.115	2.112	2.100	2.097
EPCSRST_N_5	B37	2.134	2.132	2.202	2.200	2.173	2.170	2.152	2.149	2.119	2.116	2.105	2.102
MONITOR	K23	2.133	2.134	2.203	2.203	2.174	2.175	2.153	2.155	2.122	2.124	2.109	2.111
PLL_MON	L20	2.135	2.134	2.205	2.205	2.179	2.178	2.160	2.159	2.132	2.130	2.120	2.118
TOGGLE_MON	L22	2.134	2.134	2.204	2.204	2.177	2.177	2.157	2.157	2.127	2.127	2.115	2.115

Table. 13. LVCMOS 25 VOH – DUT 18033

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.133	2.130	2.201	2.198	2.171	2.168	2.149	2.148	2.116	2.113	2.101	2.098
EPCSRST_N_0	B31	2.133	2.131	2.201	2.198	2.171	2.168	2.150	2.148	2.116	2.113	2.101	2.098
EPCSRST_N_1	B32	2.135	2.132	2.203	2.201	2.174	2.172	2.153	2.150	2.121	2.118	2.108	2.104
EPCSRST_N_2	B34	2.133	2.131	2.201	2.199	2.172	2.170	2.150	2.148	2.117	2.115	2.103	2.100
EPCSRST_N_3	B35	2.134	2.132	2.203	2.201	2.175	2.172	2.154	2.151	2.122	2.119	2.108	2.105
EPCSRST_N_4	B36	2.133	2.130	2.200	2.198	2.170	2.168	2.148	2.145	2.113	2.110	2.099	2.095
EPCSRST_N_5	B37	2.134	2.132	2.202	2.199	2.173	2.170	2.151	2.148	2.118	2.115	2.104	2.100
MONITOR	K23	2.133	2.133	2.202	2.203	2.174	2.175	2.153	2.155	2.121	2.124	2.108	2.111
PLL_MON	L20	2.135	2.134	2.205	2.205	2.179	2.178	2.160	2.159	2.132	2.131	2.120	2.118
TOGGLE_MON	L22	2.134	2.134	2.204	2.204	2.176	2.177	2.157	2.157	2.127	2.127	2.114	2.115

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Table. 14. LVCMOS 25 VOH – DUT 18038

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.132	2.129	2.200	2.197	2.170	2.167	2.148	2.147	2.114	2.112	2.100	2.097
EPCSRST_N_0	B31	2.133	2.130	2.201	2.198	2.171	2.168	2.149	2.147	2.115	2.112	2.100	2.097
EPCSRST_N_1	B32	2.134	2.131	2.203	2.200	2.174	2.171	2.153	2.150	2.121	2.117	2.107	2.103
EPCSRST_N_2	B34	2.132	2.130	2.201	2.199	2.171	2.169	2.150	2.147	2.117	2.114	2.103	2.100
EPCSRST_N_3	B35	2.133	2.130	2.202	2.200	2.174	2.171	2.153	2.150	2.121	2.118	2.108	2.104
EPCSRST_N_4	B36	2.132	2.129	2.200	2.197	2.170	2.167	2.147	2.144	2.112	2.109	2.098	2.094
EPCSRST_N_5	B37	2.132	2.130	2.201	2.198	2.172	2.169	2.150	2.147	2.117	2.113	2.103	2.099
MONITOR	K23	2.132	2.132	2.202	2.202	2.173	2.174	2.153	2.154	2.121	2.123	2.108	2.110
PLL_MON	L20	2.134	2.133	2.205	2.204	2.178	2.177	2.160	2.158	2.131	2.129	2.119	2.117
TOGGLE_MON	L22	2.134	2.134	2.204	2.204	2.176	2.176	2.157	2.156	2.127	2.127	2.115	2.114

Table. 16. LVCMOS 25 VOL – DUT 18013

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	234.7	233.7	168.4	168.2	197.1	197.2	218.4	220.4	251.1	253.3	265.3	267.8
EPCSRST_N_0	B31	233.4	233.0	168.3	168.3	197.0	197.4	218.3	220.9	251.8	254.3	266.1	269.0
EPCSRST_N_1	B32	232.7	232.3	166.3	166.3	194.2	194.4	214.8	215.3	246.7	247.3	260.0	260.9
EPCSRST_N_2	B34	233.9	233.4	167.9	167.6	196.2	196.1	217.0	217.5	249.7	250.0	263.8	264.0
EPCSRST_N_3	B35	233.8	233.2	166.6	166.4	194.3	194.3	214.6	215.0	245.9	246.4	259.1	259.8
EPCSRST_N_4	B36	235.0	234.5	169.3	169.0	198.2	198.2	219.7	220.1	253.7	254.1	268.1	268.9
EPCSRST_N_5	B37	233.7	233.4	167.5	167.4	195.7	196.0	216.6	217.3	248.8	249.8	262.4	263.8
MONITOR	K23	232.9	231.5	166.0	164.6	193.6	191.7	213.2	211.5	243.8	240.9	256.8	253.6
PLL_MON	L20	231.7	231.6	163.0	164.6	189.0	191.9	208.3	212.3	236.0	242.0	247.7	255.0
TOGGLE_MON	L22	232.5	231.2	164.3	163.5	190.9	190.2	210.0	209.0	239.1	238.2	251.4	250.7

Table. 17. LVCMOS 25 VOL – DUT 18018

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.3	234.6	168.6	168.5	197.1	197.5	218.3	220.7	251.0	253.6	265.0	268.0
EPCSRST_N_0	B31	234.3	233.8	168.4	168.5	197.2	197.8	218.5	221.0	251.7	254.3	265.8	268.8
EPCSRST_N_1	B32	233.0	232.7	166.4	166.4	194.2	194.4	214.6	215.2	246.3	247.0	259.6	260.6
EPCSRST_N_2	B34	234.9	234.6	168.5	168.5	197.0	197.0	217.7	218.2	250.5	250.8	264.2	264.9
EPCSRST_N_3	B35	234.4	234.1	167.0	166.9	194.8	194.9	215.0	215.6	246.4	246.8	259.4	260.2
EPCSRST_N_4	B36	235.8	235.4	169.6	169.5	198.8	198.9	220.0	220.7	254.1	254.8	268.7	269.7
EPCSRST_N_5	B37	234.8	234.4	168.3	168.3	196.7	197.0	217.5	218.2	250.0	250.9	263.7	265.1
MONITOR	K23	233.6	232.3	166.3	164.9	194.0	192.2	213.9	212.1	244.8	242.0	258.0	254.8
PLL_MON	L20	231.5	230.7	163.1	163.3	189.3	189.7	208.5	209.2	236.0	237.3	247.5	248.6
TOGGLE_MON	L22	232.7	231.3	165.0	163.8	192.0	190.5	211.4	209.5	241.1	238.8	253.6	251.1

Table. 18. LVCMOS 25 VOL – DUT 18031

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.4	237.5	170.4	170.3	199.2	199.5	220.4	222.7	253.2	255.7	267.3	270.1
EPCSRST_N_0	B31	237.5	236.9	170.3	170.4	199.3	199.7	220.8	223.1	254.0	256.5	268.3	271.0
EPCSRST_N_1	B32	236.0	235.6	168.2	168.1	196.1	196.3	216.5	217.4	248.5	249.3	262.0	263.0
EPCSRST_N_2	B34	237.6	237.3	170.3	169.9	198.7	198.6	219.4	219.8	252.1	252.4	266.1	266.5
EPCSRST_N_3	B35	236.7	236.2	168.4	168.2	196.2	196.2	216.5	217.0	248.1	248.4	261.1	261.8
EPCSRST_N_4	B36	238.0	237.6	171.2	171.0	200.3	200.3	221.8	222.1	255.6	256.1	270.1	270.7
EPCSRST_N_5	B37	237.0	236.4	169.5	169.6	198.1	198.2	218.6	219.5	251.0	252.0	264.7	266.1
MONITOR	K23	236.8	235.5	168.3	166.9	196.1	194.4	216.0	214.2	246.8	244.1	260.0	257.1
PLL_MON	L20	234.8	234.1	165.2	165.2	191.5	191.7	210.8	211.3	238.6	239.7	250.4	251.8
TOGGLE_MON	L22	236.1	234.8	166.6	165.6	193.5	192.5	212.7	211.6	241.9	240.7	254.2	253.0

Table. 19. LVCMOS 25 VOL – DUT 18033

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.1	237.2	170.6	170.3	199.7	199.5	221.0	222.8	254.2	255.9	268.3	270.2
EPCSRST_N_0	B31	237.5	236.9	170.5	170.3	199.4	199.6	220.9	223.1	254.3	256.5	268.6	271.1
EPCSRST_N_1	B32	235.9	235.4	168.3	168.2	196.5	196.7	216.9	217.6	248.9	249.6	262.3	263.4
EPCSRST_N_2	B34	238.0	237.6	170.3	170.1	198.9	198.8	219.9	220.1	252.8	253.1	266.7	267.2
EPCSRST_N_3	B35	237.3	236.9	168.9	168.6	197.0	196.9	217.4	217.7	248.8	249.3	262.0	262.8
EPCSRST_N_4	B36	238.9	238.5	171.8	171.7	201.1	201.3	222.8	223.3	256.9	257.6	271.5	272.5
EPCSRST_N_5	B37	237.5	237.1	170.2	170.1	198.8	199.0	219.8	220.5	252.6	253.5	266.3	267.6
MONITOR	K23	236.8	235.3	168.2	166.6	196.2	194.1	216.2	214.1	247.2	244.0	260.4	256.9
PLL_MON	L20	234.8	234.0	165.0	164.9	191.3	191.6	210.6	211.1	238.4	239.1	250.2	251.1
TOGGLE_MON	L22	235.9	234.5	166.6	165.5	193.6	192.5	213.0	211.4	242.4	241.0	254.7	253.3

Table. 20. LVCMOS 25 VOL – DUT 18038

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.8	238.1	171.2	171.1	200.2	200.3	221.8	223.7	255.1	256.9	269.3	271.4
EPCSRST_N_0	B31	237.4	237.2	170.4	170.8	199.5	200.3	221.1	223.7	254.5	257.4	268.7	272.0
EPCSRST_N_1	B32	236.3	236.2	168.5	168.7	196.7	196.9	217.1	218.0	249.2	250.1	262.5	264.0
EPCSRST_N_2	B34	237.9	237.6	170.2	170.2	199.0	199.0	219.9	220.5	252.6	253.2	266.6	267.3
EPCSRST_N_3	B35	237.3	237.1	168.9	168.9	196.9	197.1	217.3	218.0	248.8	249.6	261.9	263.0
EPCSRST_N_4	B36	238.9	238.7	171.9	172.0	201.6	201.7	223.0	223.9	257.4	258.2	272.1	273.1
EPCSRST_N_5	B37	238.3	238.1	170.4	170.5	199.1	199.6	220.0	221.2	252.8	254.1	266.5	268.2
MONITOR	K23	237.1	236.1	168.6	167.3	196.6	194.8	216.6	214.9	247.6	244.7	260.7	257.6
PLL_MON	L20	235.6	235.2	165.3	165.8	191.8	192.5	211.1	212.2	239.0	240.7	250.6	252.7
TOGGLE_MON	L22	235.5	234.6	166.5	165.9	193.4	192.8	212.4	211.8	241.7	241.1	253.9	253.6

Table. 22. LVTTL VOH – DUT 18013

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.923	2.919	2.913	2.909	2.892	2.888	2.872	2.867	2.852	2.847
EPCSRST_N_0	B31	2.923	2.920	2.913	2.909	2.892	2.888	2.871	2.866	2.851	2.846
EPCSRST_N_1	B32	2.924	2.921	2.914	2.911	2.896	2.892	2.877	2.873	2.858	2.854
EPCSRST_N_2	B34	2.923	2.920	2.913	2.910	2.893	2.890	2.873	2.870	2.854	2.850
EPCSRST_N_3	B35	2.924	2.921	2.915	2.911	2.896	2.893	2.878	2.874	2.860	2.855
EPCSRST_N_4	B36	2.923	2.920	2.912	2.909	2.891	2.888	2.870	2.866	2.849	2.845
EPCSRST_N_5	B37	2.924	2.921	2.914	2.911	2.894	2.890	2.875	2.871	2.856	2.851
MONITOR	K23	2.923	2.923	2.914	2.915	2.896	2.897	2.878	2.880	2.860	2.863
PLL_MON	L20	2.924	2.923	2.917	2.914	2.902	2.896	2.887	2.878	2.872	2.861
TOGGLE_MON	L22	2.924	2.923	2.915	2.915	2.899	2.899	2.883	2.883	2.867	2.867

Table. 23. LVTTL VOH – DUT 18018

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.922	2.919	2.912	2.908	2.892	2.888	2.872	2.867	2.852	2.847
EPCSRST_N_0	B31	2.922	2.919	2.912	2.909	2.892	2.888	2.871	2.867	2.851	2.846
EPCSRST_N_1	B32	2.924	2.921	2.914	2.911	2.895	2.892	2.877	2.873	2.858	2.854
EPCSRST_N_2	B34	2.922	2.919	2.912	2.909	2.892	2.889	2.873	2.869	2.853	2.849
EPCSRST_N_3	B35	2.923	2.920	2.914	2.911	2.895	2.892	2.877	2.874	2.859	2.855
EPCSRST_N_4	B36	2.922	2.919	2.912	2.908	2.890	2.887	2.870	2.866	2.849	2.844
EPCSRST_N_5	B37	2.923	2.920	2.913	2.909	2.893	2.890	2.874	2.869	2.854	2.849
MONITOR	K23	2.922	2.922	2.913	2.914	2.895	2.896	2.877	2.879	2.859	2.861
PLL_MON	L20	2.924	2.924	2.916	2.916	2.901	2.900	2.886	2.885	2.872	2.870
TOGGLE_MON	L22	2.923	2.923	2.914	2.915	2.898	2.899	2.881	2.883	2.864	2.866

Table. 24. LVTTL VOH – DUT 18031

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.917	2.910	2.906	2.890	2.886	2.870	2.865	2.850	2.846
EPCSRST_N_0	B31	2.921	2.918	2.910	2.907	2.890	2.886	2.870	2.865	2.849	2.845
EPCSRST_N_1	B32	2.922	2.919	2.912	2.909	2.894	2.891	2.875	2.872	2.857	2.852
EPCSRST_N_2	B34	2.921	2.917	2.911	2.908	2.891	2.888	2.872	2.868	2.852	2.848
EPCSRST_N_3	B35	2.922	2.919	2.913	2.910	2.895	2.891	2.876	2.873	2.858	2.854
EPCSRST_N_4	B36	2.921	2.918	2.910	2.907	2.889	2.886	2.868	2.865	2.848	2.844
EPCSRST_N_5	B37	2.922	2.919	2.912	2.908	2.892	2.889	2.873	2.869	2.854	2.849
MONITOR	K23	2.921	2.921	2.911	2.912	2.894	2.895	2.876	2.877	2.858	2.860
PLL_MON	L20	2.922	2.922	2.915	2.914	2.900	2.899	2.885	2.883	2.870	2.868
TOGGLE_MON	L22	2.921	2.921	2.913	2.913	2.897	2.897	2.881	2.881	2.865	2.865

Table. 25. LVTTL VOH – DUT 18033

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.917	2.910	2.907	2.890	2.886	2.870	2.866	2.849	2.845
EPCSRST_N_0	B31	2.920	2.917	2.910	2.907	2.890	2.886	2.870	2.865	2.849	2.845
EPCSRST_N_1	B32	2.922	2.919	2.913	2.909	2.894	2.890	2.875	2.871	2.856	2.852
EPCSRST_N_2	B34	2.920	2.918	2.911	2.908	2.891	2.888	2.871	2.868	2.851	2.848
EPCSRST_N_3	B35	2.922	2.919	2.913	2.909	2.894	2.891	2.876	2.872	2.857	2.853
EPCSRST_N_4	B36	2.920	2.917	2.910	2.906	2.889	2.885	2.868	2.864	2.846	2.842
EPCSRST_N_5	B37	2.921	2.918	2.911	2.908	2.892	2.888	2.872	2.868	2.852	2.847
MONITOR	K23	2.920	2.921	2.911	2.912	2.893	2.895	2.875	2.877	2.857	2.860
PLL_MON	L20	2.922	2.922	2.915	2.914	2.900	2.899	2.885	2.883	2.870	2.869
TOGGLE_MON	L22	2.921	2.921	2.913	2.913	2.897	2.897	2.880	2.881	2.864	2.865

Table. 26. LVTTL VOH – DUT 18038

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.916	2.909	2.905	2.889	2.885	2.868	2.864	2.848	2.844
EPCSRST_N_0	B31	2.920	2.917	2.910	2.906	2.890	2.885	2.869	2.864	2.849	2.843
EPCSRST_N_1	B32	2.921	2.918	2.912	2.908	2.893	2.890	2.874	2.870	2.855	2.851
EPCSRST_N_2	B34	2.920	2.917	2.910	2.907	2.890	2.887	2.871	2.867	2.851	2.847
EPCSRST_N_3	B35	2.921	2.917	2.912	2.908	2.893	2.890	2.875	2.871	2.857	2.852
EPCSRST_N_4	B36	2.919	2.916	2.909	2.905	2.888	2.884	2.866	2.862	2.845	2.841
EPCSRST_N_5	B37	2.920	2.917	2.910	2.907	2.891	2.887	2.871	2.866	2.852	2.846
MONITOR	K23	2.920	2.920	2.911	2.911	2.893	2.894	2.875	2.877	2.857	2.859
PLL_MON	L20	2.921	2.920	2.914	2.913	2.899	2.898	2.884	2.882	2.869	2.867
TOGGLE_MON	L22	2.921	2.921	2.913	2.913	2.897	2.897	2.881	2.881	2.864	2.864

Table. 28. LVTTL VOL – DUT 18013

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	214.5	213.9	224.2	226.7	243.7	244.3	263.9	265.0	284.4	287.2
EPCSRST_N_0	B31	213.6	213.1	224.0	226.3	243.8	244.5	264.4	265.8	285.4	288.7
EPCSRST_N_1	B32	213.1	212.5	221.7	221.7	240.5	240.5	259.5	259.9	278.5	279.6
EPCSRST_N_2	B34	213.9	213.4	223.0	223.0	243.0	242.8	262.8	262.6	282.7	283.1
EPCSRST_N_3	B35	213.9	213.2	221.9	221.8	240.5	240.4	258.8	259.1	277.2	278.2
EPCSRST_N_4	B36	214.9	214.6	224.5	224.7	245.5	245.7	266.5	267.0	287.8	288.6
EPCSRST_N_5	B37	213.7	213.3	222.6	222.6	242.5	242.6	261.9	262.5	281.1	282.7
MONITOR	K23	213.0	211.5	221.0	219.7	239.4	236.9	257.0	253.7	274.7	271.1
PLL_MON	L20	211.7	212.1	219.6	221.3	233.2	238.4	248.0	256.2	264.0	274.4
TOGGLE_MON	L22	212.4	211.4	220.0	218.1	235.8	235.2	251.9	251.4	268.4	267.8

Table. 29. LVTTL VOL – DUT 18018

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	214.7	214.4	224.5	227.0	243.9	244.4	263.5	265.0	283.7	287.1
EPCSRST_N_0	B31	214.3	213.7	224.1	226.9	244.0	244.6	264.2	265.7	284.8	288.2
EPCSRST_N_1	B32	213.1	212.8	221.4	221.7	240.2	240.5	258.8	259.5	277.7	279.0
EPCSRST_N_2	B34	215.0	214.5	223.8	223.9	243.7	243.7	263.2	263.6	283.1	283.7
EPCSRST_N_3	B35	214.5	214.1	222.5	222.2	241.0	241.0	259.3	259.5	277.5	278.4
EPCSRST_N_4	B36	215.8	215.2	224.8	225.1	246.2	246.3	266.9	267.3	287.9	289.1
EPCSRST_N_5	B37	214.6	214.5	223.7	223.9	243.5	243.8	262.6	263.6	282.3	284.0
MONITOR	K23	213.6	212.2	221.7	220.0	240.0	237.4	257.9	254.4	275.9	272.3
PLL_MON	L20	211.2	210.7	219.4	219.1	233.2	233.8	247.7	249.3	263.7	265.7
TOGGLE_MON	L22	212.6	211.3	220.3	218.4	237.1	235.4	253.9	251.7	270.9	268.1

Table. 30. LVTTL VOL – DUT 18031

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.6	216.8	227.2	229.4	246.1	246.7	265.7	267.0	286.0	289.1
EPCSRST_N_0	B31	216.8	216.4	226.8	229.1	246.5	247.2	266.5	267.6	287.4	290.2
EPCSRST_N_1	B32	215.6	215.1	223.9	224.3	242.7	242.8	261.2	261.7	280.0	281.3
EPCSRST_N_2	B34	217.4	216.7	226.0	225.9	245.8	245.6	265.2	264.8	284.7	285.4
EPCSRST_N_3	B35	216.4	215.9	223.8	223.9	242.5	242.5	260.6	261.0	279.2	279.9
EPCSRST_N_4	B36	217.4	216.9	227.1	227.0	247.9	248.0	268.3	268.6	289.2	290.2
EPCSRST_N_5	B37	216.4	215.9	225.4	225.3	244.9	245.0	263.8	264.7	283.3	284.8
MONITOR	K23	216.3	214.6	224.0	222.7	242.3	239.7	260.2	256.9	277.8	274.4
PLL_MON	L20	214.0	213.3	222.1	221.7	235.7	236.2	250.5	251.5	266.5	268.1
TOGGLE_MON	L22	215.5	214.1	222.4	221.0	238.5	237.6	254.5	253.5	271.0	269.7

Table. 31. LVTTL VOL – DUT 18033

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.2	216.4	227.2	229.2	246.6	246.6	266.8	267.0	287.1	289.3
EPCSRST_N_0	B31	216.8	216.2	226.7	228.9	246.6	246.9	266.9	267.6	287.6	290.2
EPCSRST_N_1	B32	215.4	215.0	223.5	224.0	243.0	243.0	261.5	262.1	280.5	281.7
EPCSRST_N_2	B34	217.4	216.7	226.2	226.0	245.8	245.6	265.3	265.4	285.4	286.0
EPCSRST_N_3	B35	216.8	216.1	224.5	224.7	243.3	243.4	261.5	261.7	280.1	280.9
EPCSRST_N_4	B36	218.4	217.7	227.6	227.8	248.8	249.0	269.7	270.1	290.8	292.0
EPCSRST_N_5	B37	216.9	216.4	225.8	225.9	245.8	246.0	265.4	266.0	284.9	286.5
MONITOR	K23	216.2	214.7	224.1	222.4	242.3	239.6	260.2	256.6	278.3	274.2
PLL_MON	L20	214.0	213.2	221.8	221.6	235.3	235.8	250.4	251.1	266.0	267.5
TOGGLE_MON	L22	215.1	214.0	222.6	220.8	238.9	237.6	255.0	253.7	271.7	270.0

Table. 32. LVTTL VOL – DUT 18038

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.8	217.2	228.0	230.4	247.6	247.7	267.8	268.2	288.3	290.5
EPCSRST_N_0	B31	216.6	216.6	227.1	229.6	246.9	247.6	266.9	268.6	287.7	291.3
EPCSRST_N_1	B32	216.1	215.7	224.3	224.8	243.1	243.6	261.8	262.5	280.9	282.3
EPCSRST_N_2	B34	217.4	216.9	226.1	226.4	246.1	246.2	265.6	265.9	285.4	286.0
EPCSRST_N_3	B35	216.8	216.4	224.9	225.1	243.3	243.6	261.7	262.0	280.1	281.3
EPCSRST_N_4	B36	218.1	217.9	228.0	228.3	249.5	249.6	270.5	270.9	291.7	292.7
EPCSRST_N_5	B37	217.7	217.6	226.6	227.1	246.2	246.8	265.5	266.9	285.3	287.3
MONITOR	K23	216.6	215.4	224.4	223.7	242.8	240.3	260.7	257.5	278.6	274.9
PLL_MON	L20	214.8	214.2	222.7	222.4	236.1	237.0	250.9	252.7	266.7	269.3
TOGGLE_MON	L22	214.8	213.7	222.3	221.1	238.5	237.8	254.4	254.1	270.9	270.2

E. Propagation Delay

Table 33 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 33. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
18013	125 krad	0.453	0.457	0.90
18018	125 krad	0.458	0.461	0.68
18031	125 krad	0.466	0.471	1.08
18033	125 krad	0.463	0.470	1.36
18038	125 krad	0.466	0.470	0.97

F. Transition Time

The figures below show the pre-irradiation and post-annealing transitions edges. In each case the radiation induced transition degradation is not observable.

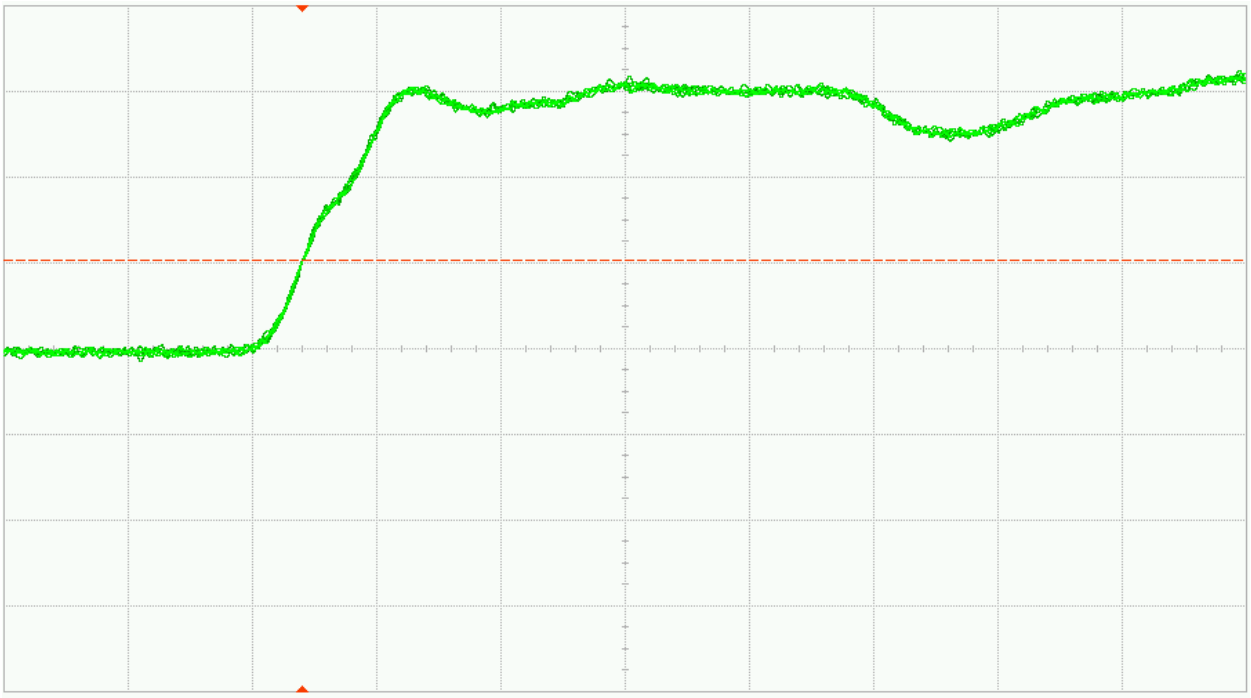

Fig. 27 (a). DUT 18013 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

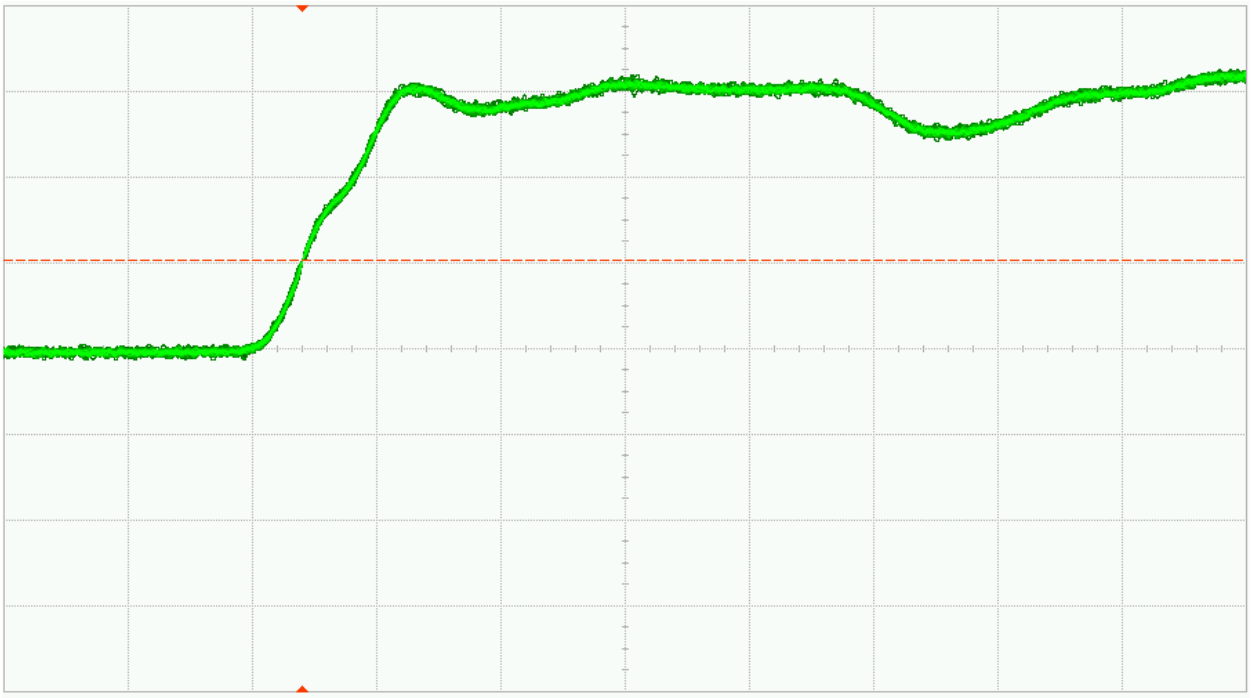

Fig. 27 (b). DUT 18013 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

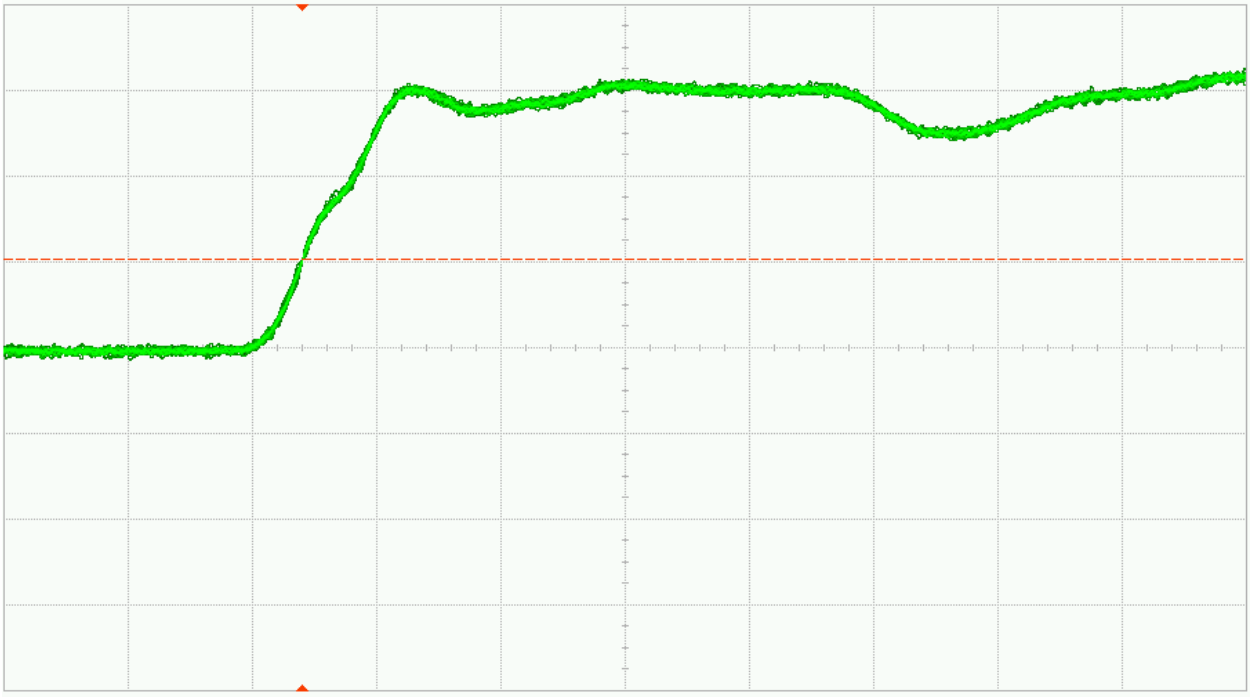

Fig. 28 (a). DUT 18018 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

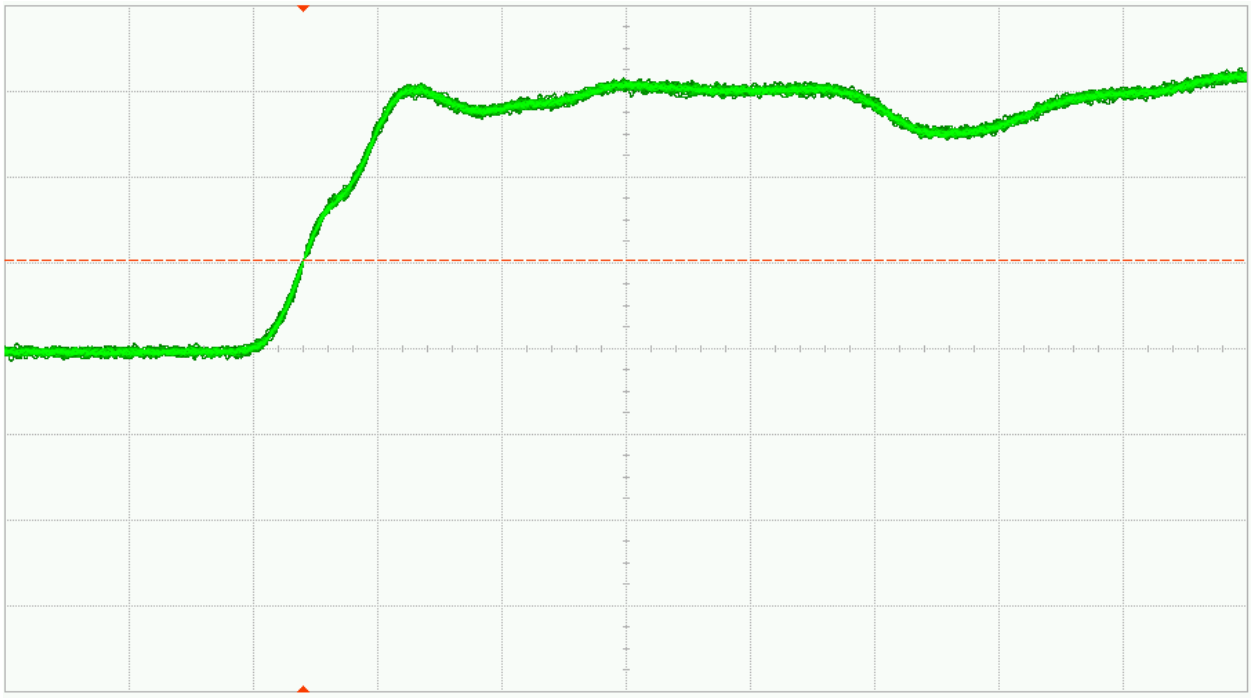

Fig. 28 (b). DUT 18018 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

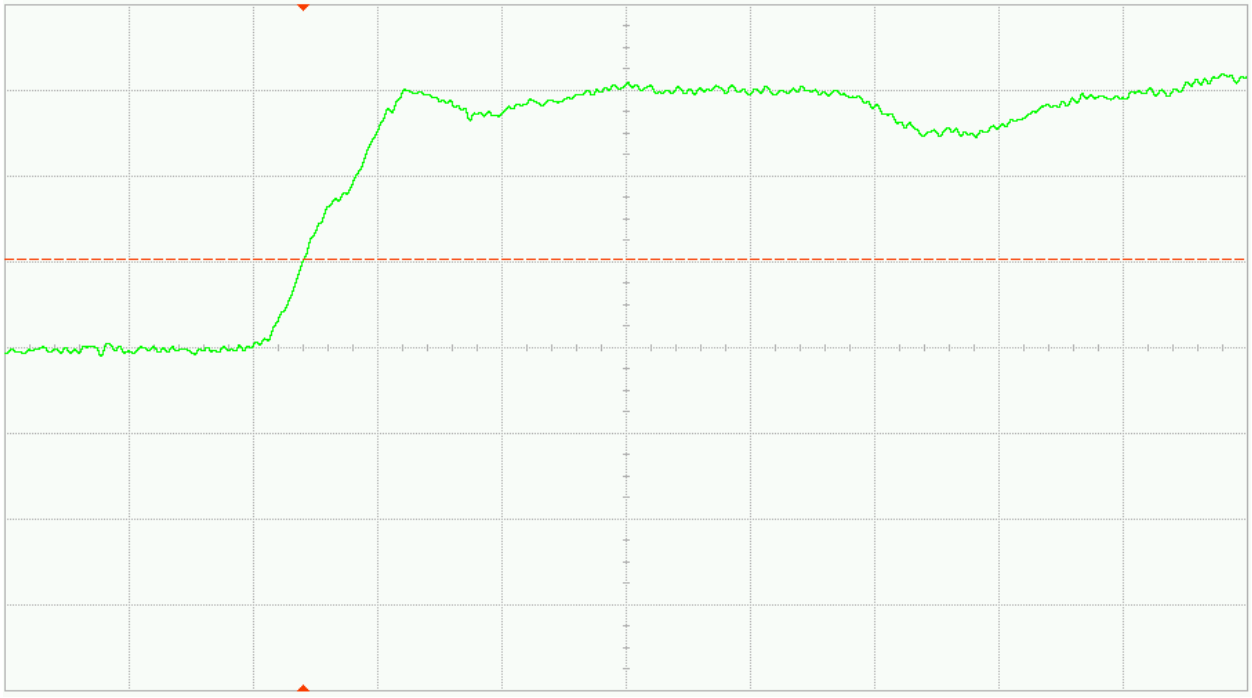

Fig. 29 (a). DUT 18031 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

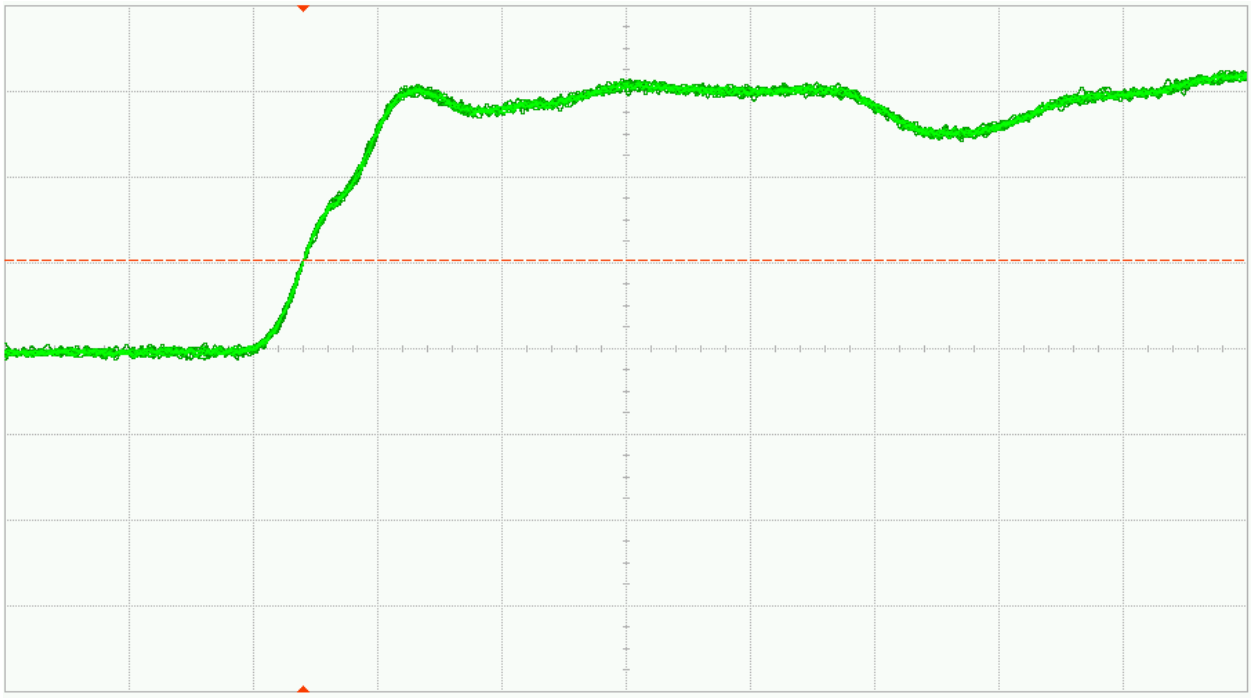

Fig. 29 (b). DUT 18031 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

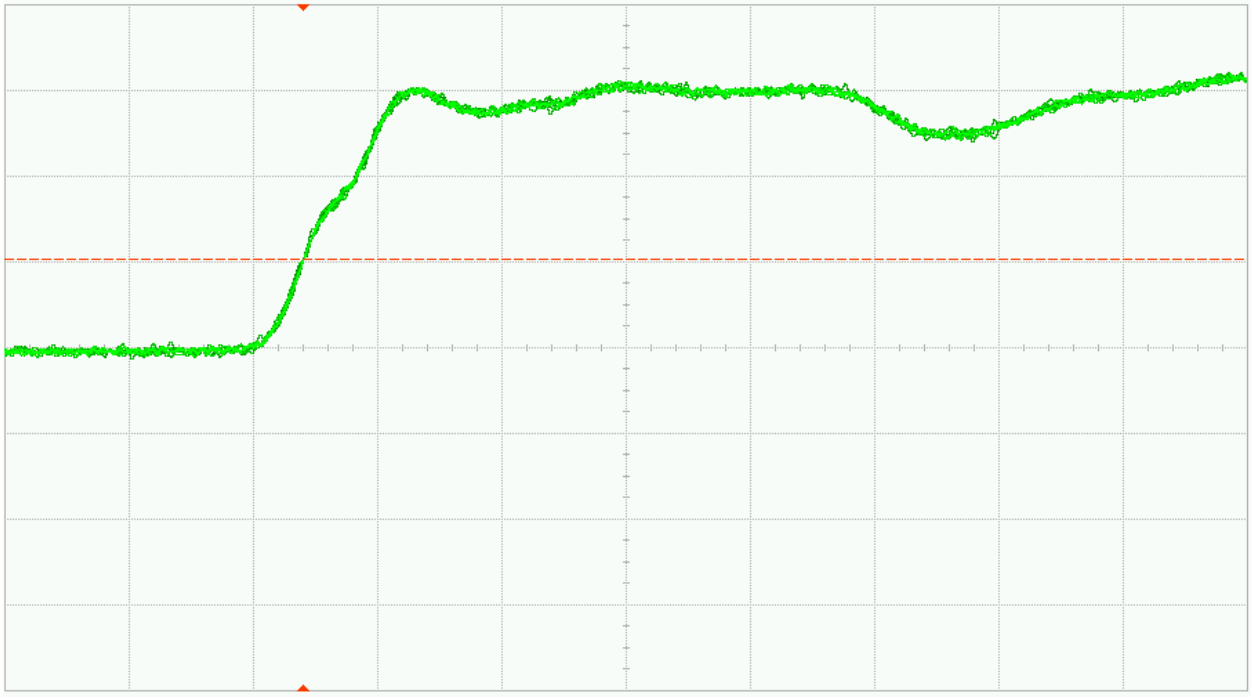

Fig. 30 (a). DUT 18033 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

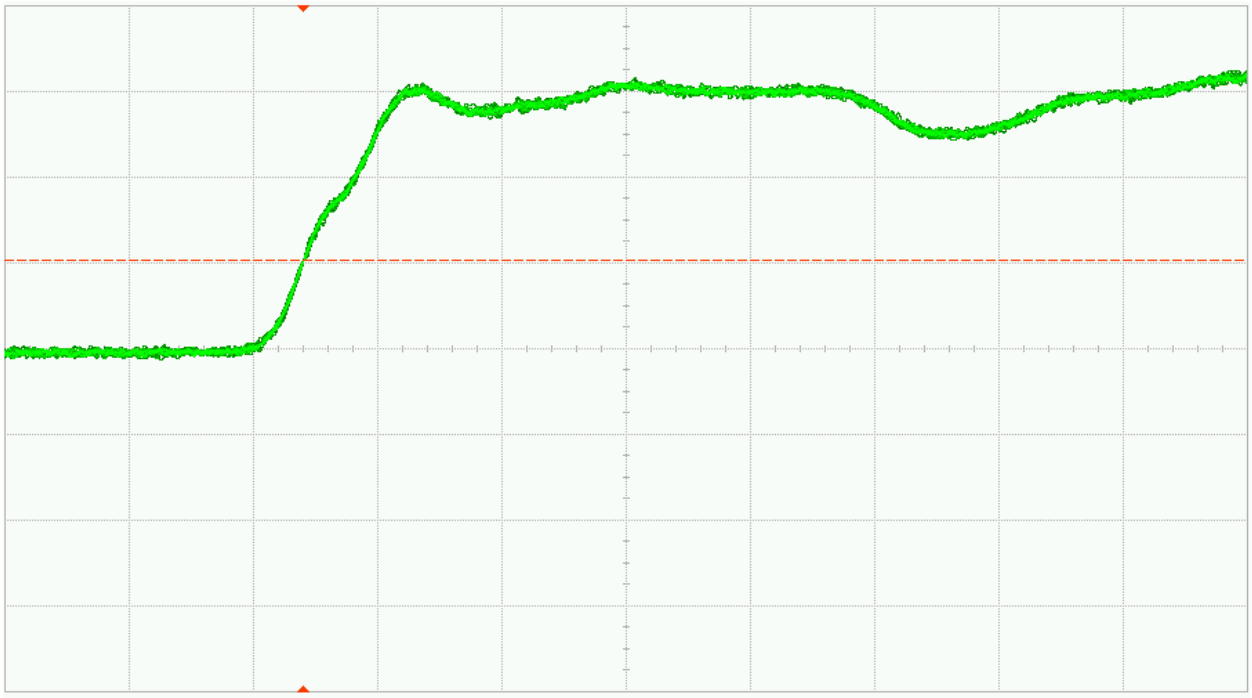

Fig. 30 (b). DUT 18033 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

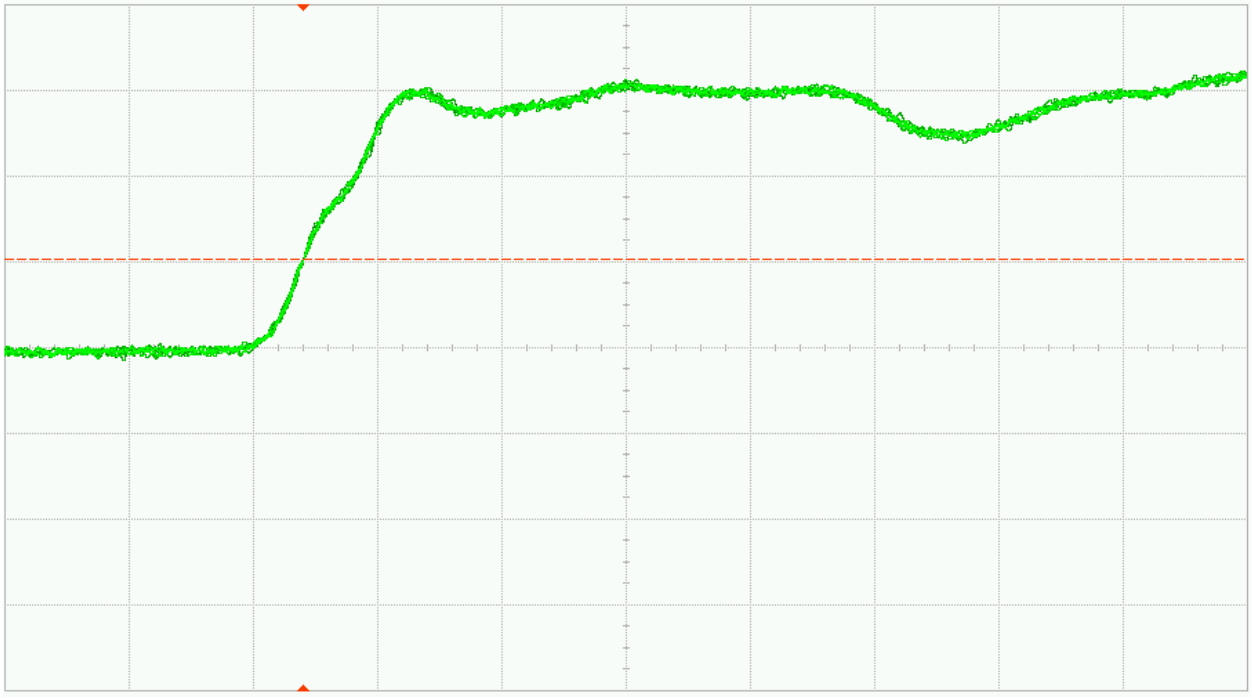

Fig. 31 (a). DUT 18038 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

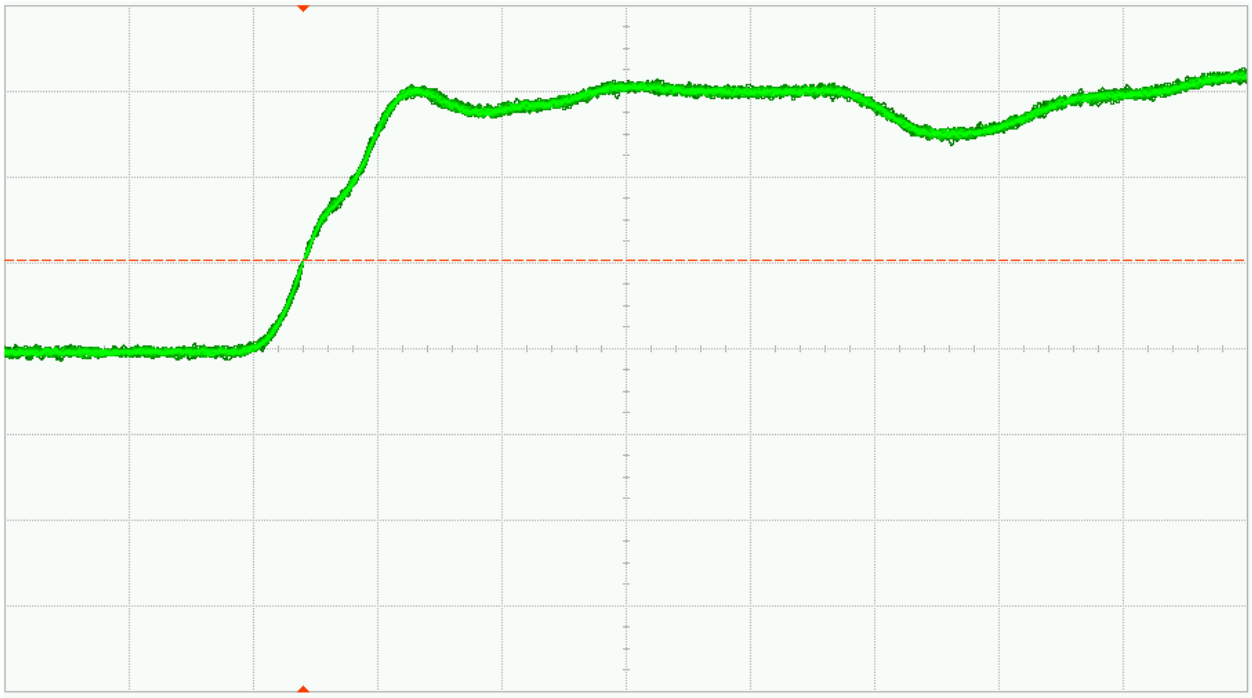

Fig. 31 (b). DUT 18038 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

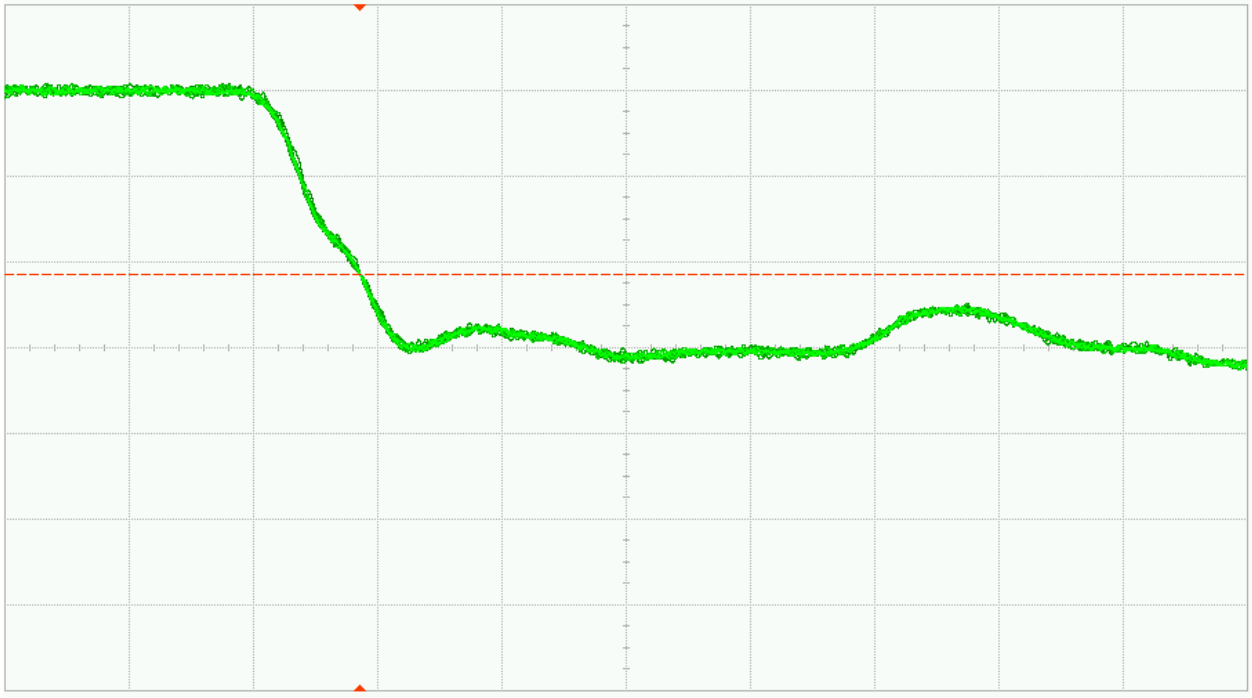

Fig. 33 (a). DUT 18013 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

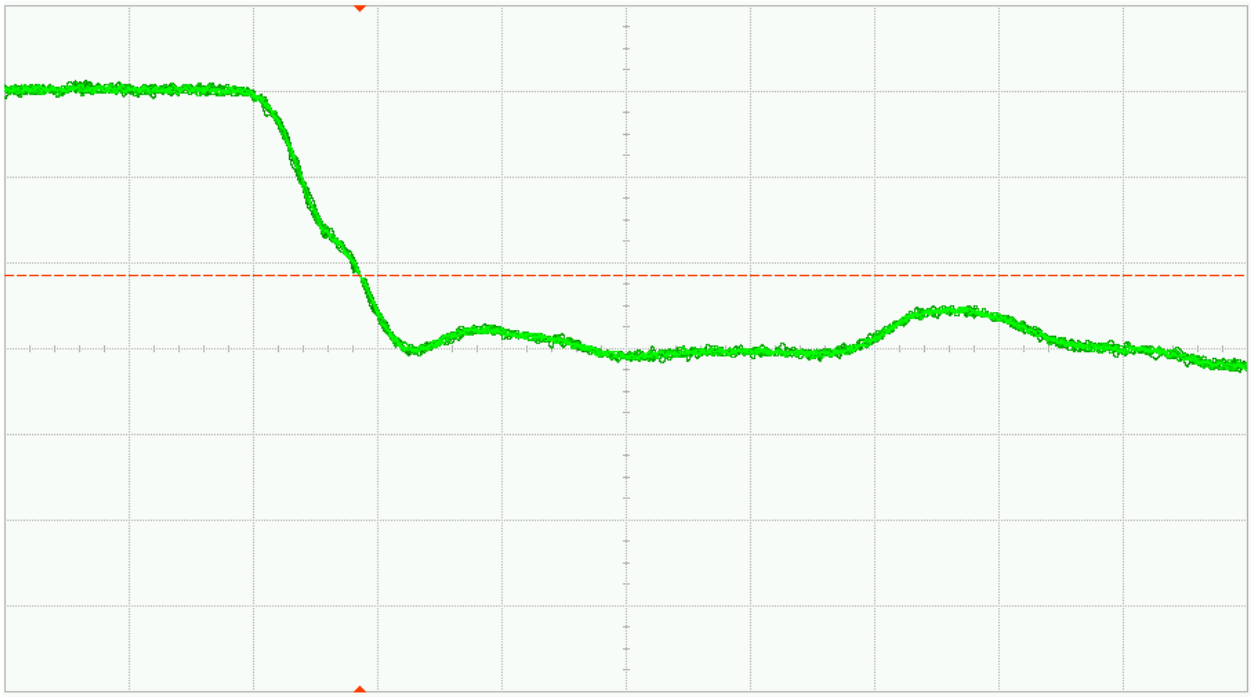

Fig. 33 (b). DUT 18013 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

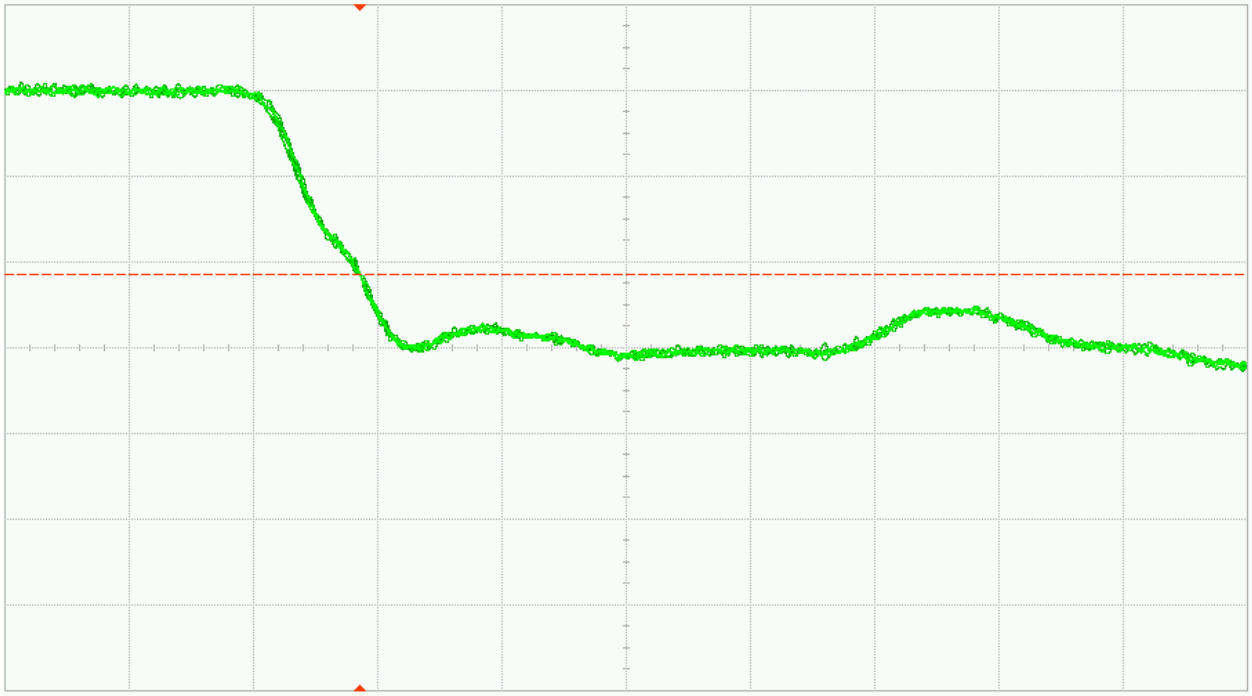

Fig. 34 (a). DUT 18018 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

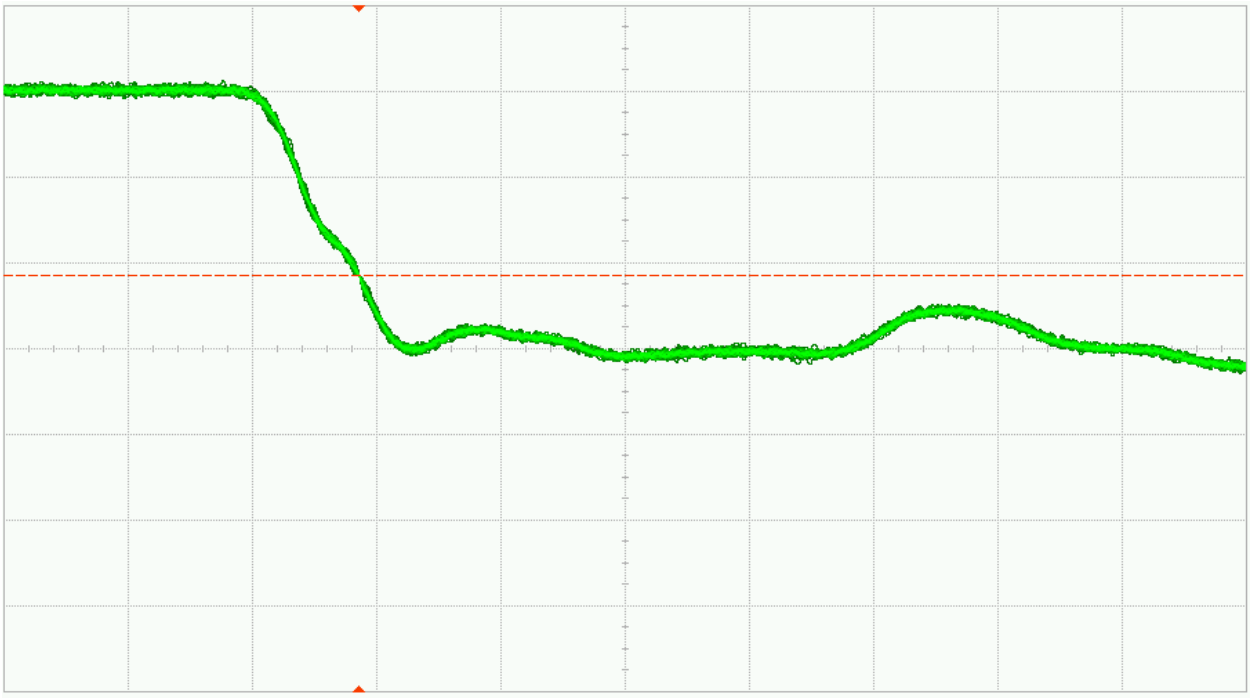

Fig. 34 (b). DUT 18018 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

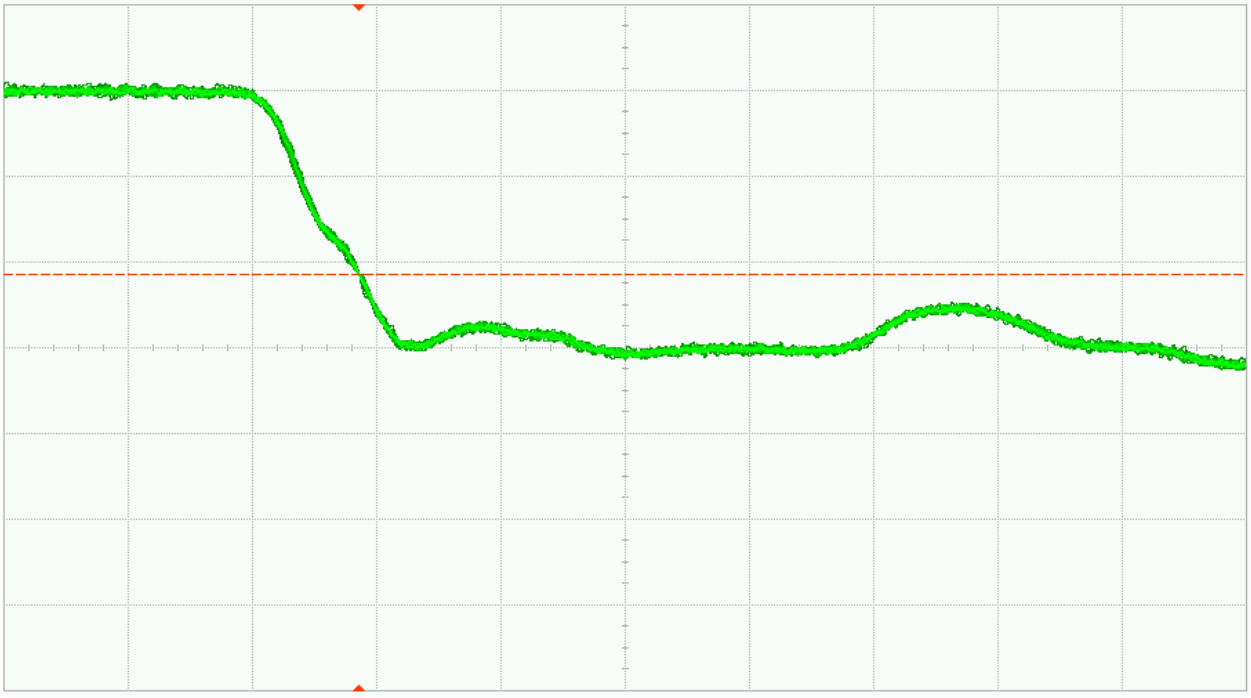

Fig. 35 (a). DUT 18031 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

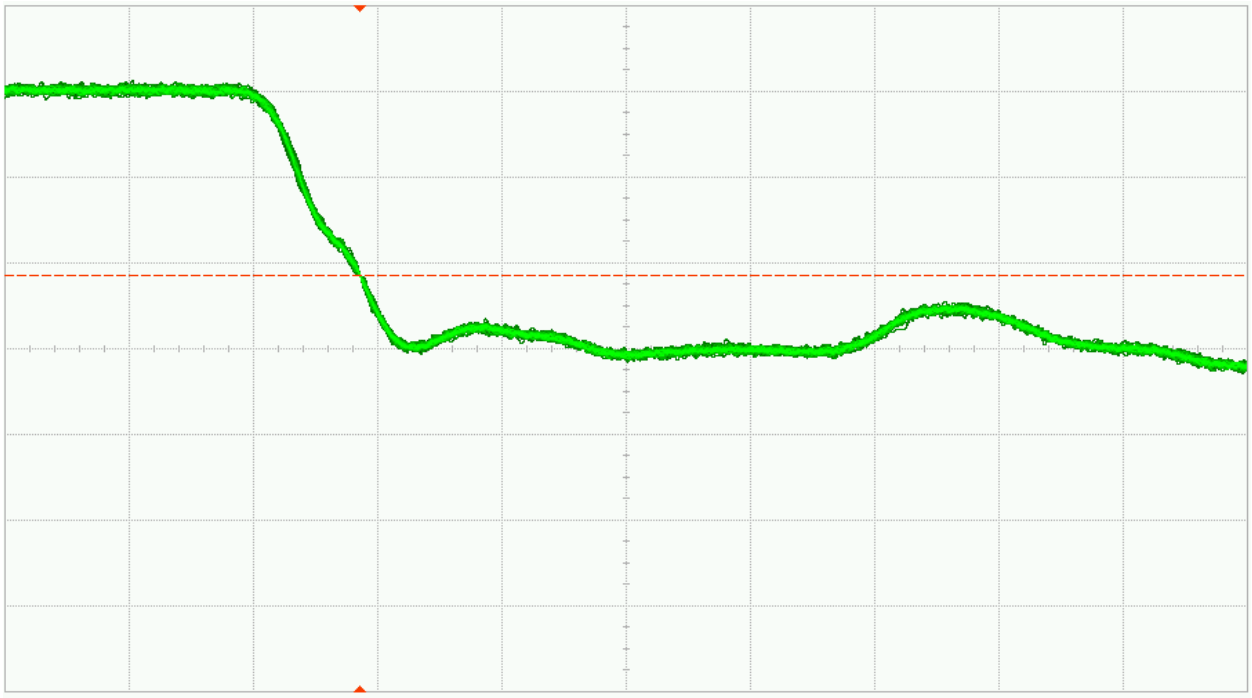

Fig. 35 (b). DUT 18031 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

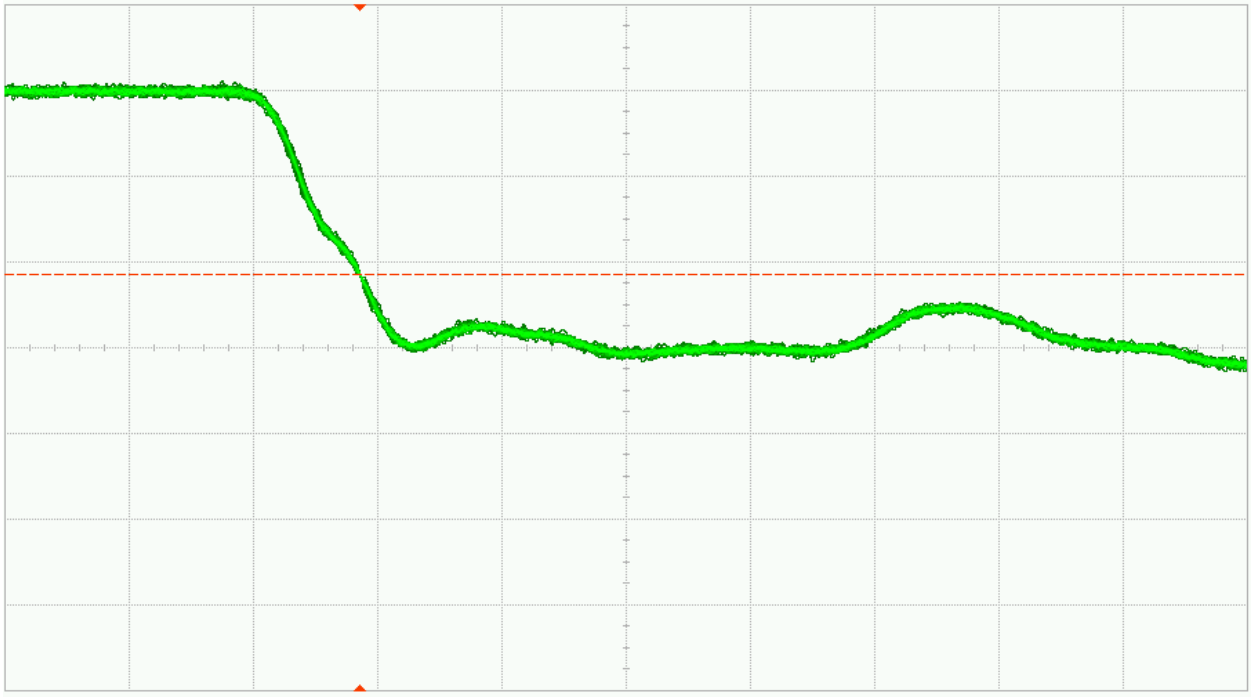

Fig. 36 (a). DUT 18033 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

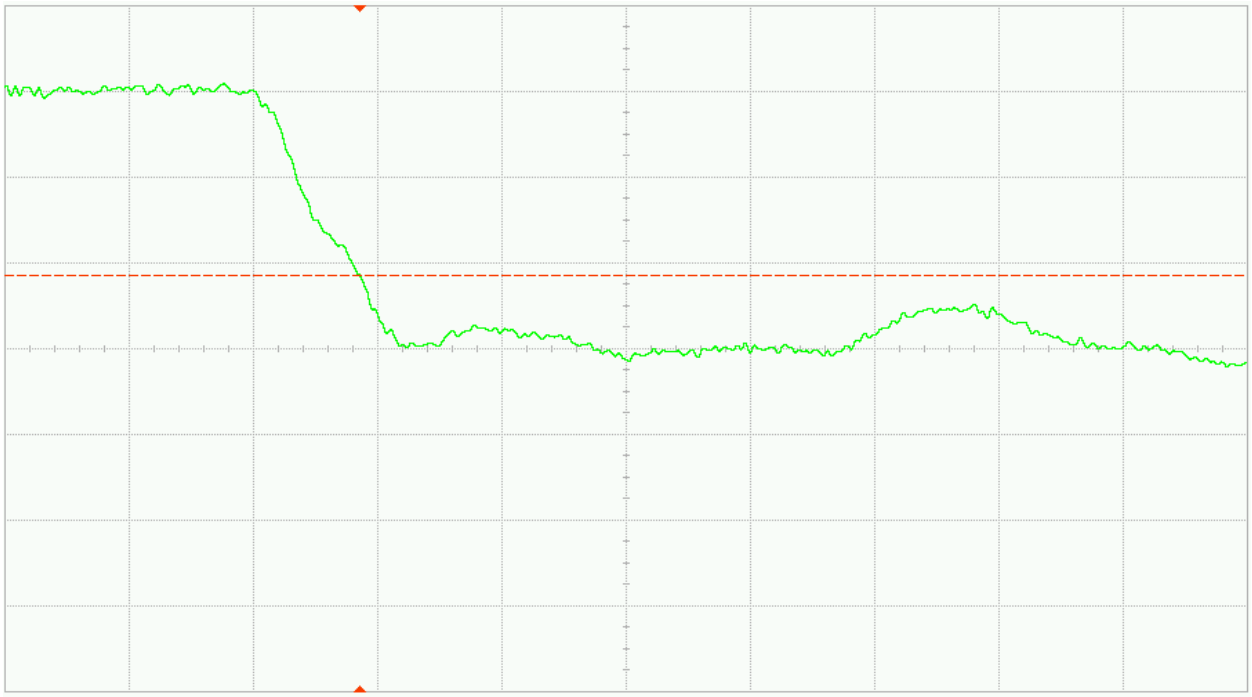

Fig. 36 (b). DUT 18033 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

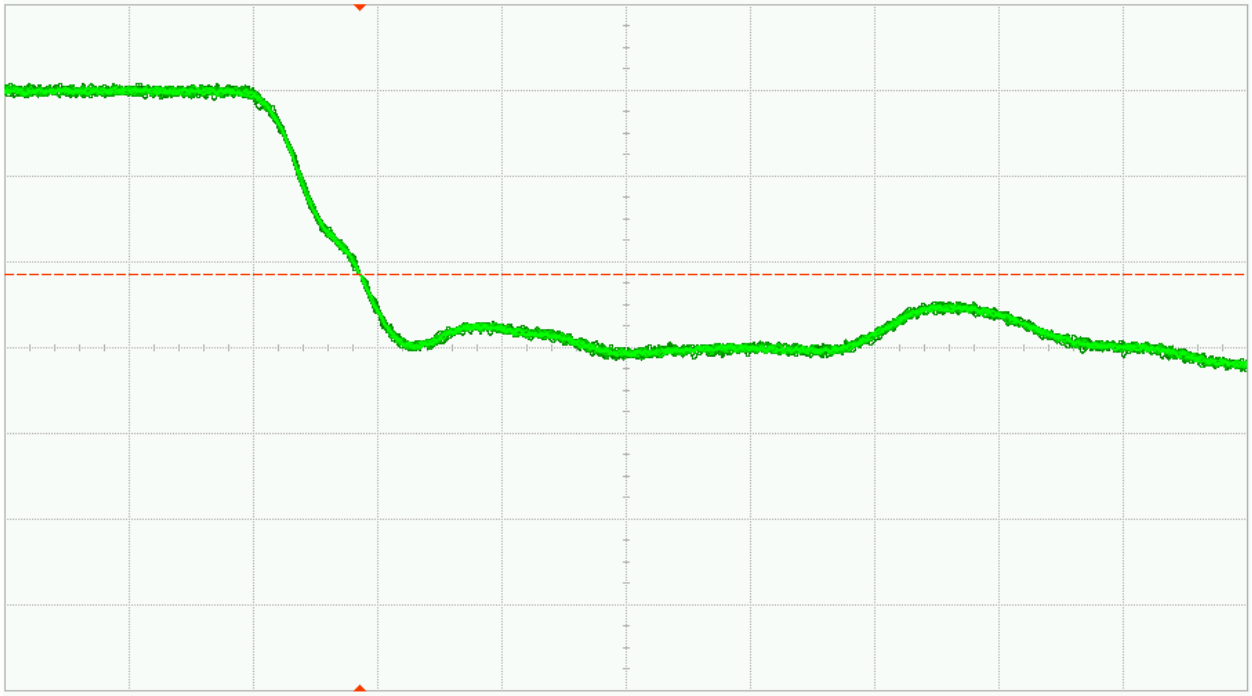

Fig. 37 (a). DUT 18038 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

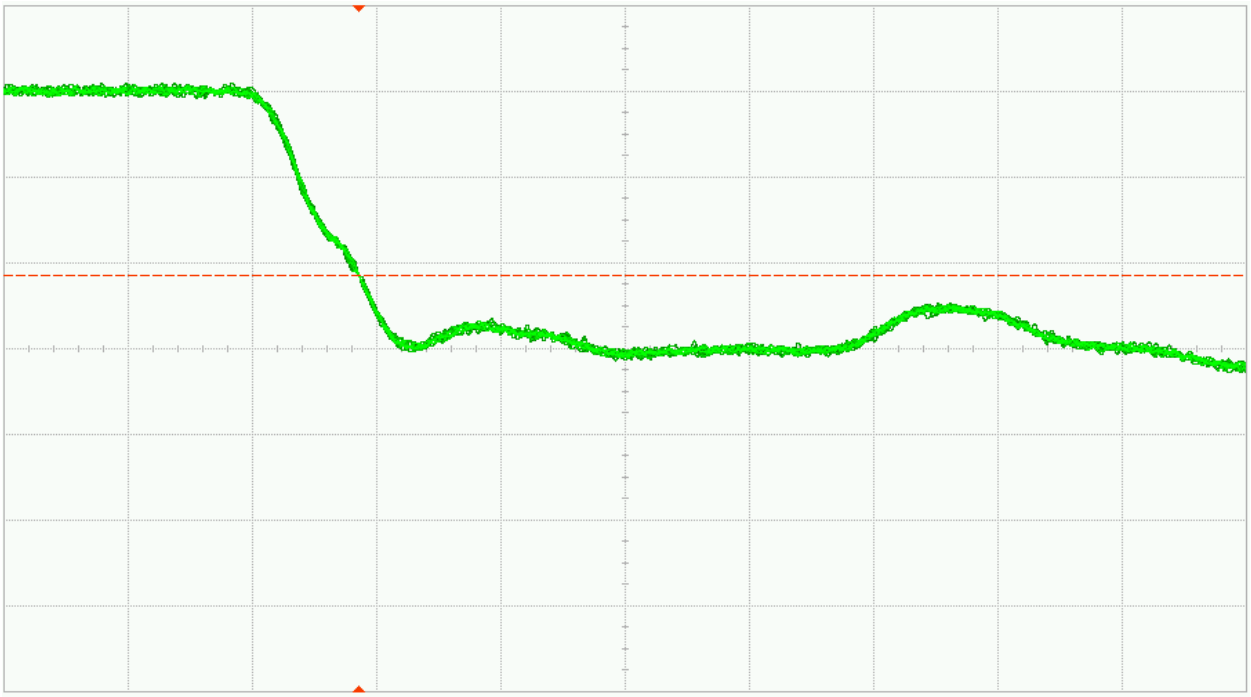

Fig. 37 (b). DUT 18038 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 34. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

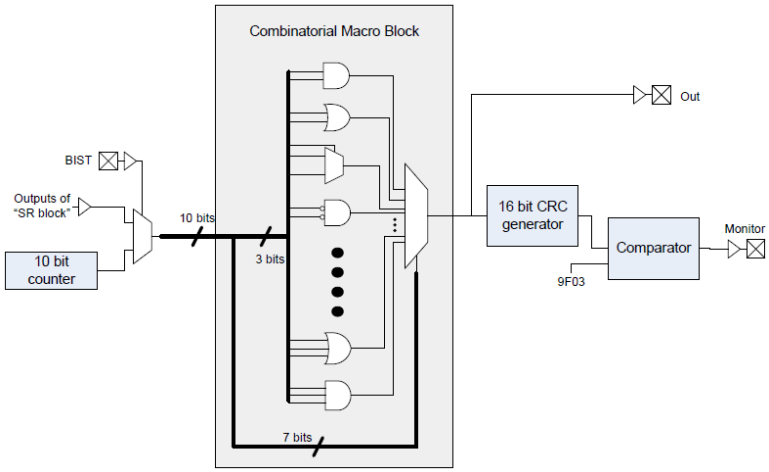

Fig. 38. Combo Block

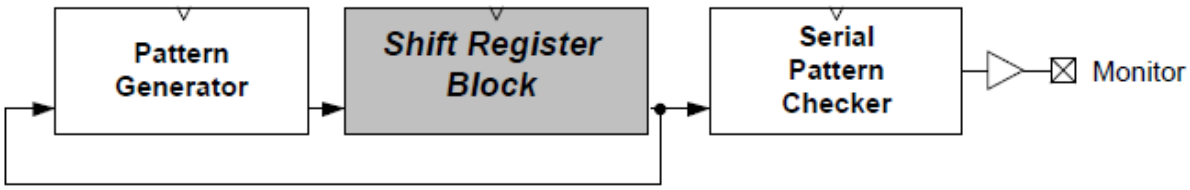

Fig. 39. Shift Register Block

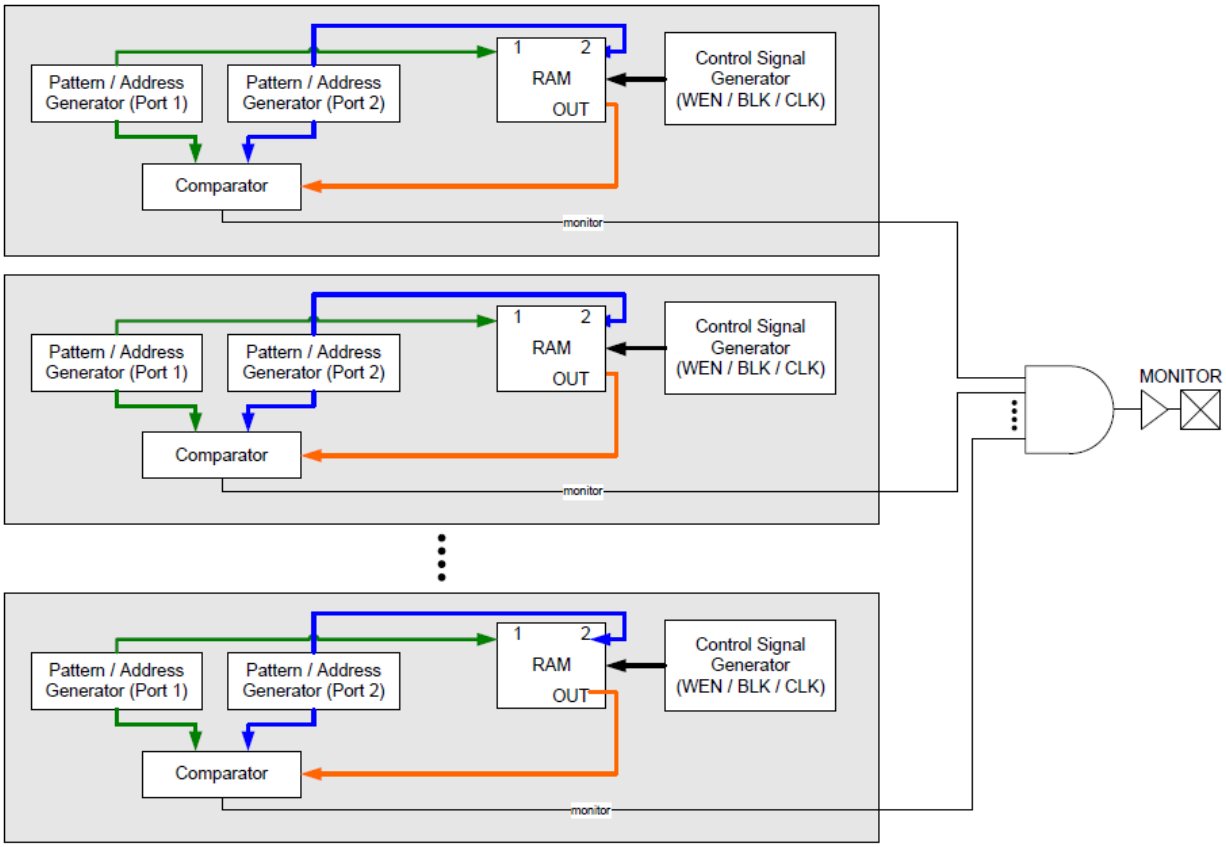

Fig. 40. Embedded Ram Blocks

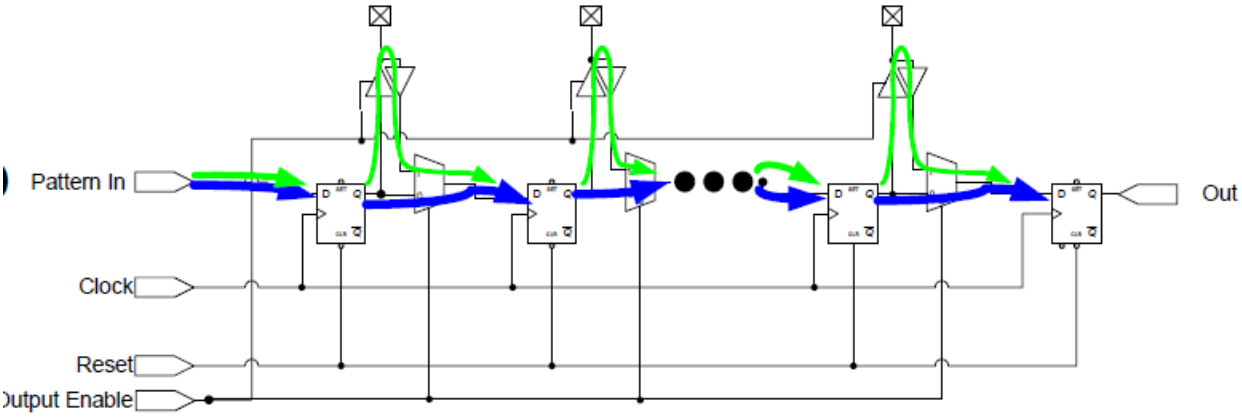

Fig. 41. IO Block

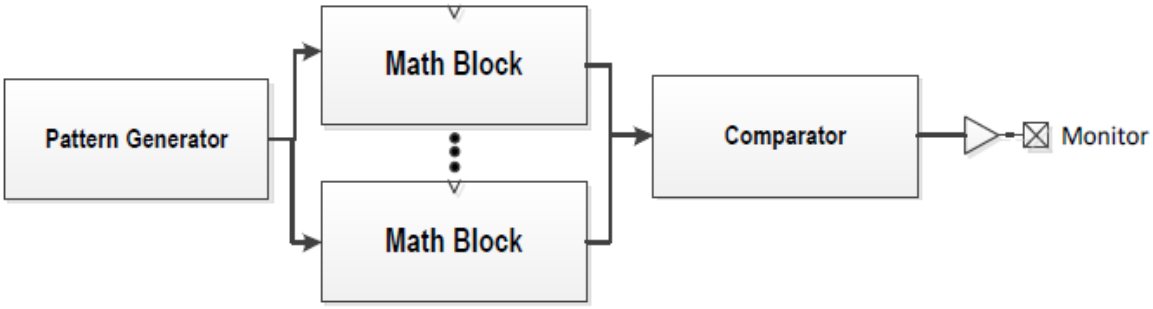

Fig. 42. Math Block

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