

UG0826
User Guide
PolarFire MIPI CSI-2 Transmitter



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 3.0

Revision 3.0 was published in October 2018. In this revision, the document was updated for Libero SoC PolarFire v2.3.

1.2 Revision 2.0

Revision 2.0 was published in September 2018. In this revision, RAW10 data type support is added to the IP, through out the document.

1.3 Revision 1.0

The first publication of this document.

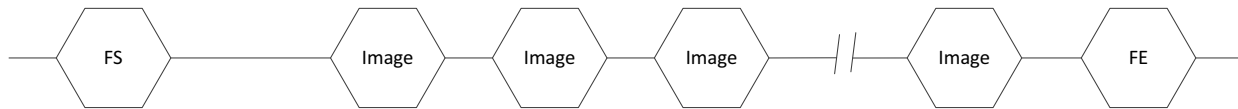
2 MIPI CSI-2 Transmitter

MIPI CSI-2 is a standard specification by Mobile Industry Processor Interface (MIPI) Alliance. The Camera Serial Interface 2 (CSI-2) specification defines an interface between a peripheral device (camera) and a host processor (baseband, application engine). This user guide describes the MIPI CSI-2 transmitter, which encodes the pixel data compliant to MIPI CSI-2 standard. The IP Core supports multi-lane (1, 2, and 4 lanes), RAW8 and RAW10 data types. MIPI CSI-2 transmitter operates in two modes—high-speed mode and low-power mode. In high-speed mode, MIPI CSI-2 supports the transport of image data using short and long packets. Short packets provide frame synchronization and line synchronization information. Long packet provides the pixel information. The sequence of transmitted packets is:

1. Frame start (short packet)
2. Few image data packets (long packets)
3. Frame End (short packet)

One long packet is equivalent to one image data line. The following illustration shows the video data stream.

Figure 1 • Video Data Stream



Note:

FS: Frame Start Packet (short packet)

Image: Pixel data of image embedded in Long Packet

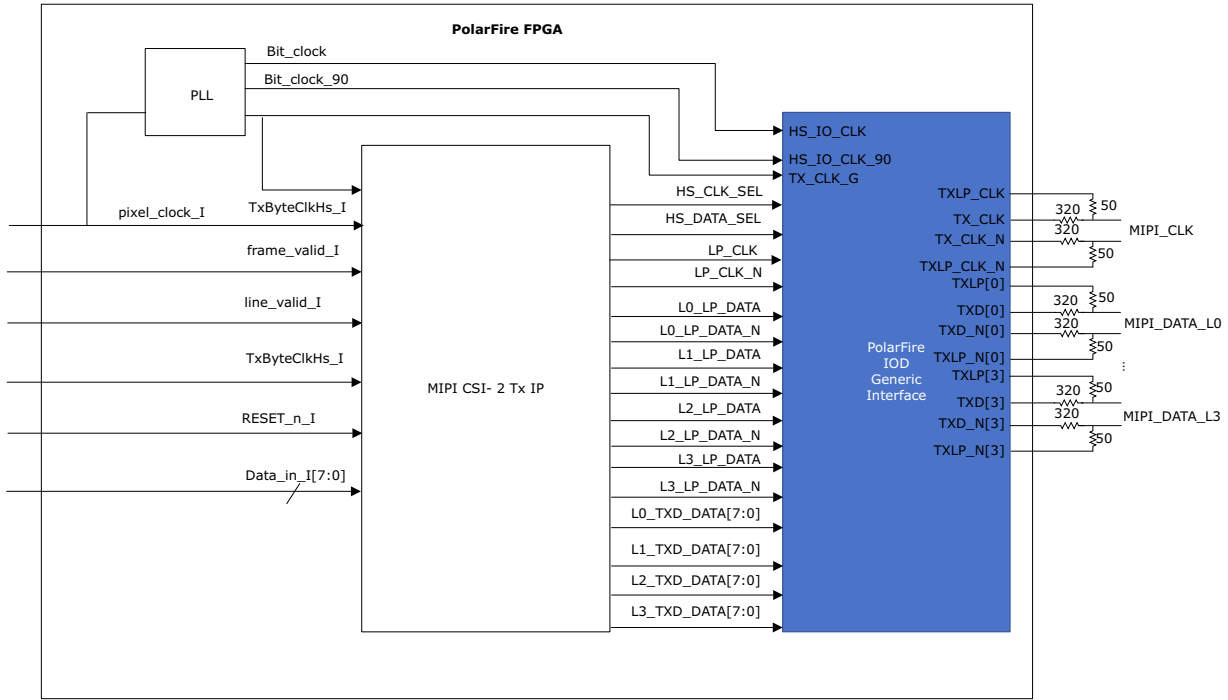
FE: Frame End Packet (short packet)

2.1 Hardware Implementation

The following illustration shows the MIPI CSI2 Transmitter solution that contains the MIPI CSI2 Tx IP. This IP is used in conjunction with the PolarFire® MIPI IOD generic interface block and PLL. The illustration shows the pin connection from the MIPI CSI2 Tx IP to the PolarFire IOG. A PLL is required to generate the TxByteClkHs_I clock (Byte clock). The input clock to the PLL is the Pixel clock. The PLL is configured to produce the TxByteClkHs_I clock, the MIPI bit clocks based on the pixel clock, and the number of lanes used.

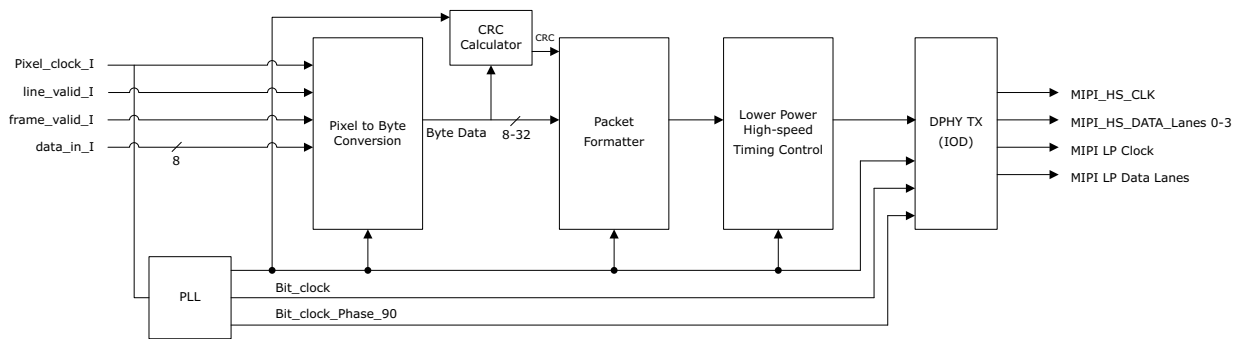
An external resistor network as shown in following figure is needed to accommodate LP and HS mode transitioning on the same signal pairs and also to bring down the voltage swing to 200 mV during HS clock and data transfers.

Figure 2 • Architecture of MIPI CSI-2 Transmitter Solution



The following illustration shows the architecture of MIPI CSI-2 transmitter core.

Figure 3 • Implementation of MIPI CSI-2 Transmitter Core



2.2 Design Description

This section describes the different internal modules of the IP.

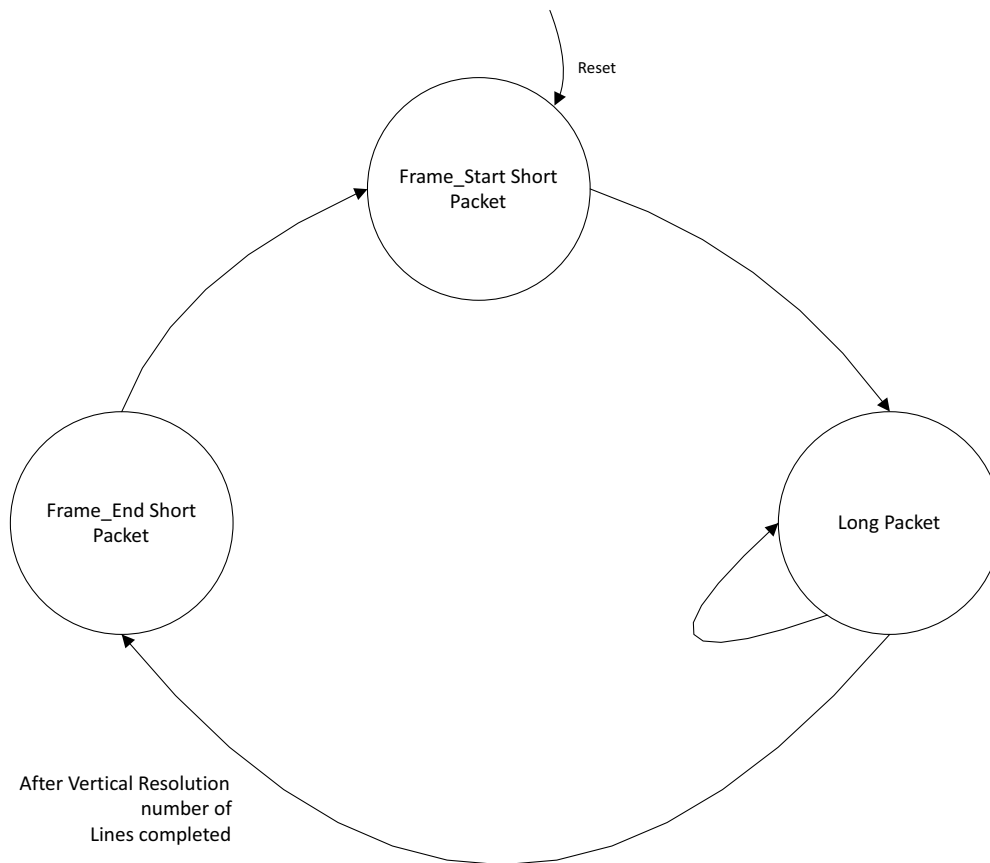
2.2.1 Pixel to Byte Conversion

This module converts the incoming pixel data to bytes based on the number of lanes the IP is configured to. The user is expected to transmit the pixels along with the control signals `line_valid_i`, `frame_valid_i`, and virtual channel number (`vc_i`). It uses a cross clock FIFO to convert the data coming from pixel clock to byte clock domain. It also generates the byte enable signal, which validates the byte data.

2.2.2 Packet Formatter

This module consists of two blocks—Header insertion and lane distribution block. On detecting the control signals (`frame_valid_i`), it transmits the frame start short packet, then long packet with the header inserted and the data from the pixel to byte conversion module. It also generates a `packet_en` signal to validate the MIPI packet data. When vertical resolution number of packets are completed, frame end short packet is generated. It also calculates the error correction code (ECC) and appends to the packet header.

Figure 4 • FSM Implementation of High-Speed Data Generation



2.2.3 PLL

Pixel_clock_i is the input clock with which incoming pixels are sampled. A PLL is used to generate the Byte clock (TxByteClkHs_I) and bit clocks used by the MIPI DPHY block (PolarFire IOD). TxByteClkHs_I must be configured such that the output MIPI CSI2 compliant packets sent on the interface are sampled. The following equations show the relation between Pixel_clock_i and TxByteClkHs_I depending on the number of lanes configured.

$$\text{Pixel_clock_i} = \text{TxByteClkHs_I} \times \text{Number of Lanes} \times 8 \text{ bits per pixel.}$$

$$\text{MIPI bit clock} = 4 \times \text{TxByteClkHs_I}$$

There are two serial clocks—0° and 90° phase shift.

Microsemi supports RAW8 and RAW10 data types. For RAW8 data type, one pixel (8 bits) per clock is transmitted and for RAW10 data type, one pixel (10 bits) per clock is transmitted.

2.2.4 Low Power/High-Speed

When the MIPI packet_en is asserted, transition to high-speed mode follows this sequence: LP-11, LP-01, LP-00, HS0/1. It controls the HS request path and the timing using the parameters based on MIPI DPHY Specification version 1.1. LP request, Escape mode and Turn around modes are not supported.

2.2.5 DPHY TX

This module uses PolarFire IOD generic blocks to convert Byte data to serial data. Gearing Ratio 4 is used to convert the parallel data to serial data. It outputs both HS and LP signals (clock and data). It also controls the switch between HS and LP using the HS_CLK_SEL and HS_DATA_SEL signals.

2.2.6 CRC Calculator

This module uses the bytes generated from the pixel to byte conversion module and calculate the 16-bit CRC for the generated bytes. This 16-bit CRC is sent to the packet formatter, which appends at the end of the long packet.

2.3 Inputs and Outputs

The following table lists the input and output ports of the MIPI CSI2 Tx configuration parameters.

Table 1 • Input and Output Ports of the MIPI CSI-2 Transmitter

Signal Name	Direction	Width	Description
RESET_n_I	Input		Active low asynchronous reset signal to design
Pixel_clock_i	Input		Input clock with which incoming pixels are sampled
TxByteClkHs_I	Input		Tx Byte clock. This clock must be configured such that the pixels sent on the MIPI CSI-2 interface are sampled according to it
vc_i	Input	[1:0]	Virtual Channel Identifier.
data_in_i	Input	[g_DATAWIDTH-1:0]	Input Pixel Data. Supports RAW8 and RAW10 data types
frame_valid_i	Input		Asserts high for every valid frame
line_valid_i	Input		Asserts high when the valid packet is available
L(0-3)_LP_DATA	Output		Low power data (P side)
L(0-3)_LP_DATA_N	Output		Low power data (N side)
LP_CLK	Output		Low power clock (P side)
LP_CLK_N	Output		Low power clock (N side)
L(0-3)_TXD_DATA	Output	[7:0]	Lane0 to Lane3 transmit bytes.

Table 1 • Input and Output Ports of the MIPI CSI-2 Transmitter (continued)

Signal Name	Direction	Width	Description
HS_CLK_SEL	Output		High-speed clock select
HS_DATA_SEL	Output		High-speed data select

2.4 Configuration Parameters

The following table lists the description of the configuration parameters used in the hardware implementation of MIPI CSI-2 transmitter block. These are generic parameters and can vary based on the application requirements.

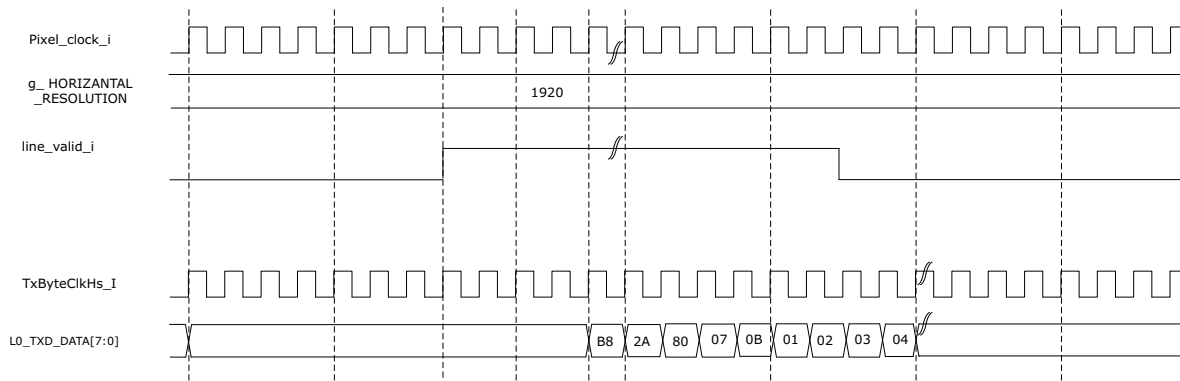
Table 2 • Configuration Parameters

Name	Description
g_DATAWIDTH	Input pixel data width. Supports 8-bit and 10-bit
g_HORIZONTAL_RESOLUTION	Active horizontal resolution
g_LANE_WIDTH	Number of MIPI lanes
g_TX_BYTE_FREQ	TxByteClkHs_I value derived by the calculation
g_FREE_RUNNING_CLOCK	Continuous clock mode select

2.5 Timing Diagrams

2.5.1 Long Packet

The following illustration shows the timing waveform of long packet for one lane.

Figure 5 • Timing Waveform of Long Packet

2.6 Resource Utilization

The following table lists the resource utilization of a sample MIPI CSI-2 transmitter core implemented in a PolarFire MPF300T-1FCG1152I device for RAW8 four lanes configuration.

Table 3 • Resource Utilization of the MIPI CSI-2 Transmitter

Cell Usage	Description
DFFs	906
4-input LUTs	900
LSRAM	11