ER0215

Errata

PolarFire FPGAs: MPF300XT Devices

May 2018

Microsemi

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in May 2018. It was the first publication of this document.

2 Errata for PolarFire MPF300XT

The PolarFire® MPF300XT FPGA devices are subject to the limitations described in this errata. This document contains updated information about any known issues and provides the available limitations and workarounds. Errata dependencies may exist between silicon device revisions and specific support by Libero® PolarFire SoC software versions. Contact Microsemi Technical Support for more information.

2.1 Device Revisions

The following table lists the device revisions and package offerings listed, unless specified otherwise.

Table 1 • Sample Revisions Released per Device

Devices	Packages	Revisions
MPF300XT	FCG1152, FCG784, FCG484	0

Table 2 • PolarFire XT FPGA Device Options

Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C– 100 °C	STD	–1	Transceivers T	Lower Static Power "L"	Data Security "S"
MPF300XT	Yes	Yes	Yes	Yes	Yes	N/A	N/A

See, DS0143: PolarFire FPGA MPF300XT Datasheet, for specifications.

2.2 PCB Designs

For information about how to determine proper signal pinout, see UG0726: PolarFire FPGA Board Design User Guide. The proper signal pinout is required for all clocking, transceiver, and FPGA pin recommendations.

3 Errata Descriptions and Workarounds

The following table lists brief descriptions of errata items. The following sections provide detailed descriptions of device erratas and applicable workarounds.

Table 3 • Summary of PolarFire FPGA Errata

Description	MPF300XT
Power supply sequencing	*
Hot-swapping/cold sparing support on any I/Os powered by VDDI3 or XCVR_CLK_VDD banks	*
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JTAG programming times	*
SSTL18I I/O standard is not supported for PF_XCVR_REF_CLK	*
PCIe ECC detection	*
JTAG TCK duty cycle	*
Transceiver PCS mode 64b/6xb limitations	*
Transceiver lock to reference clock limitation	*
Limitations for ACJTAG IEEE 1149.6 for transceiver transmit pins	*
Incorrect transceiver RXPLL behavior /LANEx_RX_READY pin behavior	*
Low common mode I/O types not supported	*
Auto-update trigger	*
LPDDR electrical compliance	*
VDD power estimation	*
PCIe protocol compliance test with LeCroy exerciser	*
GPIO on-die termination	*
Unsupported Features	
System controller suspend mode	*
Flash*Freeze mode	*
Temperature voltage sensor (TVS)	*
Device zeroization	*
Digest check	*
Tamper detection	*
PCIe Gen2 electrical compliance for x2 and x4 links	*
Automated DFE support (contact Microsemi)	*

Description	MPF300XT
Feature Clarifications	
Memory interfaces	List of currently supported memory interfaces with MPF300XT devices and Libero PolarFire SoC V2.1 software
Supported transceiver protocols	List of currently supported transceiver protocols with MPF300XT devices and Libero PolarFire SoC V2.1 software

Note: * indicates that the errata exists for that particular device and revision number.

Note: X indicates that the errata is removed and no longer exists for that particular device and revision number (based on additional details).

3.1 Power Supply Sequencing

The engineering sample must have the power-on sequence as follows:

1. V_{DD} to V_{DD} operational minimum.
2. V_{DD25} to V_{DD25} operational minimum.
3. V_{DDI} and V_{DDAUX} must be powered up any time before V_{DD18} or simultaneously with V_{DD18}, if supplied from same power source. If V_{DDI} and V_{DDAUX} are not tied to same voltage rail, then V_{DDI} should be powered up before V_{DDAUX}.
4. V_{DD18} (V_{PP}) must be the last major supply in the power-up sequence. Other supplies that are not mentioned, such as power supplies related to transceivers, do not have mandatory sequence requirements.

The V_{DD25} power supply can draw large currents at power-up or power cycling if the correct sequence is not followed.

For more information about the operational minimum voltages, see the DS0143: PolarFire FPGA MPF300XT Datasheet. Observe the power supply ramp rates specified in the datasheet. Sequencing will not be required for production of MPF300T devices.

3.2 Hot-Swapping/Cold Sparing Support on any I/Os Powered by VDDI3 or XCVR_CLK_VDD Banks

This feature is not supported on any I/Os powered by V_{DDI3} or the transceiver reference clock input pins, including the following list of pins.

- SDO
- SDI
- FF_EXIT_N
- IO_CFG_INTFK
- SPI_EN
- SCK
- DEVRST_N
- SS
- TCK
- TMS
- TDI
- TDO
- TRSTB
- XCVR_#A_REFCLK_P/N
- XCVR_#B_REFCLK_P/N
- XCVR_#C_REFCLK_P/N

There is no workaround for this issue.

3.3 Hot-Swapping/Cold Sparing on Erased Devices/Unexpected Driven Pins

The following table lists the 35 FPGA IO pins that do not support hot-swapping/cold sparing on erased devices.

Table 4 • Impacted pins on Erased Devices

Bank	GPIO Pins
0	HSIO169PB0, HSIO170PB0, HSIO171PB0, HSIO173NB0
1	HSIO72NB1, HSIO73PB1, HSIO74PB1, HSIO75PB1, HSIO79PB1, HSIO80PB1, HSIO81PB1
2	GPIO244NB2, GPIO246PB2, GPIO247PB2, GPIO248PB2, GPIO26PB2, GPIO27PB2, GPIO28PB2, GPIO32PB2, GPIO33PB2, GPIO34PB2, GPIO35NB2
4	GPIO174PB4, GPIO180PB4, GPIO181PB4
5	GPIO238PB5, GPIO239PB5, GPIO241PB5
6	HSIO62PB6, HSIO63PB6, HSIO64PB6, HSIO68PB6, HSIO69PB6, HSIO70PB6, HSIO71NB

This errata is only applicable to erased parts. Programmed parts do not have the errata. If these pins are used as input or bi-directional buffers, an erased device will actively drive these outputs rather than properly disabling them. For more information about the pin numbers, see the MPF300T/MPF300TS package pin assignment table at https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga.

If the part is not programmed, do not use these pins even if required, for hot-swapping/cold sparing applications.

3.4 Calibration of FPGA I/O Buffers

The FPGA I/O buffers have calibration circuitry to optimize and match the I/O impedance and termination within a system. The calibration occurs every time the device is powered up. After the device power-up, re-calibration is not available on command. The device requires a power-cycle to correctly re-calibrate.

3.5 SmartDebug Live Probe READ Limited Speed/ SmartDebug Active Probe Write

The SmartDebug live probe output cannot toggle faster than 100 MHz. SmartDebug Active Probe write operation is not available. Active Probe read operation functions, as documented.

There is no workaround for this issue.

3.6 Missing Global Clock Connection in XCVR Quad1

Designs cannot utilize two global clocks for XCVR Quad1. Designs have access to only one global clock on Quad1.

In the Libero SoC PolarFire transceiver lane configurator, the user can select the clock resources used for transmit, receive, and global or regional clocks. For lanes assigned to Quad1, only a single global connection is available. This implies that only one lane in that quad, and one direction of that lane can select global in this interface. Therefore, the clocks assigned to LANE#_RX_CLK_[G] and LANE#_TX_CLK_[G] are limited to one across all lanes in a quad.

3.7 Inefficient Usage of Asynchronous Dual-Port LSRAM Blocks

For LSRAM blocks, configured as asynchronous dual-ports, when port A is greater than x20, twice the number of required LSRAM blocks are used. Two 1K × 20 LSRAM blocks are automatically instantiated by Libero SoC PolarFire to implement the single 512 × 40 LSRAM.

3.8 GPIO IOCDR SGMII

IOD CDR interfaces cannot be used with a > 0 ppm offset. For SGMII, the PHY device and PolarFire IOD CDR must use the same reference clock. SGMII interfaces using transceivers are not affected by this limitation. SGMII can be implemented with IOCDR using 0 ppm or a common clock using the same clock configuration for both Tx and Rx clocks.

3.9 HSIO and GPIO Drive Strength

HSIO and GPIO drive strength deviates by up to ±20% from the datasheet specifications.

There is no workaround for this issue.

3.10 Voltage Reference Sensitivity Issue

There is a voltage reference sensitivity issue with HSIOs when V_{DD18} and V_{DD25} supply voltage rail separation is too large. This effects the HSIO buffer banks only.

This issue is managed by reducing the separation between V_{DD25} and V_{DD18}. For example, when V_{DD25} is maximum, then V_{DD18} needs to be maximum or when V_{DD25} is typical, then V_{DD18} needs to be typical. If V_{DD18} and V_{DD25} are minimum and the other maximum (respectively), it will influence the effectiveness of the voltage references of the HSIO banks, preventing proper functioning of I/O buffers.

3.11 LVDS VOS Output Common Mode Specification

The LVDS VOS output common mode specification can vary as much as 175 mV below the datasheet specification.

3.12 Transceiver Polarity Inversion

There is no programmable receiver polarity inversion possible on the transceivers for 8b10b, 64b6xb, and PMA modes.

There is no workaround for this issue.

3.13 JTAG Programming Times

FPGA programming using the FlashPro4 or 5 programming cable exceeds the current datasheet programming specification. This also impacts programming times of external SPI flash devices with PolarFire using the FlashPro cable.

For more information regarding actual programming specifications, see DS0143: PolarFire FPGA MPF300XT Datasheet.

This is not a MPF300XT device limitation. The speed is due to the programming cable and will be addressed in a subsequent release of the new FlashPro hardware.

3.14 SSTL18I I/O Standard Not Supported for PF_XCVR_CLK

The SSTL18 I/O type is not supported in the PF_XCVR_REF_CLK input pins, as shown in the UG0677: PolarFire FPGA Transceiver User Guide.

LVDS25, HCSL25, and LVCMOS25 I/O types can be used as alternative inputs.

3.15 PCIe ECC Detection

The embedded ECC functions of the PCIe core; that provide indicators for single-error correction (SEC) and double-error detection (DED) and data detection, are improperly functioning. These flags are tied to the incorrect operation of PCIE_#_M_RDERR/WRERR and PCIE_#_S_RDERR/WRERR pins of the PCIe embedded core.

The error-correcting logic is functional. The SECDED status indicators are incorrect.

3.16 JTAG TCK Duty Cycle

The minimum and maximum specifications for JTAG TCK duty cycle, deviate from the datasheet values of 25 MHz TCK with 45/55% duty cycle.

3.17 Transceiver PCS Mode 64b/6xb Limitations

The 64-bit data bus of the fabric interface for mode 64b6xb is permitted for the lanes, Q0 LANE{0, 1, 2, 3} and Q{1-5} LANE{0,2}. The 32-bit data bus of the fabric interface can be used on all lanes of all transceiver quads.

3.18 Transceiver Lock to Reference Clock Limitation

The RX_CLK will stop for a specific period of time in BMR mode, when the user changes the mode to lock-to-reference-clock-mode using control pins from the FPGA fabric.
The minimum period of time is 1,024 REFCLK cycles and the maximum is 10,240 REFCLK cycles over the REFCLK frequency range of 100 MHz–312 MHz.

3.19 Limitations for ACJTAG IEEE 1149.6 for Transceiver Transmit Pins

For transceiver transmit pins, the following ACJTAG IEEE 1149.6 limitations exist.

- The instruction EXTEST_PULSE actually implements EXTEST_TRAIN instruction.
- The transceiver transmitter transmits signals at very low amplitude during any AC or DC JTAG instructions.

3.20 Incorrect Transceiver RXPLL Behavior/LANEx_RX_READY Pin Behavior

The transceiver LANEx_RX_READY pin toggles when the Rx signal is open or disconnected, or while an out-of-range condition occurs. For example, incorrect Rx serial data rates, with serial input data > 1.7% away, is considered out of range.

Initially the RX CDR Lock may not lock with missing or bad data stream. A work-around is available for situations where invalid data causes this condition. Contact Microsemi for work around.

3.21 Low Common Mode HSIO Not Supported

Low Common Mode HSIO is not supported in PolarFire XT devices. Libero PolarFire SoC software allows for the selection, but, the device does not support it. This does not impact GPIO.

3.22 Auto-Update Trigger

The system controller triggers auto-update when the design version is not equal to current design version.

MPF300XT auto-update criteria is; that the system controller starts auto-update, if the design version in the bit stream is greater than the design version in the device.

3.23 LPDDR3 Electrical Compliance

LPDDR3 electrical compliance per the JEDEC JESD79-3E and JESD79-3-1 DDR3 SDRAM specifications are not completely optimized with designs implemented with the Libero software.

3.24 VDD Power Estimation

The PolarFire power estimator (v3e) is currently optimistic with regard to the estimated V_{DD} static power. It is expected that designs utilizing MPF300XT silicon can have a 20% higher static current on the V_{DD} power supply compared to the provided estimation.

3.25 PCIe Protocol Compliance Test with LeCroy Exerciser

PolarFire device testing for PCIe Compliance with a Lecroy Exerciser reports a failure for a PTC test related to REPLAY_BUFFER.

However, PTC test conducted on the Keysight Exerciser passed successfully.

PolarFire met full compliance at the PCISIG Compliance Workshop #101 and entry into the integrators list.

PTC Test 52-20 (LinkRetrainOnRetryFail) fails in the LeCroy Testing suite. Root-cause is that PCIe Controller executes some of the second-round replays prior to, rather than after, link re-training.

Functional Impact to this issue is low because no TLP is lost due in fact to the built-in Replay Mechanism required by the PCIe Base Specification. Replays will occur both before and after link re-training as long as TLP is not acknowledged.

3.26 GPIO On-Die Termination

The 20 Ω and 30 Ω ODT for GPIO SSTl15I and SSTL15II settings should not be used. Instead use the 40 Ω or greater settings only.

3.27 Unsupported Features

The following list of features are not supported in PolarFire XT devices.

- System Controller suspend mode
- Flash*Freeze mode
- Temperature voltage sensor (TVS)
- Device zeroization
- Digest check
- Tamper detectors
- PCIe Gen2 electrical compliance for x2 and x4 links. Compliance tested for x1 Link only
- Automated DFE support
- Contact Microsemi for DFE support
- Current support is limited to 10.3 Gbps and below. Contact Microsemi for solutions, outside the support listed in the UG0677: PolarFire FPGA Transceiver User Guide.

4 Supported Memory Interfaces

Double-data-rate (DDR) memory interface capabilities deviate from the specifications published in the DS0141: PolarFire FPGA Datasheet and UG0676: PolarFire FPGA DDR Memory Controller User Guide.

The following table highlights the current DDR3 and DDR4 capabilities per device and package combinations with all MPF300XTdevices.

Table 5 • DDR Memory Interfaces

Package	IO Type	Edge_Anchor[1]	Memory Type	Interface Width	–1 SPD (Mbps)	STD (Mbps)
FCG484	HSIO	NORTH_NW	DDR3	up to x16	1333	1066
FCG484	HSIO	NORTH_NW	DDR3	x32, x40	1066	800
FCG484	HSIO	NORTH_NE	DDR3	up to x16	1333	1066
FCG484	HSIO	NORTH_NE	DDR3	x16, x32, x40	1066	800
FCG484	HSIO	NORTH_NW	DDR4	up to x16	1600	1333
FCG484	HSIO	NORTH_NW	DDR4	x32, x40	1333	1066
FCG484	HSIO	NORTH_NE	DDR4	up to x16	1600	1333
FCG484	HSIO	NORTH_NE	DDR4	x32, x40	1333	1066
FCG784	HSIO	NORTH_NE	DDR3	up to x16	1333	1066
FCG784	HSIO	NORTH_NE	DDR3	x16, x32, x40, x72	1072	800
FCG784	HSIO	NORTH_NW	DDR3	up to x40	1333	1066
FCG784	HSIO	NORTH_NW	DDR3	x64, x72	1066	800
FCG784	HSIO	NORTH_NW	DDR4	up to x40	1600	1333
FCG784	HSIO	NORTH_NW	DDR4	x64, x72	1333	1066
FCG784	HSIO	NORTH_NE	DDR4	up to x16	1600	1333
FCG784	HSIO	NORTH_NE	DDR4	x32, x40, x64, x72	1333	1066
FCG1152	HSIO	NORTH_NW	DDR3	up to x72	1333	1072
FCG1152	HSIO	NORTH_NE	DDR3	up to x16	1333	1072
FCG1152	HSIO	NORTH_NE	DDR3	x16, x32, x40, x72	1072	800
FCG1152	HSIO	SOUTH_SE	DDR3	up to x16	1333	1066
FCG1152	HSIO	NORTH_NW	DDR4	up to x72	1600	1333
FCG1152	HSIO	NORTH_NE	DDR4	up to x16	1600	1333
FCG1152	HSIO	NORTH_NE	DDR4	x32, x40, x72	1333	1066
FCG1152	HSIO	SOUTH_SE	DDR4	up to x16	1600	1333

1. Refer to the Package Pin Assignment Tables (PPAT) for information.

5 Supported Transceiver Protocols Exceptions

Transceiver protocol capabilities deviate from the specifications published in the DS0143: PolarFire FPGA MPF300XT Datasheet and UG0677: PolarFire FPGA Transceiver User Guide.

The following table summarizes the transceiver protocols supported by all MPF300XT devices.

Table 6 • Supported Transceiver Protocols

Transceiver Protocol	Details
SGMII/1000BaseX	Transceiver: 1.25 Gbps with CoreTSE IP Core TxPLL SyncE not supported
CPRI	Support for CPRI data rates 1–6
10GBASE-R	Transceiver: 10.3 Gbps with Core10GMAC IP Core TxPLL SyncE not supported IEEE 1588 time stamping not supported
JESD204B	Up to 10G with CoreJESD20BTX/RX IP Core
PCIE Endpoint Gen1/Gen2	See Errata Descriptions and Workarounds (see page 3)
PCIE Rootport Gen1/Gen2	See Errata Descriptions and Workarounds (see page 3)
LiteFast	Up to 5 Gbps

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