Total Ionizing Dose Test Report

November 4th, 2016

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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the ATE test program. The report summarizes sample pins. Two factors make sampling appropriate: first, the tolerance is determined by current and propagation delays which are global parameters; second the total dose effect is uniformly distributed across the chip.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input and most of the output is grounded.

Table. 1. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	KRJWL
Quantity Tested	3
Serial Number	3883, 3893, 3898
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

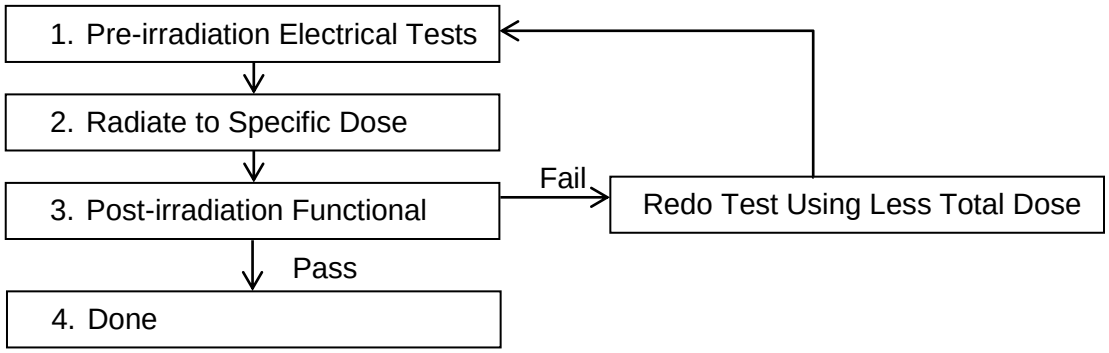

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 2. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 uRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump/PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design are reported at the LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-13 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL. In each case the current measured pre and post irradiation is minimal.

Table. 3. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
3883	125 krad	0.353	0.375	6.11
3893	125 krad	0.333	0.348	4.63
3898	125 krad	0.430	0.452	5.23

Table. 4. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
3883	125 krad	0.0114	0.0141	23.19
3893	125 krad	0.0107	0.0132	23.20
3898	125 krad	0.0121	0.0149	23.06

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
3883	125 krad	0.0383	0.0458	19.58
3893	125 krad	0.0392	0.0451	15.08
3898	125 krad	0.0345	0.0415	20.32

Table. 6. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
3883	125 krad	0.0162	0.0173	6.58
3893	125 krad	0.0163	0.0179	17.49
3898	125 krad	0.0161	0.0164	11.03

The following figures (2-13) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

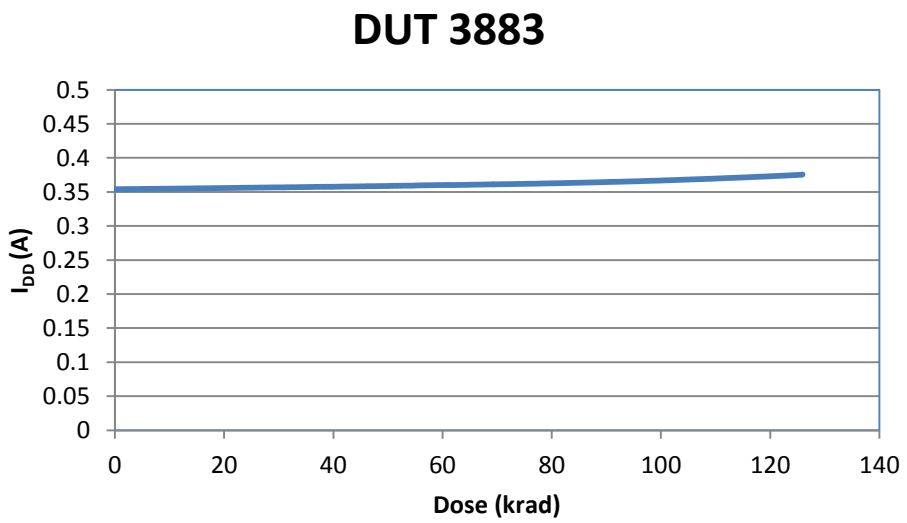

Fig. 2. DUT 3883 core power supply current (I_{DD}) versus TID

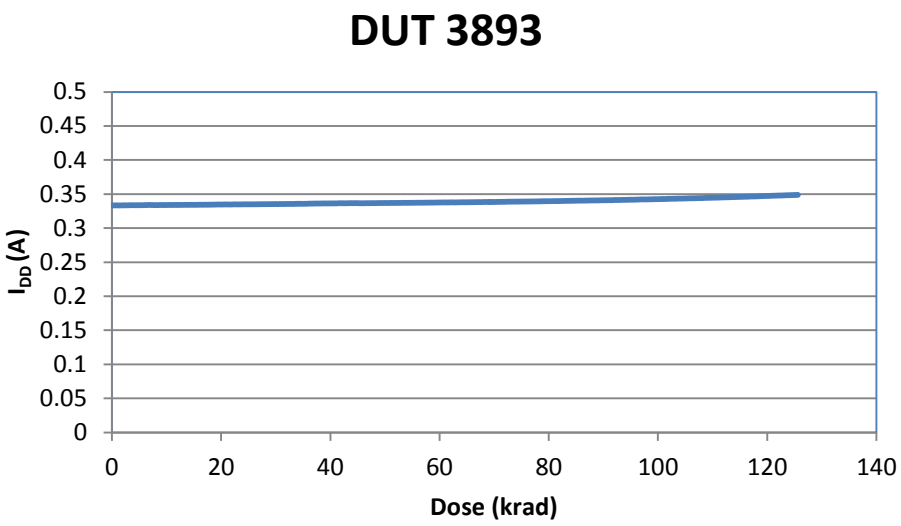

Fig. 3. DUT 3893 core power supply current (I_{DD}) versus TID

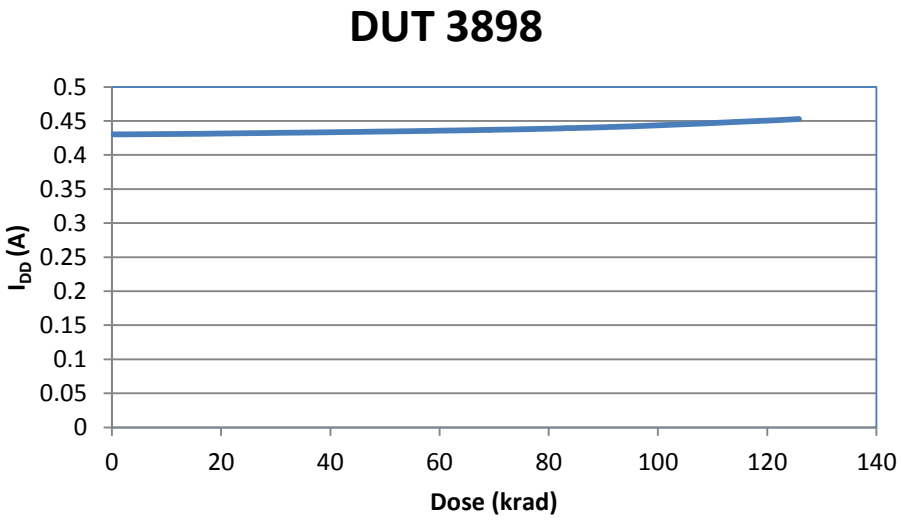

Fig. 4. DUT 3898 core power supply current (I_{DD}) versus TID

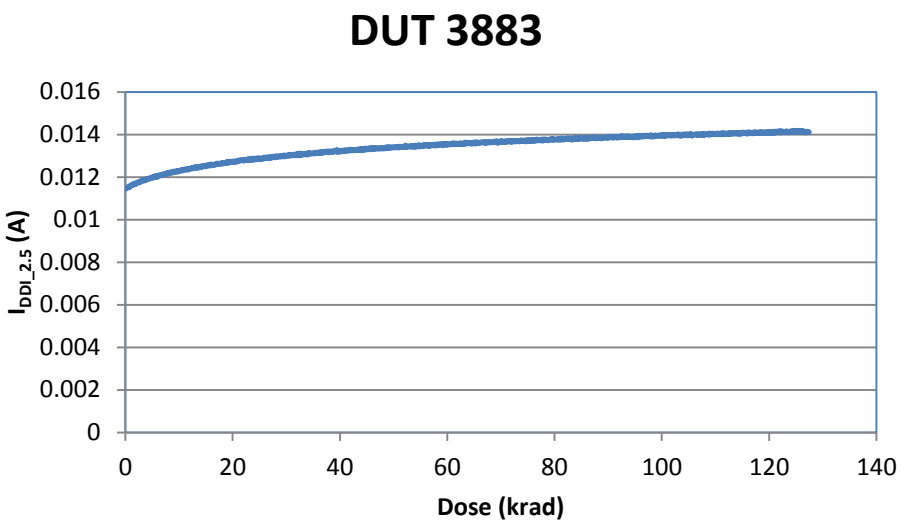

Fig. 5. DUT 3883 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

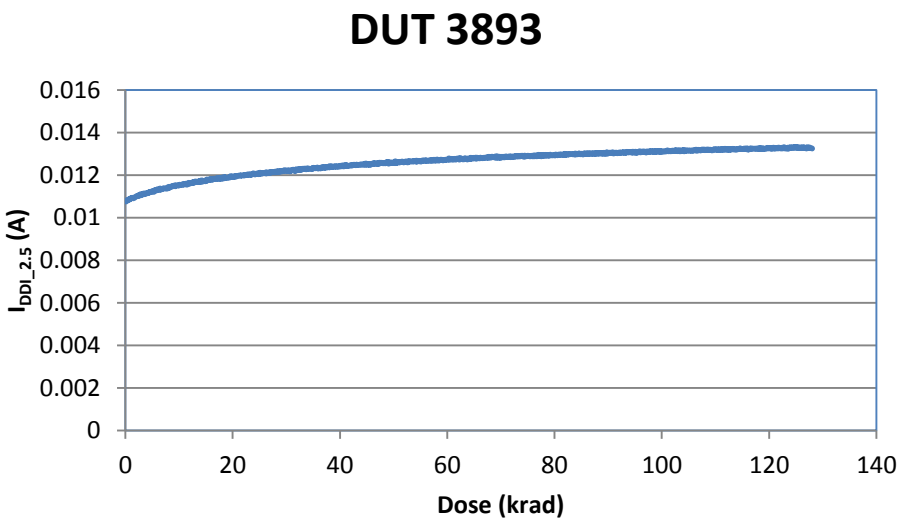

Fig. 6. DUT 3893 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

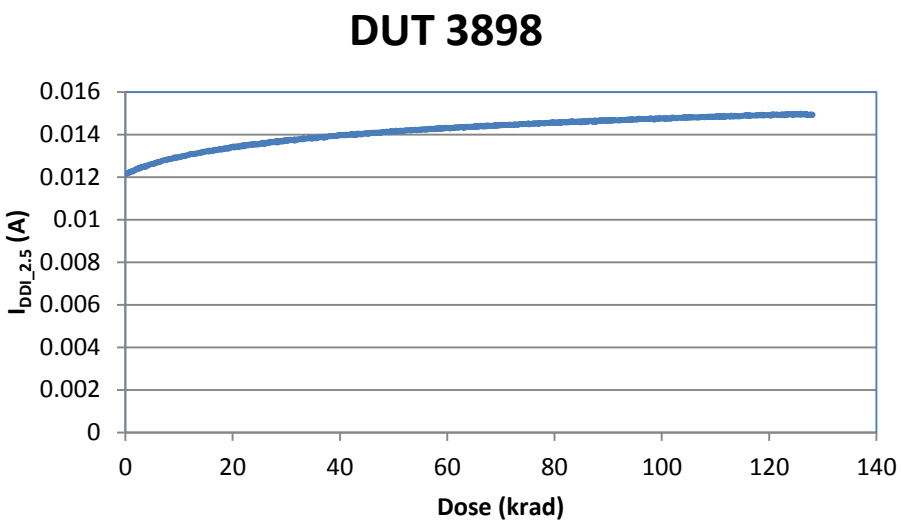

Fig. 7. DUT 3898 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

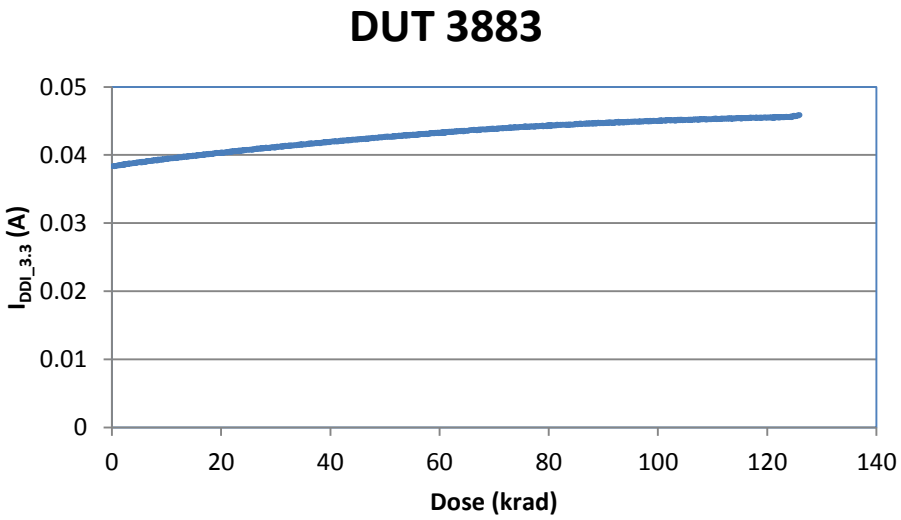

Fig. 8. DUT 3883 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

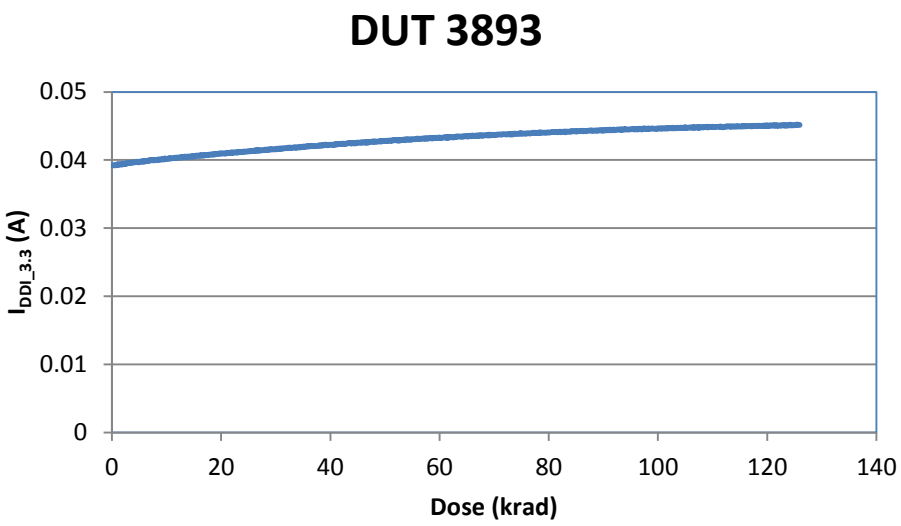

Fig. 9. DUT 3893 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

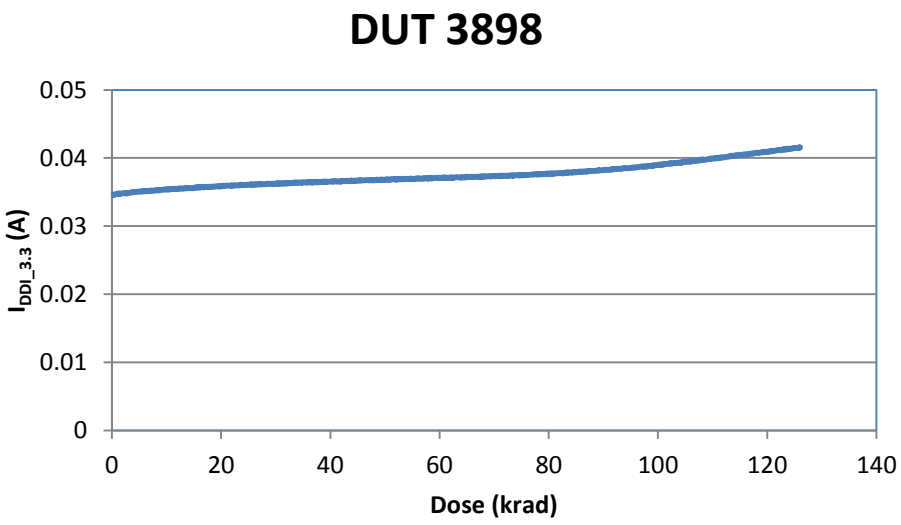

Fig. 10. DUT 3898 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

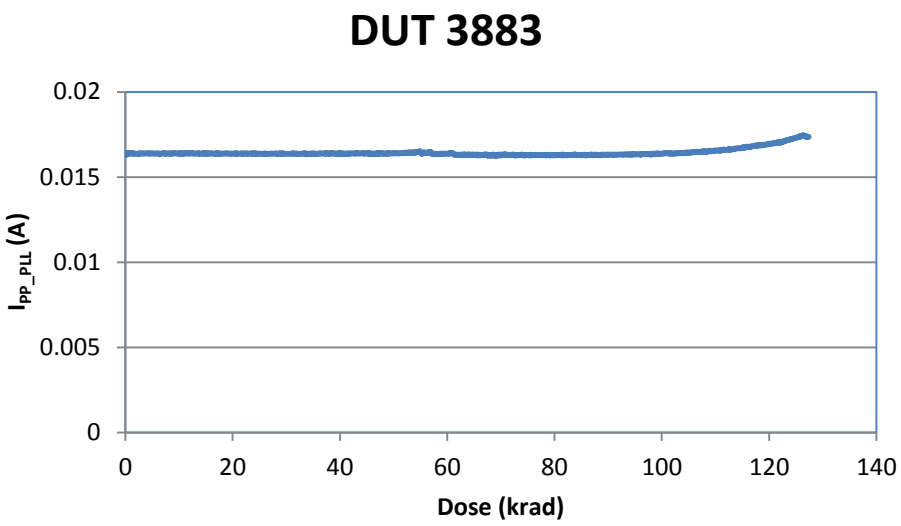

Fig. 11. DUT 3883 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

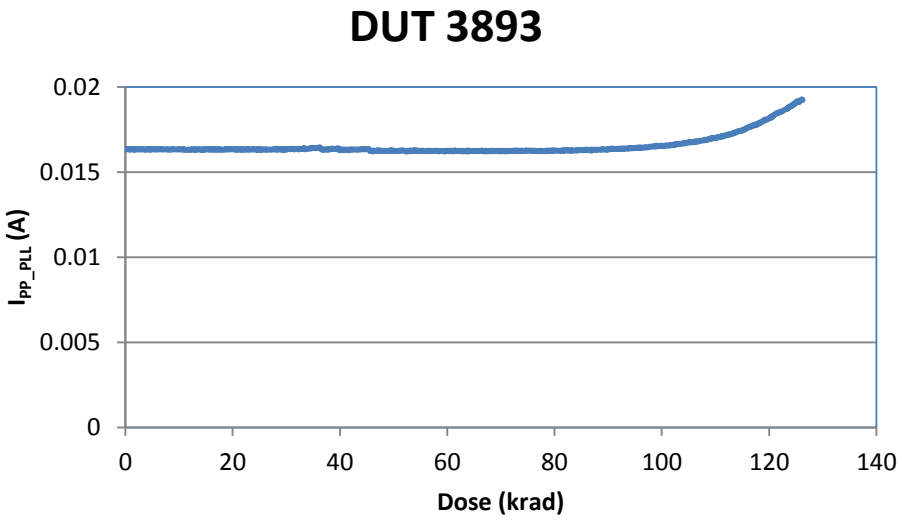

Fig. 12. DUT 3893 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

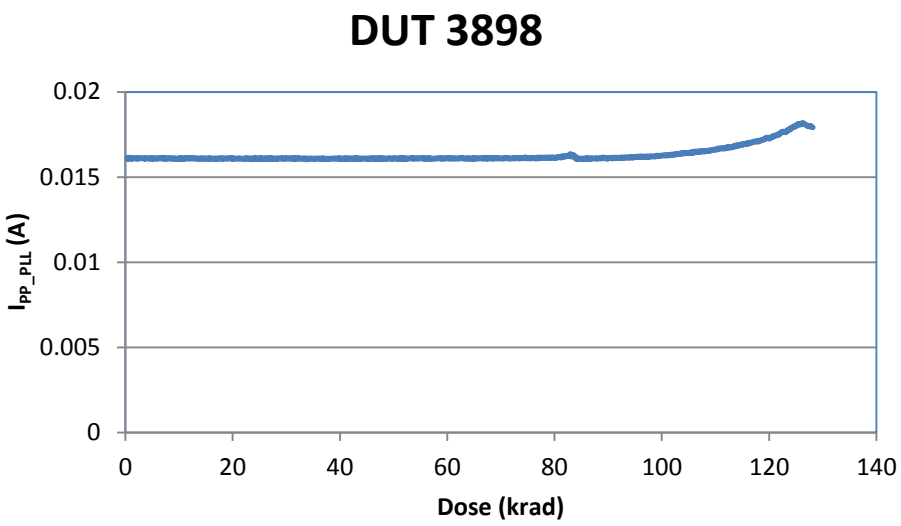

Fig. 13. DUT 3898 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 7. VIH Summary

DUT	Pre-irradiation	Post-irradiation
3883	Passed	Passed
3893	Passed	Passed
3898	Passed	Passed

Table. 8. VIL Summary

DUT	Pre-irradiation	Post-irradiation
3883	Passed	Passed
3893	Passed	Passed
3898	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 9 through 20 are sampled on several pins used in the burn in design.

Table. 9. LVCMOS 25 VOH – DUT 3883

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1334	2.1282	2.201	2.193	2.1715	2.1599	2.1518	2.1366	2.1174	2.0954	2.103	2.0771
EPCSRST_N_0	B31	2.1339	2.1282	2.2016	2.1919	2.1723	2.1582	2.1526	2.134	2.1184	2.0913	2.1038	2.0722
EPCSRST_N_1	B32	2.1348	2.1311	2.2036	2.1981	2.1749	2.1672	2.1547	2.1442	2.1227	2.1078	2.1093	2.092
EPCSRST_N_2	B34	2.1336	2.1312	2.2023	2.1994	2.1734	2.1693	2.1529	2.1474	2.1202	2.1127	2.1063	2.0978
EPCSRST_N_3	B35	2.1347	2.1334	2.2041	2.2027	2.1757	2.1744	2.1559	2.1541	2.1249	2.1226	2.1115	2.1093
EPCSRST_N_4	B36	2.1325	2.1292	2.1998	2.1957	2.17	2.1641	2.1484	2.1406	2.1136	2.1019	2.0987	2.0852
EPCSRST_N_5	B37	2.1343	2.1326	2.2034	2.2017	2.1748	2.1732	2.1548	2.1524	2.1234	2.1202	2.1101	2.1067
MONITOR	K23	2.1343	2.1302	2.2035	2.1981	2.1758	2.1682	2.157	2.1467	2.1263	2.112	2.1135	2.0971
PLL_MON	L20	2.1334	2.1317	2.2048	2.2036	2.1781	2.1766	2.1601	2.1583	2.1317	2.1296	2.1199	2.1176
TOGGLE_MON	L22	2.1332	2.1316	2.2035	2.2024	2.1763	2.1748	2.1569	2.1548	2.1276	2.1255	2.1155	2.1133

Table. 10. LVCMOS 25 VOH – DUT 3893

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1328	2.1277	2.2008	2.1929	2.1713	2.16	2.1517	2.1365	2.1173	2.0953	2.1026	2.0772
EPCSRST_N_0	B31	2.1336	2.1274	2.2018	2.1909	2.1722	2.1562	2.1525	2.1315	2.1184	2.0876	2.1037	2.0682
EPCSRST_N_1	B32	2.1344	2.1311	2.2033	2.1981	2.1748	2.167	2.1544	2.1444	2.1226	2.1079	2.1092	2.0922
EPCSRST_N_2	B34	2.1332	2.1312	2.2016	2.1993	2.1724	2.1693	2.1517	2.148	2.1188	2.1134	2.1051	2.0986
EPCSRST_N_3	B35	2.1339	2.1324	2.2033	2.2025	2.175	2.174	2.1554	2.1539	2.124	2.1223	2.1108	2.109
EPCSRST_N_4	B36	2.1319	2.1289	2.1994	2.1954	2.1696	2.1636	2.1481	2.1399	2.1132	2.1014	2.0981	2.0848
EPCSRST_N_5	B37	2.1338	2.1323	2.203	2.2018	2.1745	2.1731	2.1545	2.1525	2.1225	2.1205	2.1094	2.1068
MONITOR	K23	2.1334	2.1298	2.203	2.1978	2.175	2.1677	2.156	2.1462	2.1253	2.1113	2.1124	2.0967
PLL_MON	L20	2.1334	2.1318	2.2045	2.2038	2.1777	2.1764	2.1596	2.1582	2.1311	2.1298	2.1191	2.118
TOGGLE_MON	L22	2.133	2.1312	2.2033	2.2019	2.1759	2.1742	2.1563	2.1545	2.1268	2.1246	2.1147	2.1124

Table. 11. LVCMOS 25 VOH – DUT 3898

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1324	2.1271	2.2014	2.1934	2.1719	2.1603	2.1526	2.1375	2.119	2.0966	2.1048	2.0791
EPCSRST_N_0	B31	2.1334	2.1271	2.2019	2.1923	2.1725	2.1586	2.1532	2.1352	2.1193	2.0929	2.1052	2.0746
EPCSRST_N_1	B32	2.1344	2.1302	2.2036	2.1981	2.1753	2.1675	2.1554	2.1453	2.1241	2.1094	2.1108	2.0938
EPCSRST_N_2	B34	2.1326	2.1304	2.2017	2.1996	2.1729	2.1701	2.1525	2.1491	2.1204	2.1156	2.1067	2.1015
EPCSRST_N_3	B35	2.1337	2.1323	2.2037	2.2021	2.1755	2.174	2.1559	2.1541	2.1252	2.1235	2.1124	2.1104
EPCSRST_N_4	B36	2.131	2.1281	2.1989	2.1953	2.1688	2.1642	2.1471	2.1405	2.1118	2.1029	2.0967	2.0865
EPCSRST_N_5	B37	2.1331	2.1311	2.2033	2.2016	2.1751	2.1732	2.1552	2.153	2.1243	2.1214	2.1115	2.1083
MONITOR	K23	2.1337	2.1297	2.2026	2.1979	2.1744	2.1678	2.1547	2.1462	2.1237	2.1117	2.1107	2.097
PLL_MON	L20	2.13	2.1316	2.1978	2.203	2.1668	2.1756	2.1455	2.1574	2.1091	2.1284	2.0929	2.1164
TOGGLE_MON	L22	2.1326	2.1306	2.2032	2.2019	2.1758	2.1741	2.156	2.1538	2.1265	2.1239	2.1143	2.1116

Table. 12. LVCMOS 25 VOL – DUT 3883

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.527	239.626	169.263	176.567	198.115	209.002	221.787	236.118	254.259	275.542	268.3893	293.2682
EPCSRST_N_0	B31	234.836	239.927	168.722	177.887	197.436	210.963	220.869	238.972	253.291	280.219	267.4464	298.7243
EPCSRST_N_1	B32	233.55	236.613	166.423	171.771	194.255	201.888	215.196	225.013	246.192	260.893	259.7	276.6105
EPCSRST_N_2	B34	234.868	237.052	167.816	170.654	195.913	199.829	217.229	221.862	248.74	255.745	262.3615	270.4087
EPCSRST_N_3	B35	234.115	235.119	166.435	167.427	193.791	194.984	214.493	215.811	244.823	246.468	257.8546	259.5243
EPCSRST_N_4	B36	236.274	239.124	170.302	174.52	199.541	205.604	221.875	229.457	255.683	266.868	270.5845	283.465
EPCSRST_N_5	B37	234.63	235.91	167.026	168.206	194.532	196.214	215.434	217.305	245.903	248.427	259.0974	261.9096
MONITOR	K23	233.951	236.665	165.62	170.307	192.661	199.434	213.231	221.876	242.496	255.2	254.7976	269.7884
PLL_MON	L20	233.207	234.011	163.929	164.62	190.076	190.956	209.875	210.843	237.305	238.373	248.9199	250.0262
TOGGLE_MON	L22	233.503	234.13	164.791	165.419	191.468	192.309	210.704	211.544	239.526	240.492	251.5842	252.7386

Table. 13. LVCMOS 25 VOL – DUT 3893

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	236.194	240.116	169.363	176.517	198.102	208.738	221.611	235.904	254.045	275.329	268.339	293.0923
EPCSRST_N_0	B31	234.823	240.242	168.634	178.855	197.461	212.597	220.919	241.134	253.178	283.525	267.4212	302.5586
EPCSRST_N_1	B32	233.525	236.55	166.435	171.495	194.067	201.574	214.995	224.724	246.142	260.265	259.4615	276.033
EPCSRST_N_2	B34	235.483	237.329	168.557	170.792	196.791	199.654	218.234	221.762	249.958	255.206	263.9434	269.7308
EPCSRST_N_3	B35	234.73	235.747	166.762	167.703	194.193	195.322	214.857	215.999	245.363	246.619	258.294	259.8005
EPCSRST_N_4	B36	236.814	239.664	170.541	174.759	199.842	205.78	222.301	229.759	256.047	267.082	270.7728	283.7412
EPCSRST_N_5	B37	234.868	236.086	167.026	168.105	194.908	196.226	215.685	217.242	246.38	248.326	259.6624	261.7589
MONITOR	K23	234.793	237.03	166.11	170.533	193.352	199.861	214.123	222.353	243.451	255.954	256.0919	270.6554
PLL_MON	L20	233.118	233.496	164.193	164.558	190.441	190.831	210.554	210.755	238.046	238.335	249.9633	250.0639
TOGGLE_MON	L22	233.515	233.98	165.017	165.569	191.644	192.472	211.055	211.795	239.727	241.082	252.0485	253.4915

Table. 14. LVCMOS 25 VOL – DUT 3898

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.087	239.299	168.71	176.228	197.587	208.738	221.02	235.917	253.341	275.454	267.4841	293.218
EPCSRST_N_0	B31	234.145	239.148	168.094	177.359	196.908	210.573	220.379	238.607	252.813	279.854	267.0567	298.586
EPCSRST_N_1	B32	233.311	236.362	166.297	171.746	193.803	201.888	214.681	225.277	245.815	261.282	259.2481	277.3009
EPCSRST_N_2	B34	234.479	236.651	168.093	170.641	196.201	199.905	217.694	222.239	249.833	256.562	263.8304	271.5135
EPCSRST_N_3	B35	233.638	235.194	166.172	167.678	193.803	195.611	214.581	216.577	244.886	247.673	258.0052	260.8676
EPCSRST_N_4	B36	235.709	238.559	170.039	174.194	199.302	205.228	221.649	229.206	255.62	266.605	270.3334	283.2892
EPCSRST_N_5	B37	234.454	235.935	166.774	168.356	194.519	196.452	215.196	217.455	245.702	249.117	258.9468	262.713
MONITOR	K23	233.499	236.087	165.13	169.703	192.032	198.855	212.565	221.398	241.83	254.973	254.3327	269.5496
PLL_MON	L20	232.188	232.515	163.213	163.665	189.335	189.837	209.184	209.649	236.689	236.89	248.2663	248.5931
TOGGLE_MON	L22	232.662	233.152	164.327	164.691	190.979	191.493	210.34	210.653	239.212	239.664	251.396	251.8979

Table. 15. LVTTL VOH – DUT 3883

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9204	2.9152	2.9097	2.9015	2.8892	2.8741	2.8688	2.8468	2.8498	2.8206
EPCSRST_N_0	B31	2.9208	2.9151	2.9103	2.9003	2.8899	2.8716	2.8696	2.8427	2.8509	2.8148
EPCSRST_N_1	B32	2.9212	2.9181	2.9118	2.9063	2.8937	2.8836	2.8751	2.8605	2.8572	2.8376
EPCSRST_N_2	B34	2.9199	2.9178	2.9106	2.9074	2.8916	2.8865	2.8723	2.8655	2.8538	2.8443
EPCSRST_N_3	B35	2.9212	2.9201	2.9123	2.911	2.8947	2.8932	2.8771	2.8753	2.8596	2.8575
EPCSRST_N_4	B36	2.919	2.9161	2.9084	2.9039	2.8872	2.8793	2.866	2.8544	2.8448	2.8299
EPCSRST_N_5	B37	2.9206	2.9195	2.9113	2.91	2.8935	2.8913	2.8757	2.873	2.858	2.8547
MONITOR	K23	2.9211	2.9176	2.9124	2.9066	2.8955	2.8858	2.8788	2.8649	2.8626	2.8444
PLL_MON	L20	2.9209	2.9194	2.9136	2.9121	2.8989	2.8975	2.884	2.8822	2.8697	2.868
TOGGLE_MON	L22	2.9201	2.919	2.9121	2.9109	2.8963	2.8948	2.8806	2.8791	2.8648	2.8627

Table. 16. LVTTL VOH – DUT 3893

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9197	2.9149	2.9094	2.9012	2.889	2.8737	2.8686	2.8468	2.8498	2.8207
EPCSRST_N_0	B31	2.9205	2.9144	2.91	2.899	2.89	2.8689	2.8697	2.839	2.8508	2.8103
EPCSRST_N_1	B32	2.9207	2.9179	2.9115	2.9063	2.8935	2.8836	2.875	2.8606	2.857	2.8379
EPCSRST_N_2	B34	2.9197	2.9182	2.91	2.9075	2.8904	2.8866	2.8713	2.8659	2.8521	2.8452
EPCSRST_N_3	B35	2.9203	2.9195	2.9116	2.9104	2.8942	2.8929	2.8764	2.875	2.859	2.8573
EPCSRST_N_4	B36	2.9182	2.9159	2.9076	2.9037	2.8866	2.8789	2.8655	2.854	2.8444	2.8294
EPCSRST_N_5	B37	2.9205	2.9193	2.9111	2.91	2.8932	2.8915	2.8751	2.8732	2.8574	2.8547
MONITOR	K23	2.9206	2.9171	2.9116	2.9063	2.8946	2.8851	2.8777	2.8642	2.8612	2.8435
PLL_MON	L20	2.9208	2.9195	2.9132	2.9121	2.8983	2.8973	2.8834	2.8823	2.8691	2.8681
TOGGLE_MON	L22	2.9198	2.9188	2.9117	2.9103	2.8957	2.8942	2.8798	2.8781	2.8641	2.8619

Table. 17. LVTTL VOH – DUT 3898

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9212	2.9163	2.9106	2.9025	2.8903	2.8746	2.8702	2.8472	2.851	2.8207
EPCSRST_N_0	B31	2.9213	2.9159	2.9112	2.9015	2.891	2.8724	2.8704	2.8429	2.8515	2.8152
EPCSRST_N_1	B32	2.9217	2.9184	2.9126	2.9067	2.8945	2.8833	2.8758	2.8601	2.8578	2.8368
EPCSRST_N_2	B34	2.9209	2.9193	2.9111	2.9082	2.8914	2.8865	2.8717	2.865	2.8524	2.8435
EPCSRST_N_3	B35	2.9217	2.9204	2.9127	2.9113	2.895	2.8931	2.8772	2.8745	2.8596	2.8563
EPCSRST_N_4	B36	2.9201	2.9177	2.9094	2.9049	2.8879	2.8801	2.8666	2.8552	2.8454	2.8306
EPCSRST_N_5	B37	2.9216	2.9202	2.912	2.9107	2.8944	2.8918	2.8764	2.8729	2.8585	2.8541
MONITOR	K23	2.9219	2.9185	2.9133	2.9079	2.8966	2.8867	2.8799	2.8656	2.8635	2.845
PLL_MON	L20	2.9223	2.9214	2.9149	2.9137	2.9001	2.8991	2.8853	2.8842	2.871	2.8699
TOGGLE_MON	L22	2.9213	2.9204	2.9132	2.9122	2.8973	2.8961	2.8813	2.8802	2.8654	2.8642

Table. 18. LVTTL VOL – DUT 3883

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	216.147	219.7829	230.0011	237.3356	245.7358	260.154	265.9213	287.486	287.9882	316.4501
EPCSRST_N_0	B31	215.3634	220.1904	229.1861	238.2759	245.1716	263.0377	265.0124	291.8742	287.2716	322.673
EPCSRST_N_1	B32	214.2429	216.8053	223.8987	228.961	240.6167	250.46	259.0846	273.4277	278.4434	297.375
EPCSRST_N_2	B34	215.0866	216.9928	225.3049	227.8672	242.6166	247.4601	261.4282	268.6154	281.6823	290.7087
EPCSRST_N_3	B35	214.6491	215.1491	223.7424	224.3674	239.9292	241.2104	257.4284	259.1158	276.2338	277.9035
EPCSRST_N_4	B36	216.5865	219.1176	227.836	231.7733	247.4914	255.1473	268.5529	279.7399	290.8343	305.1711
EPCSRST_N_5	B37	214.9616	215.8365	224.2424	225.4611	240.9292	242.9916	258.7096	261.2095	277.6399	280.5399
MONITOR	K23	214.2925	216.8249	224.5159	228.2988	238.7098	247.3387	254.9359	268.1295	272.6031	289.5415
PLL_MON	L20	213.2064	213.9563	222.3937	222.675	234.7373	235.8623	249.362	250.4558	265.8904	266.7327
TOGGLE_MON	L22	213.7081	214.1148	221.5286	221.6537	236.8881	237.4825	252.3415	253.4989	269.0508	269.9667

Table. 19. LVTTL VOL – DUT 3893

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	216.6172	220.0023	229.8757	237.1475	245.5791	259.8719	265.6706	286.8591	287.9379	316.1987
EPCSRST_N_0	B31	215.4261	220.6606	229.0294	239.4043	244.8268	264.9183	264.9183	295.0713	287.0328	327.2616
EPCSRST_N_1	B32	214.1179	216.4615	223.7112	228.336	240.4917	250.1162	258.6471	273.0215	278.1295	296.8728
EPCSRST_N_2	B34	215.6803	217.024	225.9611	227.836	243.804	247.5851	262.7719	267.8342	283.3018	289.6542
EPCSRST_N_3	B35	214.9928	215.6178	224.3049	225.0861	240.3667	241.3041	258.0846	259.4283	276.7862	278.1797
EPCSRST_N_4	B36	216.9615	219.7114	228.0547	232.1483	247.6788	255.3035	268.9591	279.8961	291.236	305.5226
EPCSRST_N_5	B37	215.1178	215.9928	224.8049	225.3674	241.3041	242.6166	259.3971	261.0845	278.2551	280.3641
MONITOR	K23	215.0115	217.1062	225.2037	228.9554	239.3038	247.839	256.0302	268.7235	273.8219	290.4211
PLL_MON	L20	213.3626	213.5188	222.6125	222.6125	235.2998	235.7373	250.1433	250.4245	266.607	266.6824
TOGGLE_MON	L22	213.8019	214.1148	221.6537	222.0291	237.0758	238.3271	253.1235	254.4374	269.6154	270.9204

Table. 20. LVTTL VOL – DUT 3898

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	214.9873	218.8113	228.7473	236.1132	244.5134	259.5898	264.6676	286.7338	286.7688	316.2364
EPCSRST_N_0	B31	214.3291	219.1874	227.8697	237.1789	244.0119	262.1287	264.3541	290.9339	286.3036	322.1953
EPCSRST_N_1	B32	213.1804	216.3365	222.8987	228.1797	239.648	250.3975	258.1471	273.3964	277.5771	298.0529
EPCSRST_N_2	B34	214.3054	216.149	224.3049	227.2735	242.6791	247.4914	262.1157	268.8341	282.8875	291.3365
EPCSRST_N_3	B35	213.7429	214.5241	223.305	224.0862	239.648	241.6791	257.3659	260.022	276.2213	279.1841
EPCSRST_N_4	B36	215.5866	218.0552	226.8985	230.8046	246.6789	254.4598	267.9279	278.9587	290.307	304.807
EPCSRST_N_5	B37	214.0241	215.2428	223.8674	224.9611	240.3042	242.6478	258.3034	261.3657	277.3386	281.1174
MONITOR	K23	213.6046	215.8244	223.234	227.1421	237.428	246.2445	253.873	267.1915	271.4596	288.9006
PLL_MON	L20	211.7064	211.8626	221.1125	221.2062	233.4248	233.9873	248.2058	248.7371	264.5831	264.8973
TOGGLE_MON	L22	212.3943	212.7696	220.2461	220.3399	235.8245	236.2625	251.841	252.3415	268.3983	268.7621

E. Propagation Delay

Table 21 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 21. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
3883	125 krad	0.446	0.442	-0.965
3893	125 krad	0.454	0.448	-1.328
3898	125 krad	0.442	0.439	-0.706

F. Transition Time

The figures below show the pre-irradiation and post-annealing transitions edges. In each case the radiation induced transition degradation is not observable.

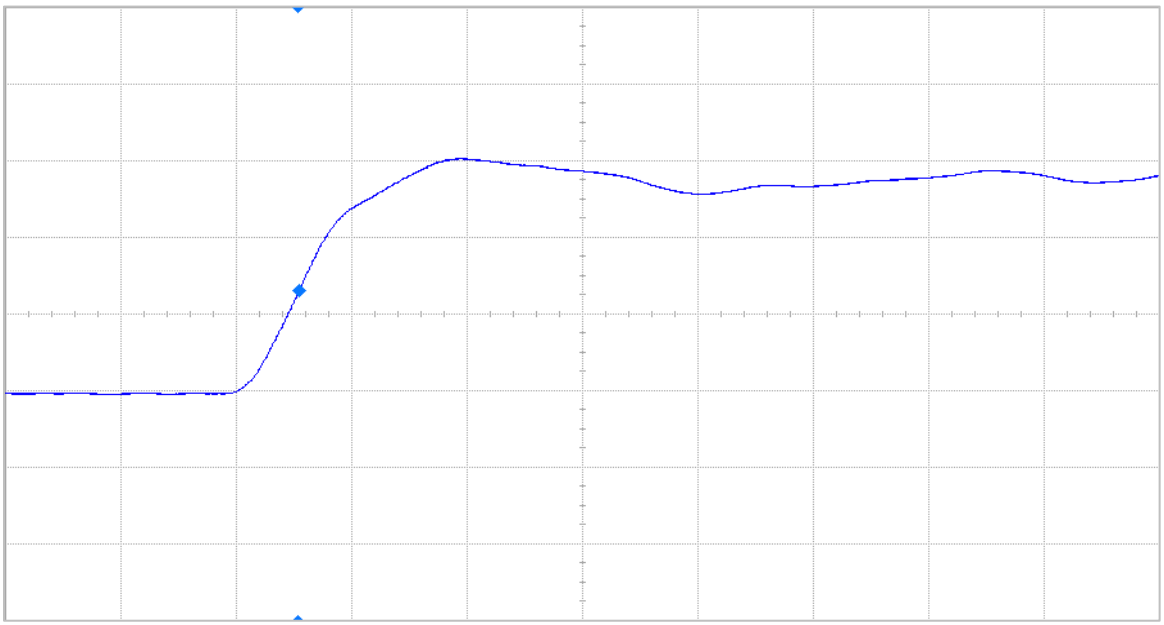

Fig. 14 (a). DUT 3883 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

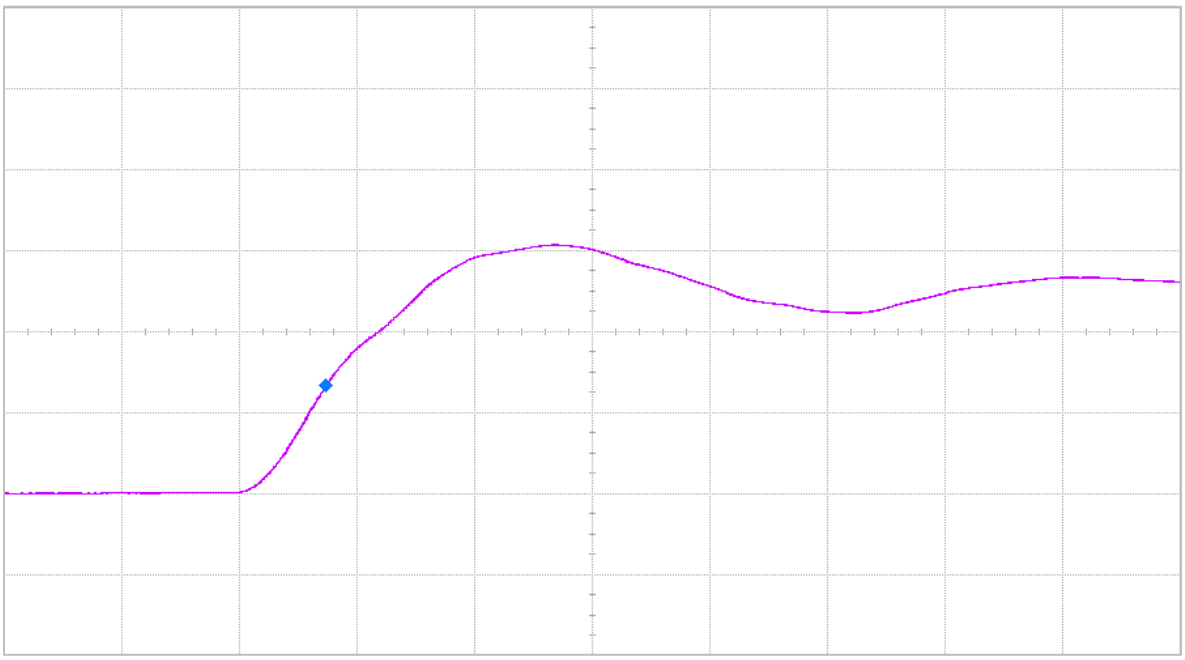

Fig. 14 (b). DUT 3883 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

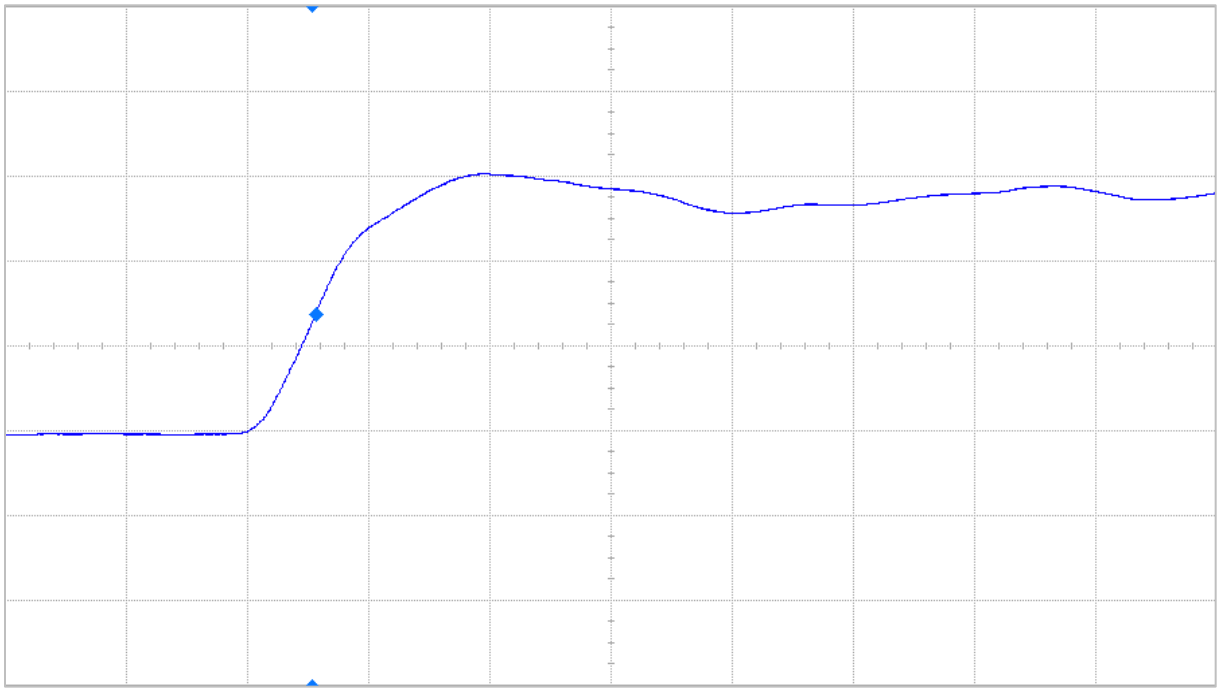

Fig. 15 (a). DUT 3893 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

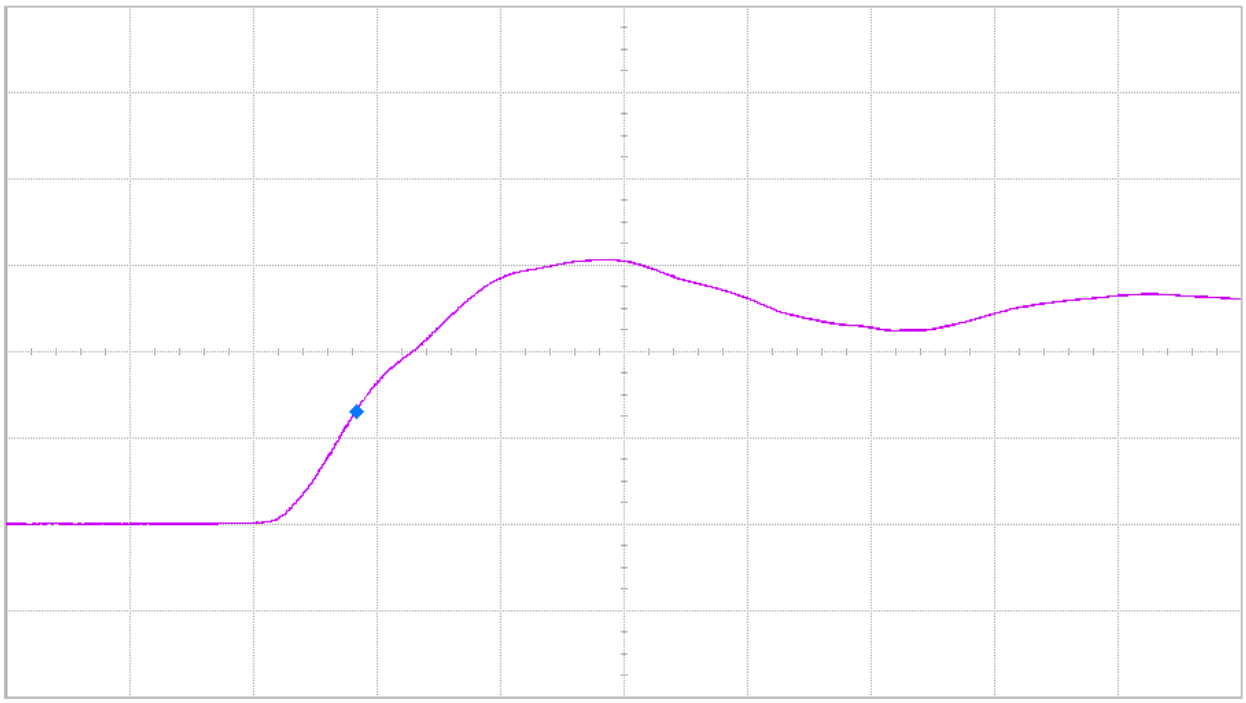

Fig. 15 (b). DUT 3893 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

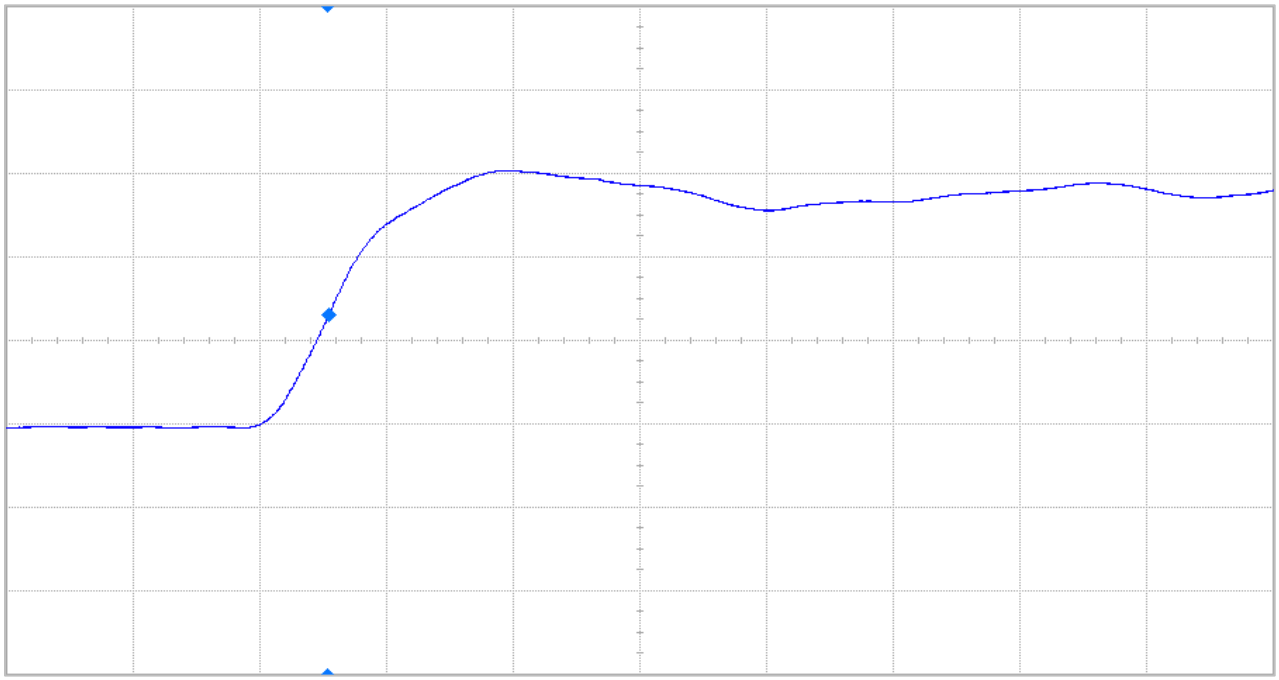

Fig. 16 (a). DUT 3898 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

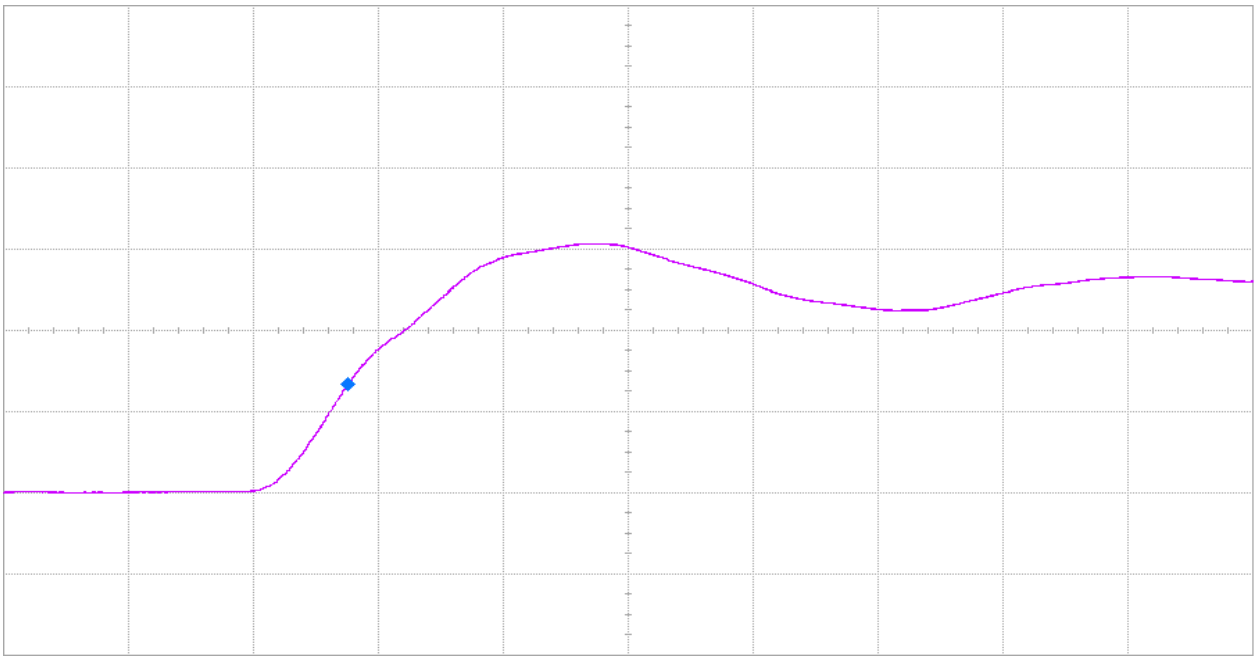

Fig. 16 (b). DUT 3898 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

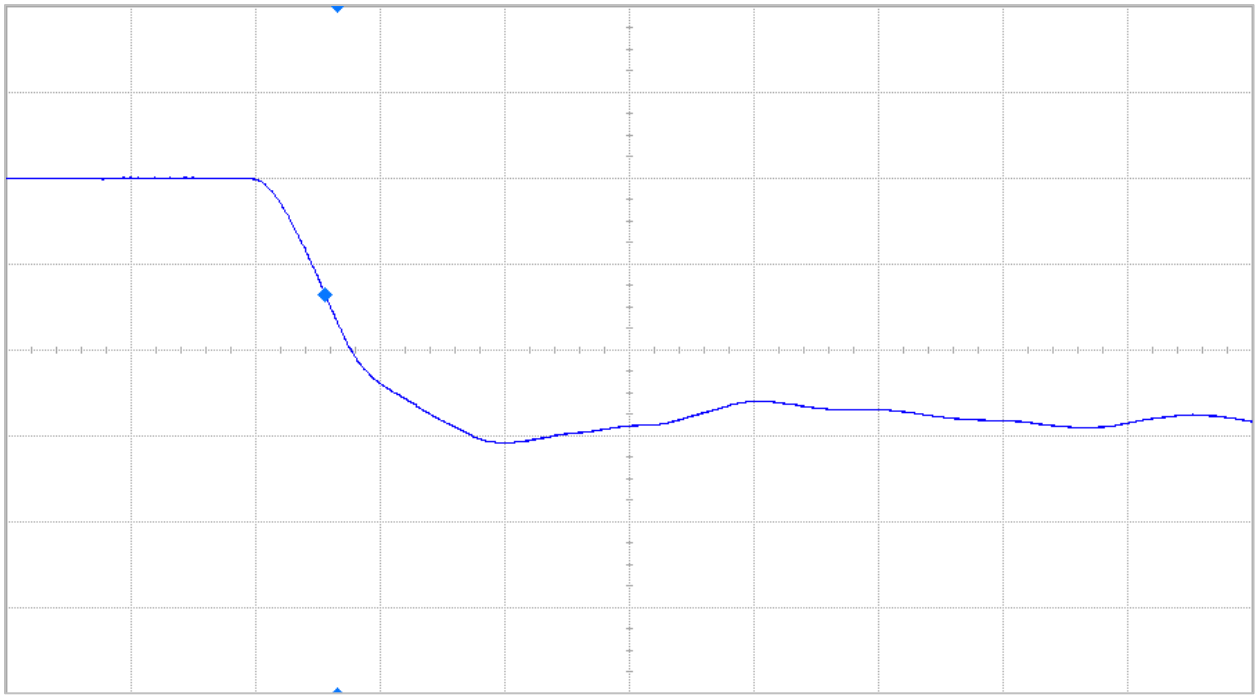

Fig. 17 (a). DUT 3883 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

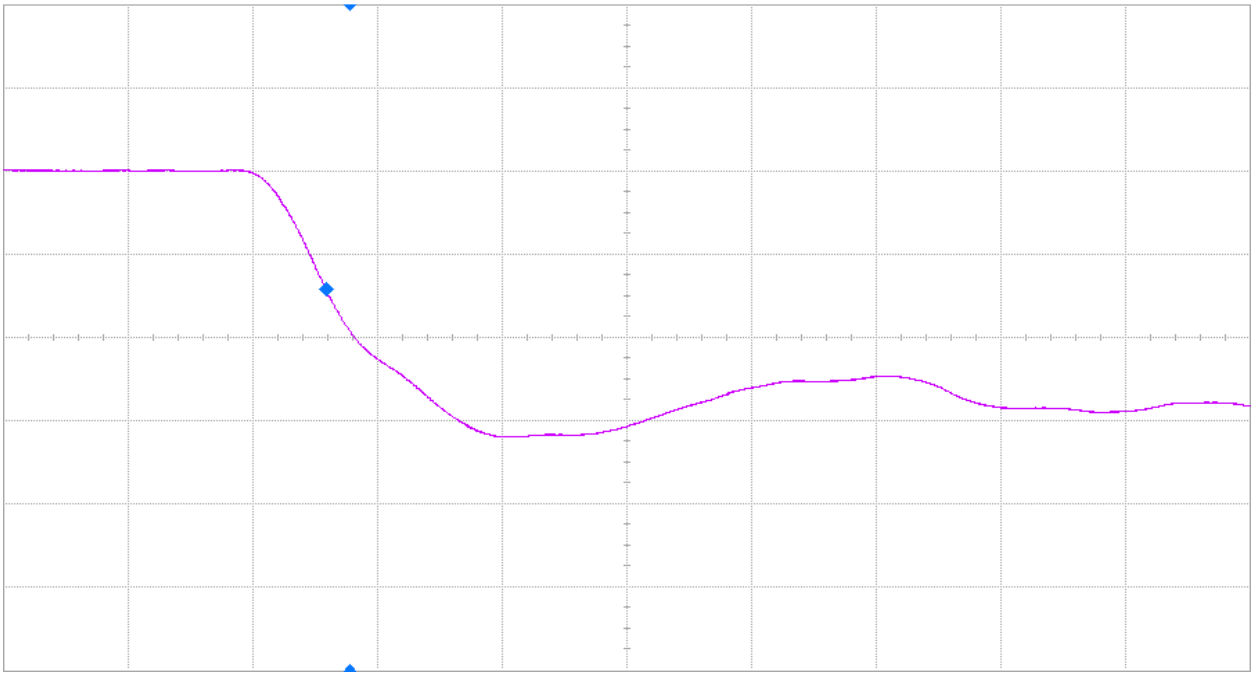

Fig. 17 (b). DUT 3883 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

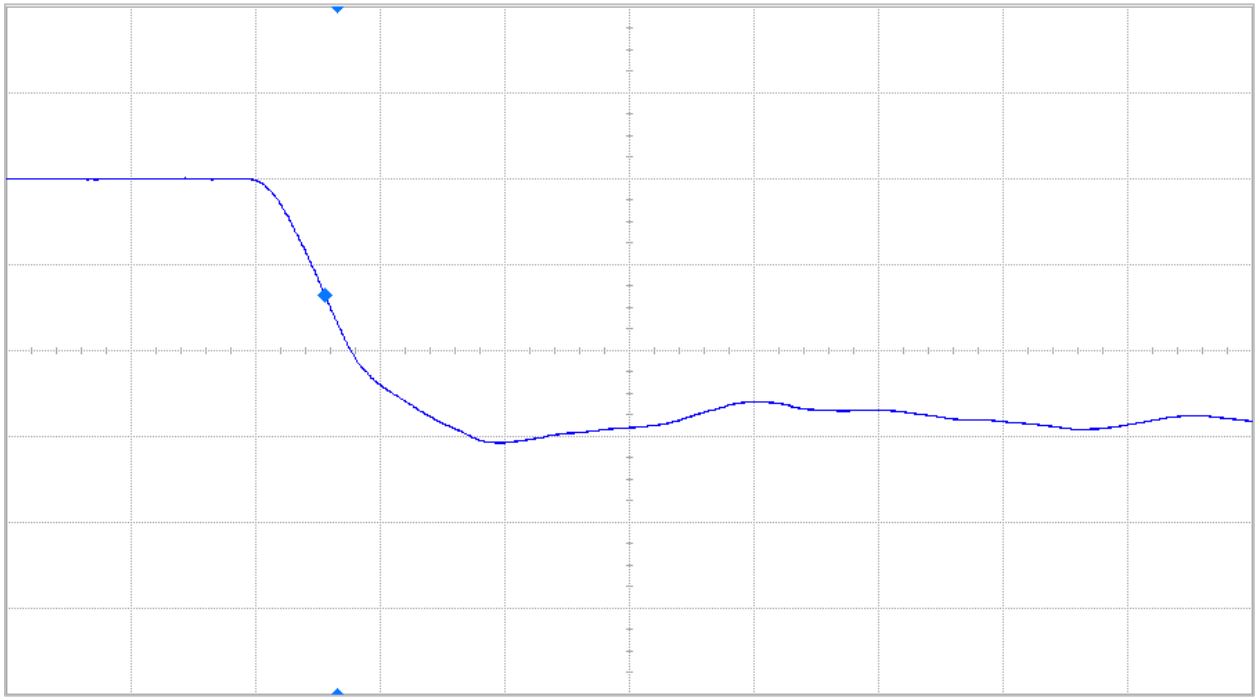

Fig. 18 (a). DUT 3893 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

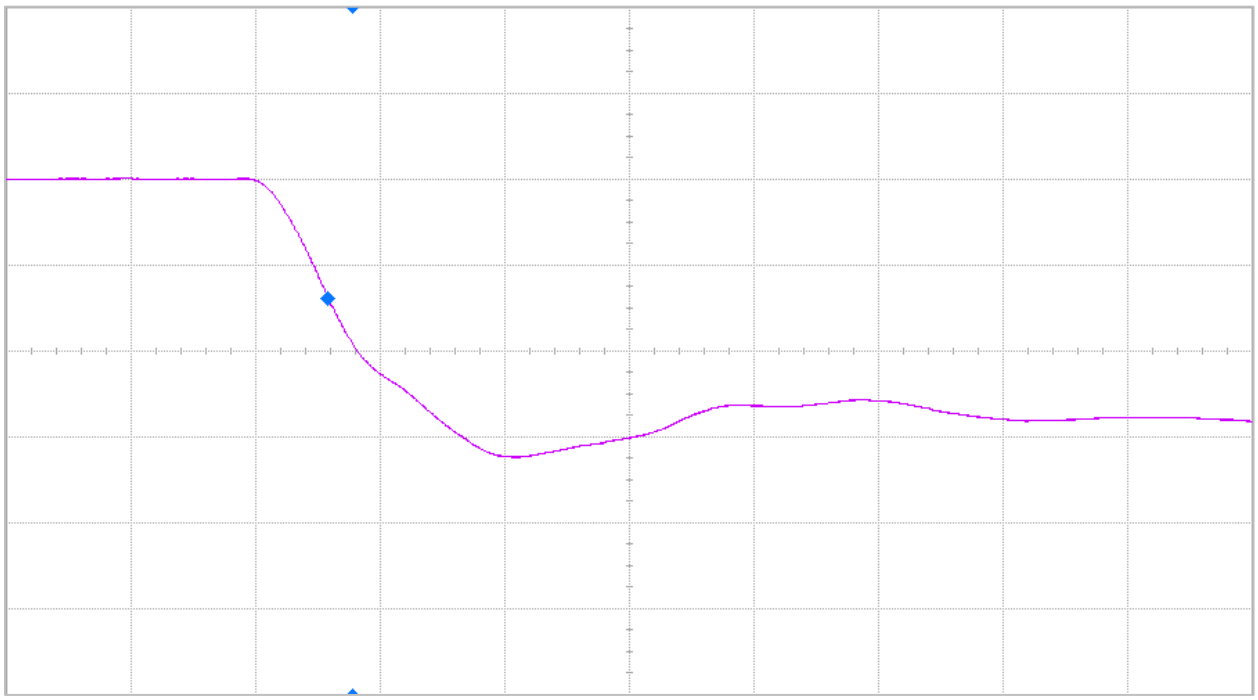

Fig. 18 (b). DUT 3893 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

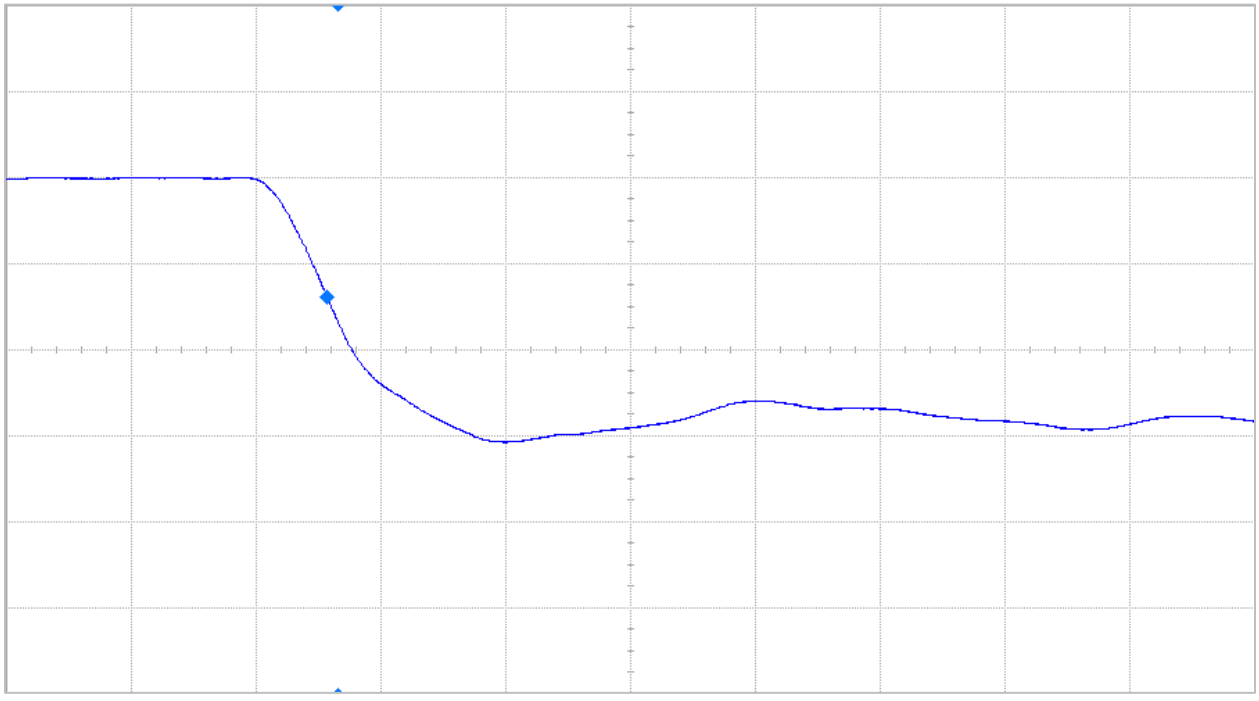

Fig. 19 (a). DUT 3898 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

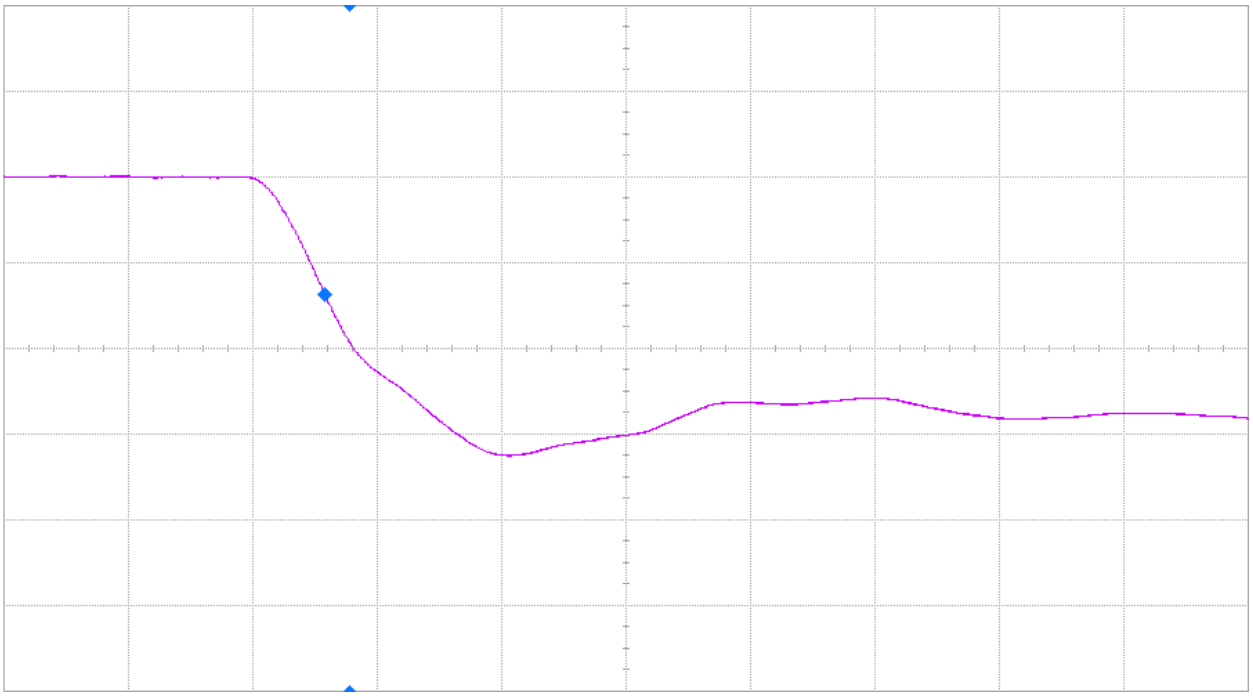

Fig. 19 (b). DUT 3898 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 22. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	**Coverage**
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 uRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

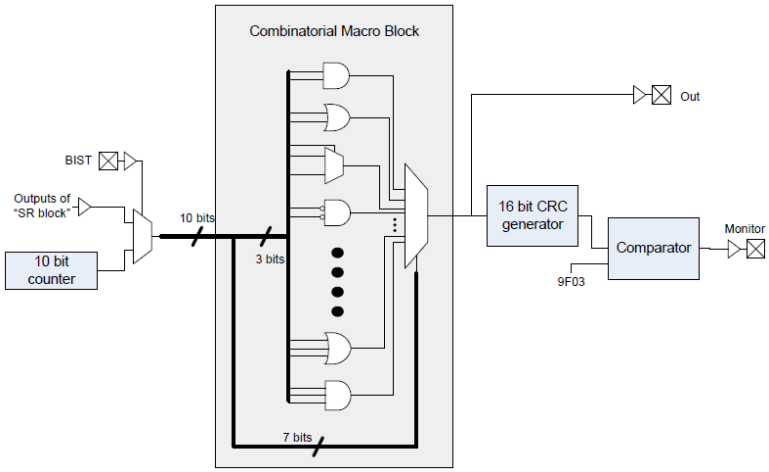

Fig. 20. Combo Block

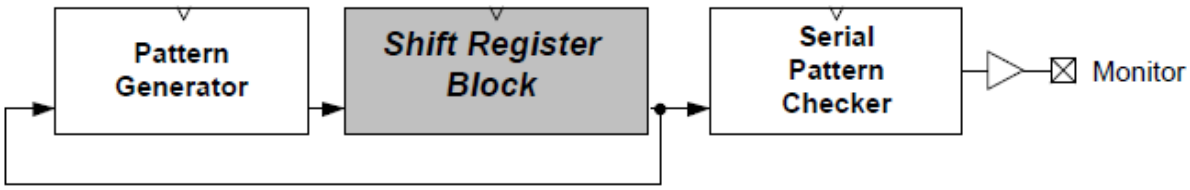

Fig. 21. Shift Register Block

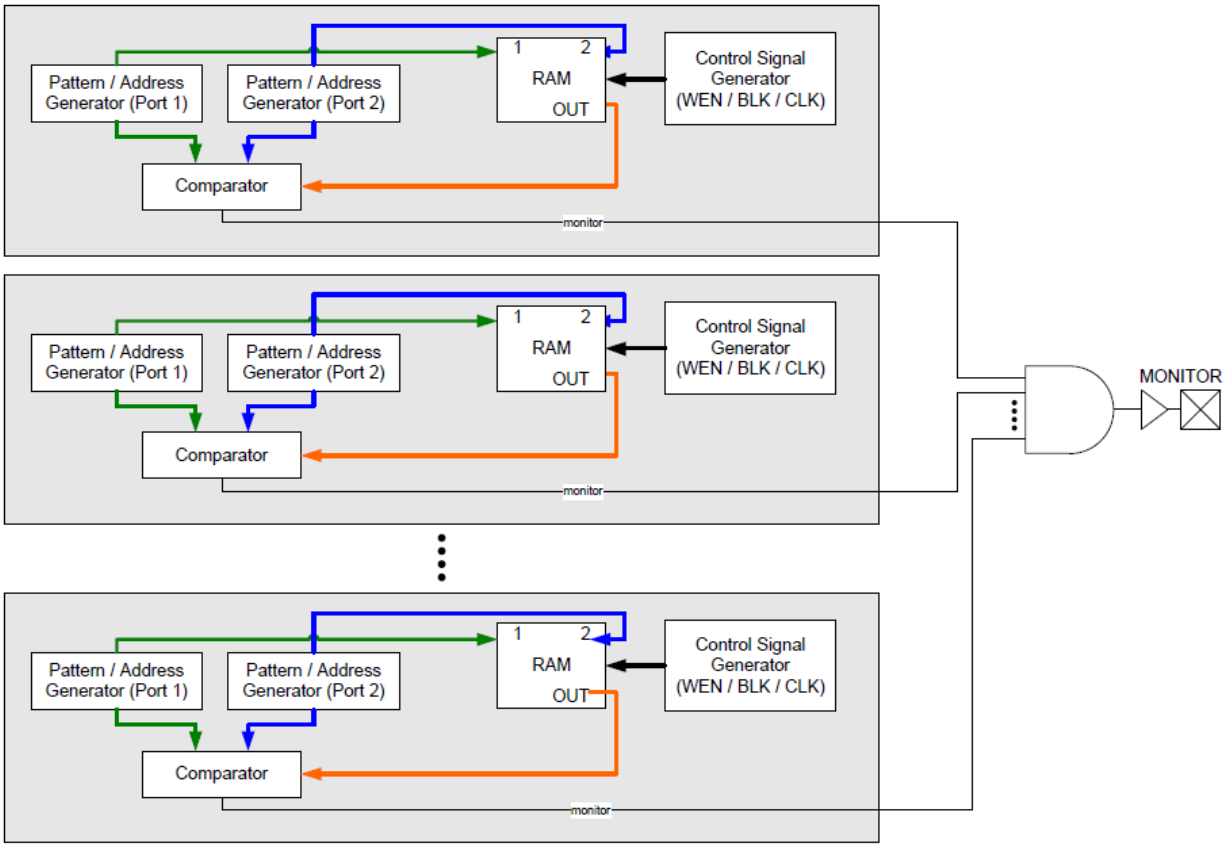

Fig. 22. Embedded Ram Blocks

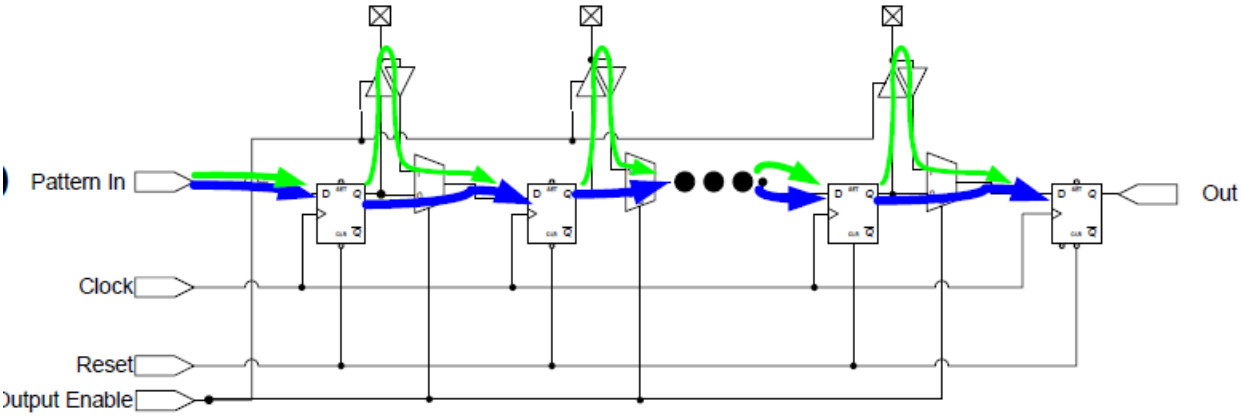

Fig. 23. IO Block

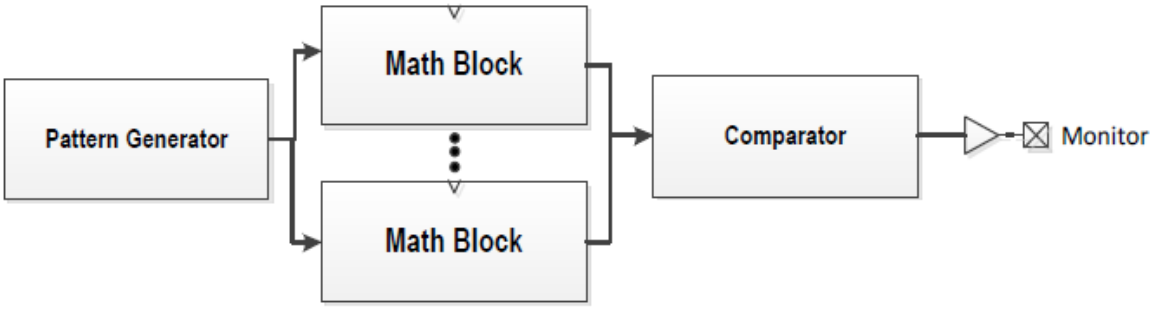

Fig. 24. Math Block