Total Ionizing Dose Test Report

No. 14T-RTAX4000S-CQ352-D7FLT1

December 16, 2014

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CK Huang and J.J. Wang

(408) 643-6136, 643-6302

chang-kai.huang@microsemi.com, jih-jong.wang@microsemi.com

I. Summary Table

The TID tolerance for each tested parameter is summarized below in Table 1. The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by 1019.8 to anneal down ICC is performed for approximately 7 days. DUT is expected to pass the major specifications listed in the table for 300 krad (SiO2) of irradiation.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 300 krad (SiO_2)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Time	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation all inputs are grounded except for the inputs Burnin, oe_EAQ, enable_HSB and the utilized clocks (Rclock1-3 and Hclock1-4). The inputs Burnin, oe_EAQ and enable_HSB are set high to 3.3 V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal each input and output is tied to ground or VCCI through a 4.7 kΩ resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Part Number	**RTAX4000S**
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	MASTER_RTAX4000S_DESIGN_80_SP1
Die Lot Number	D7FLT1
Quantity Tested	6
Serial Number	200 krad: 3989, 3991, 3993 300 krad: 4005, 4017, 4020
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

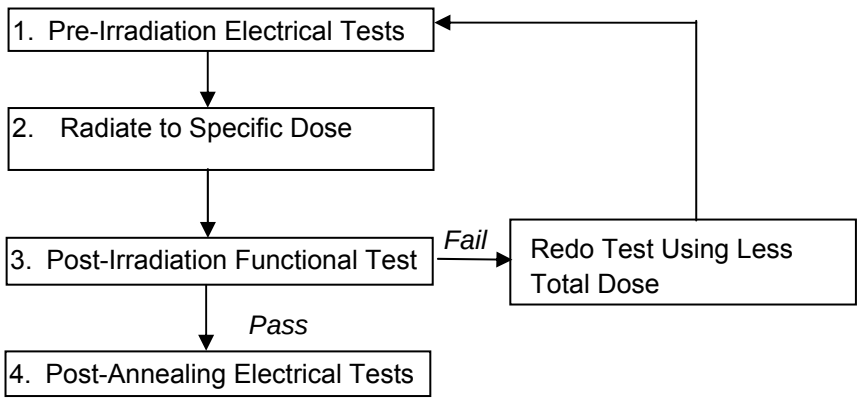

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi SoC Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (Master_RTAX4000S_Design_80_SP1) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-D Devices

Supply Voltage	Minimum	Recommended	Maximum
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1,170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8)
5. Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the IO power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2-7 show the influx ICCA and ICCI versus total dose for the DUTs.

Referring to TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICC should be defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of the *RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs datasheet* posted on the Microsemi SoC Products Group website:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

Therefore, the PIPL for ICCA is 600 mA, and the PIPL for ICCI is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
3989	200 krad	16	23	19	72	124	23
3991	200 krad	6	10	6	72	126	25
3993	200 krad	14	21	18	76	118	24
4005	300 krad	5	135	15	75	238	55
4017	300 krad	17	223	35	78	197	50
4020	300 krad	16	187	23	88	203	51

Based on these PIPL, the post-annealing DUT passes both the ICCA and ICCI specification for 300 krad(SiO_2).

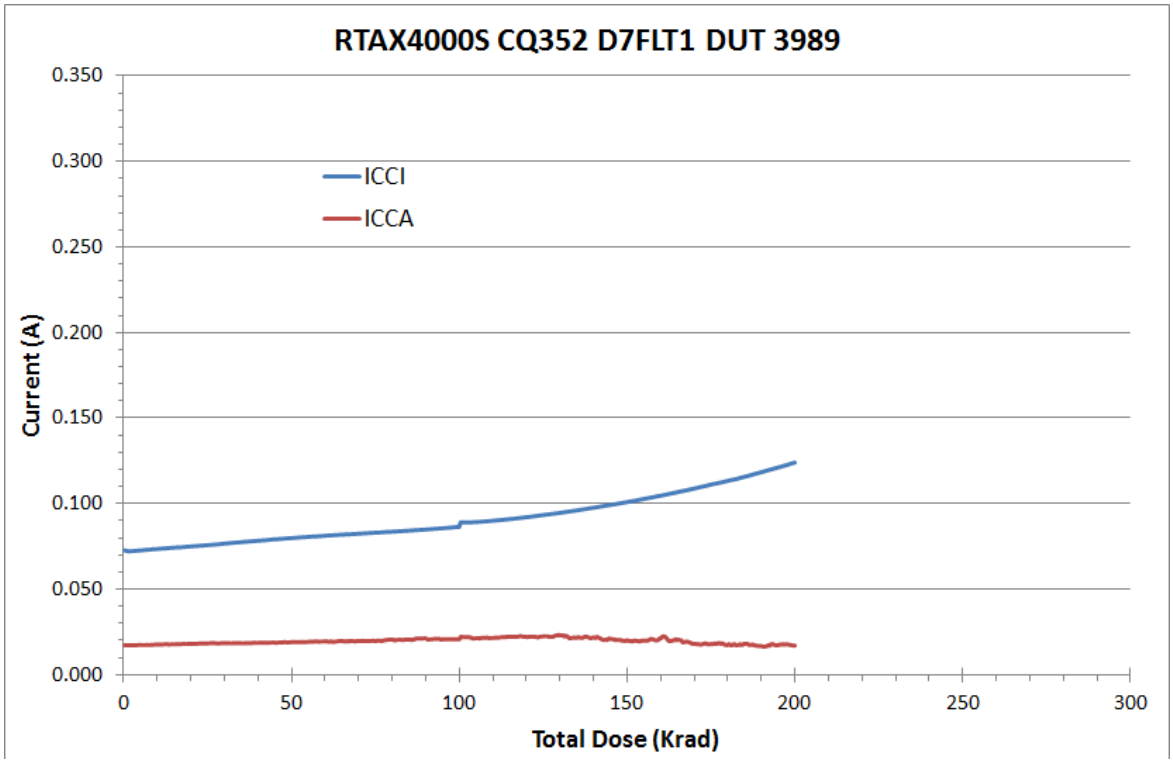

Figure 2 DUT 3989 Influx ICCI and ICCA

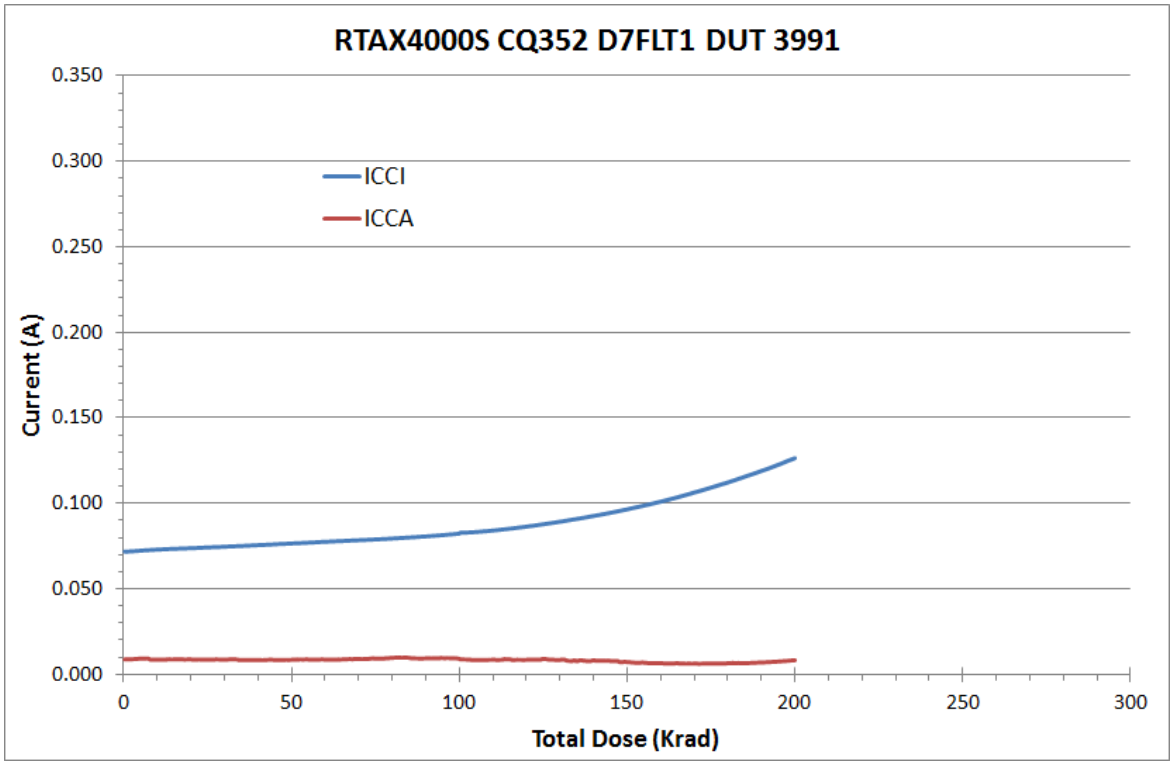

Figure 3 DUT 3991 Influx ICCI and ICCA

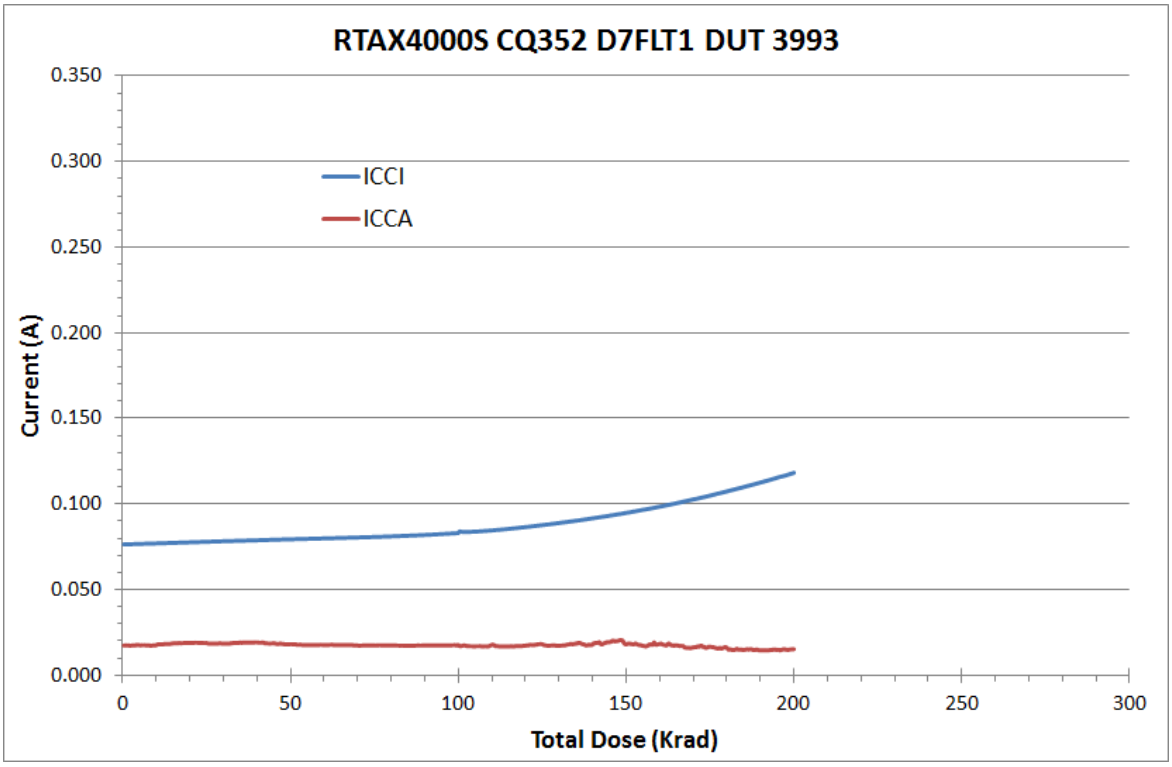

Figure 4 DUT 3993 Influx ICCI and ICCA

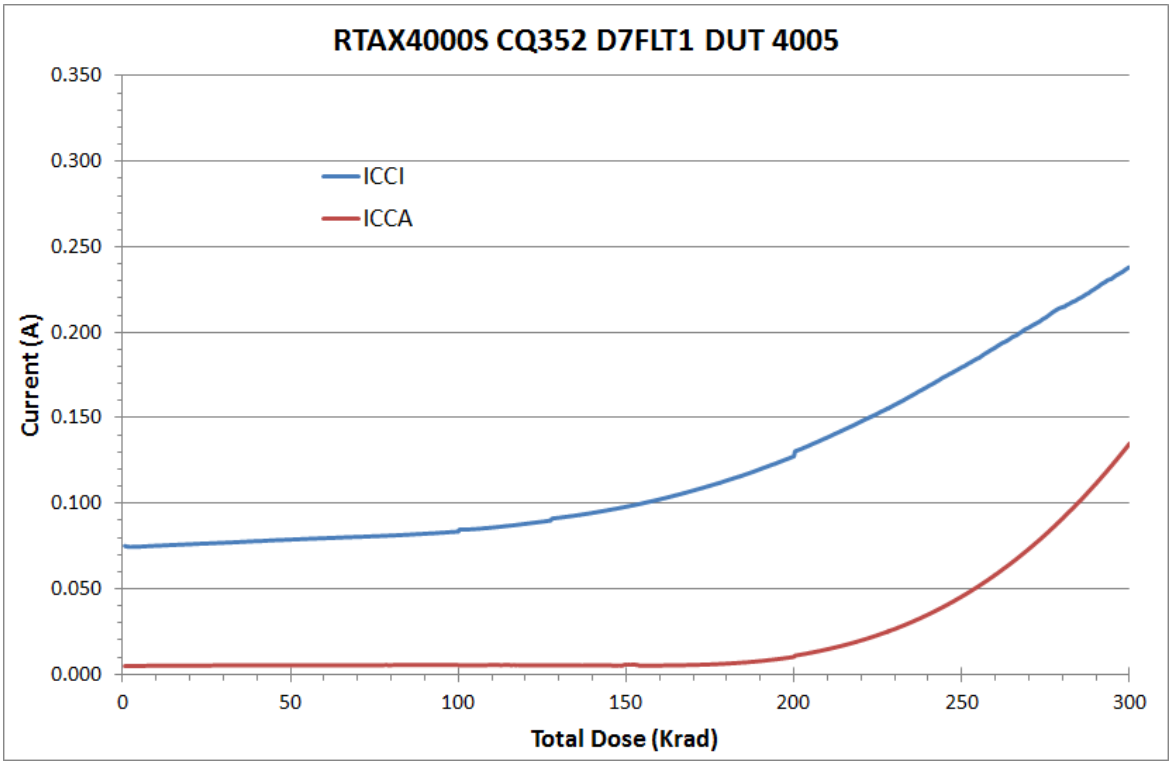

Figure 5 DUT 4005 Influx ICCI and ICCA

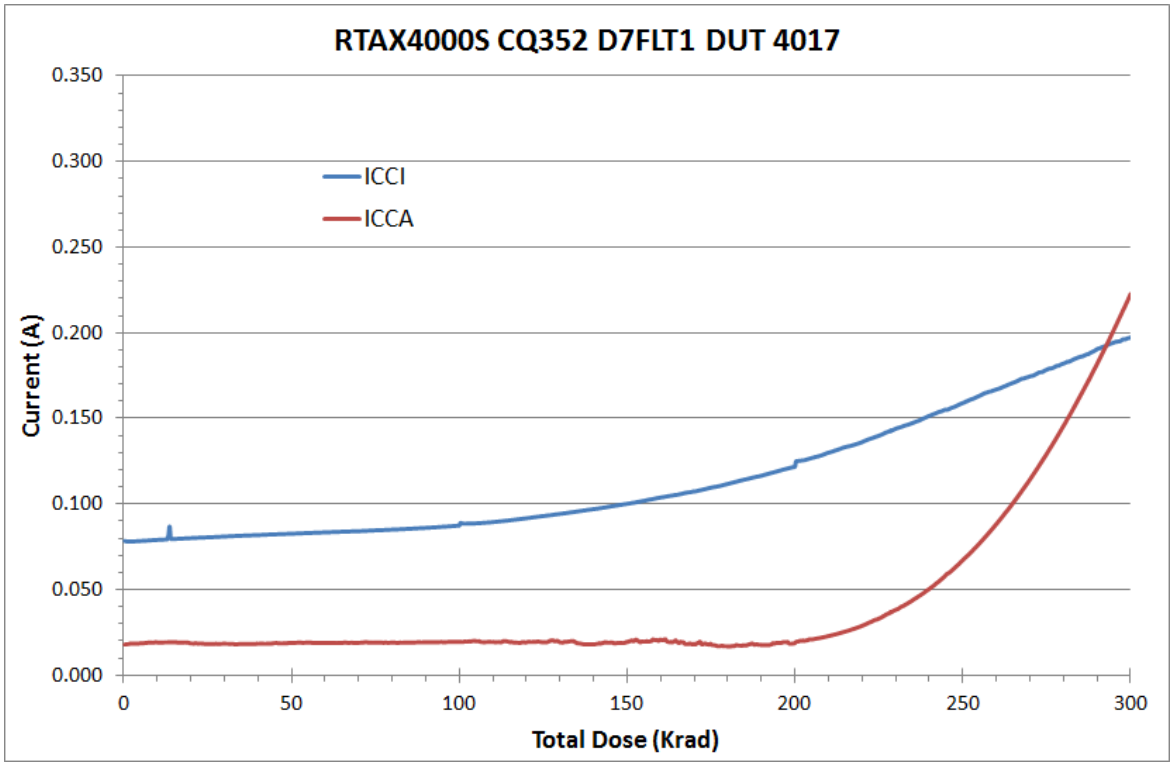

Figure 6 DUT 4017 Influx ICCI and ICCA

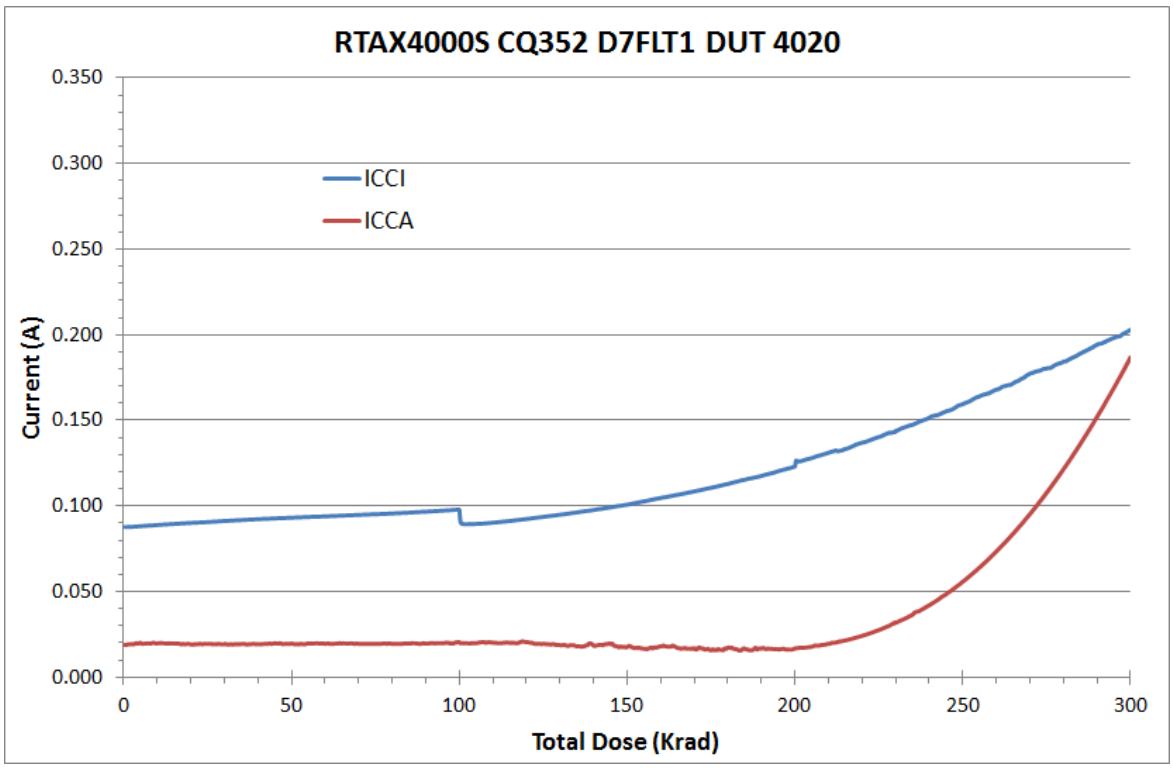

Figure 7 DUT 4020 Influx ICCI and ICCA

C. Single-Ended 3.3 V LVTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design often just input and output buffers starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. The difference between the pre-irradiation and post-annealing data is usually negligibly small.

The pre-irradiation and post-annealing single-ended VIL and VIH are tested and recorded as pass or fail. In each case, the pre-irradiation and post-annealing both passed with respect to the specification.

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 6 and 7. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 6 Pre-Irradiation and Post-Annealing VOL (mV)

Pin \ DUT(Dose)	3989 (200 krad)		3991 (200 krad)		3993 (200 krad)		4005 (300 krad)		4017 (300 krad)		4020 (300 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	153.8	191.8	192.0	188.2	190.9	208.4	207.3	187.0	195.5	165.6	196.2	153.8
Array_out_EAQ_1	153.4	194.0	190.9	179.3	187.1	215.9	205.6	182.3	195.2	164.4	196.0	153.4
Array_out_EAQ_2	149.9	192.9	186.3	179.9	170.6	196.8	210.5	177.0	197.7	164.9	188.9	149.9
Global_Monitor_EAQ	153.9	195.4	191.3	180.3	195.0	209.2	213.5	181.9	202.7	168.0	196.4	153.9
Shiftout3	151.5	195.6	188.7	184.6	195.2	194.9	208.3	188.5	198.1	164.6	195.3	151.5
Shiftout7	153.8	191.8	192.0	188.2	190.9	208.4	207.3	187.0	195.5	165.6	196.2	153.8
Shiftout8	143.1	185.8	179.4	178.8	186.8	211.5	203.7	183.2	189.3	152.1	182.6	143.1
RAM_Monitor_EAQ	146.7	189.2	182.8	183.9	187.9	198.3	205.5	186.0	192.6	154.2	191.8	146.7
RAM_out_EAQ_0	143.3	185.8	179.7	178.9	186.8	209.0	203.7	183.2	189.4	152.4	182.4	143.3
RAM_out_EAQ_4	146.0	186.9	181.7	182.7	186.7	196.8	203.2	184.8	191.2	149.9	188.2	146.0
RAM_out_EAQ_8	142.7	186.5	180.0	182.8	186.0	194.1	200.0	182.4	188.4	150.3	188.8	142.7

Table 7 Pre-Irradiation and Post-Annealing VOH (V)

Pin \ DUT(Dose)	3989 (200 krad)		3991 (200 krad)		3993 (200 krad)		4005 (300 krad)		4017 (300 krad)		4020 (300 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	2.76	2.71	2.72	2.72	2.73	2.70	2.70	2.72	2.71	2.75	2.71	2.76
Array_out_EAQ_1	2.76	2.71	2.72	2.73	2.71	2.71	2.70	2.72	2.71	2.75	2.71	2.76
Array_out_EAQ_2	2.76	2.72	2.72	2.72	2.72	2.71	2.70	2.72	2.71	2.75	2.72	2.76
Global_Monitor_EAQ	2.76	2.71	2.72	2.72	2.72	2.69	2.69	2.72	2.71	2.75	2.71	2.76
Shiftout3	2.76	2.71	2.72	2.72	2.72	2.71	2.70	2.72	2.71	2.75	2.71	2.76
Shiftout7	2.76	2.71	2.72	2.72	2.73	2.70	2.70	2.72	2.71	2.75	2.71	2.76
Shiftout8	2.76	2.72	2.72	2.72	2.72	2.69	2.70	2.72	2.71	2.76	2.72	2.76
RAM_Monitor_EAQ	2.76	2.71	2.72	2.72	2.71	2.70	2.69	2.72	2.71	2.76	2.71	2.76
RAM_out_EAQ_0	2.76	2.72	2.72	2.72	2.72	2.69	2.70	2.72	2.71	2.76	2.72	2.76
RAM_out_EAQ_4	2.76	2.71	2.72	2.72	2.71	2.70	2.69	2.72	2.71	2.76	2.71	2.76
RAM_out_EAQ_8	2.76	2.71	2.72	2.72	2.71	2.70	2.70	2.72	2.71	2.76	2.71	2.76

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is well below 10% (except one read point of a sample shows 10.6% post-300krad).

Table 8 Radiation-Induced Propagation Delay Degradations

Delay (µs)

DUT	Total Dose	Pre-rad.	Post-100krad	Post-200krad	Post-300krad	Post-ann.
3989	200 krad	6.395	6.460	6.475	-	6.325
3991	200 krad	6.690	6.730	6.760	-	6.625
3993	200 krad	6.415	6.465	6.495	-	6.345
4005	300 krad	6.735	6.795	6.830	7.230	6.665
4017	300 krad	6.400	6.470	6.510	7.080	6.340
4020	300 krad	6.525	6.600	6.630	6.760	6.430

Radiation Δ (%)

DUT	Total Dose	Pre-rad.	Post-100krad	Post-200krad	Post-300krad	Post-ann.
3989	200 krad	-	1.0%	1.3%	-	-1.1%
3991	200 krad	-	0.6%	1.0%	-	-1.0%
3993	200 krad	-	0.8%	1.2%	-	-1.1%
4005	300 krad	-	0.9%	1.4%	7.3%	-1.0%
4017	300 krad	-	1.1%	1.7%	10.6%	-0.9%
4020	300 krad	-	1.1%	1.6%	3.6%	-1.5%

F. Transition Time

Figure 8a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

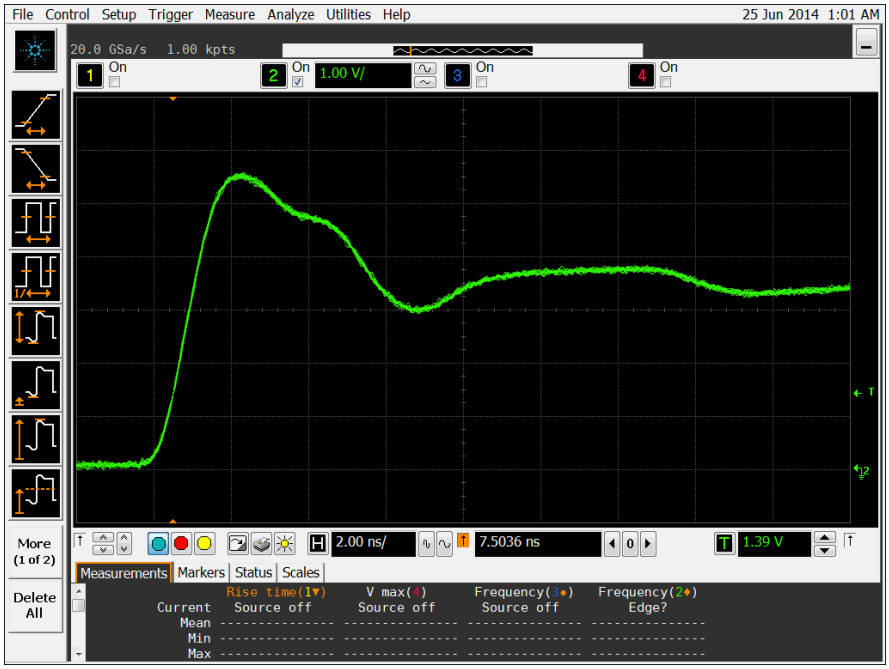

Figure 8a DUT 3989 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

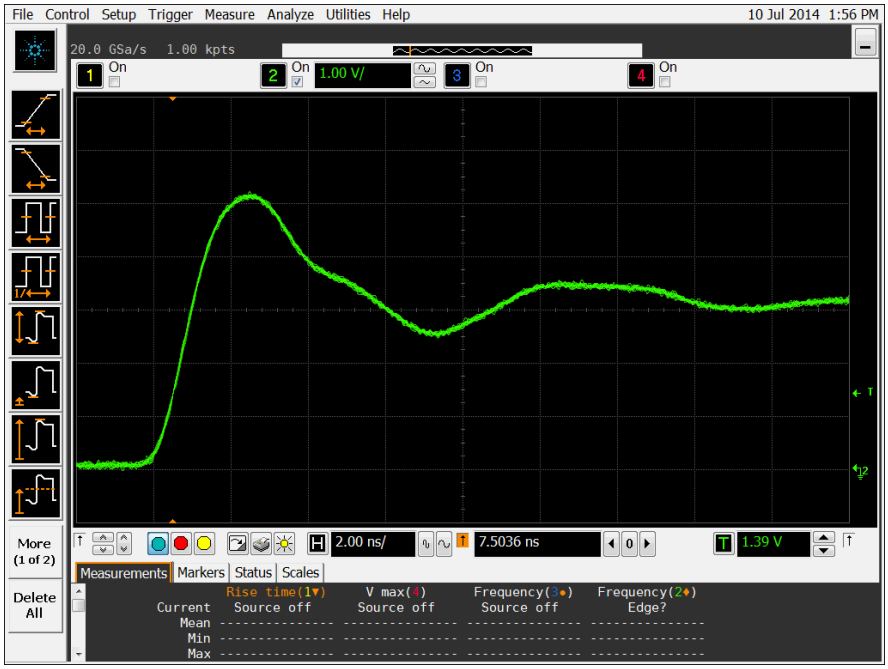

Figure 8b DUT 3989 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

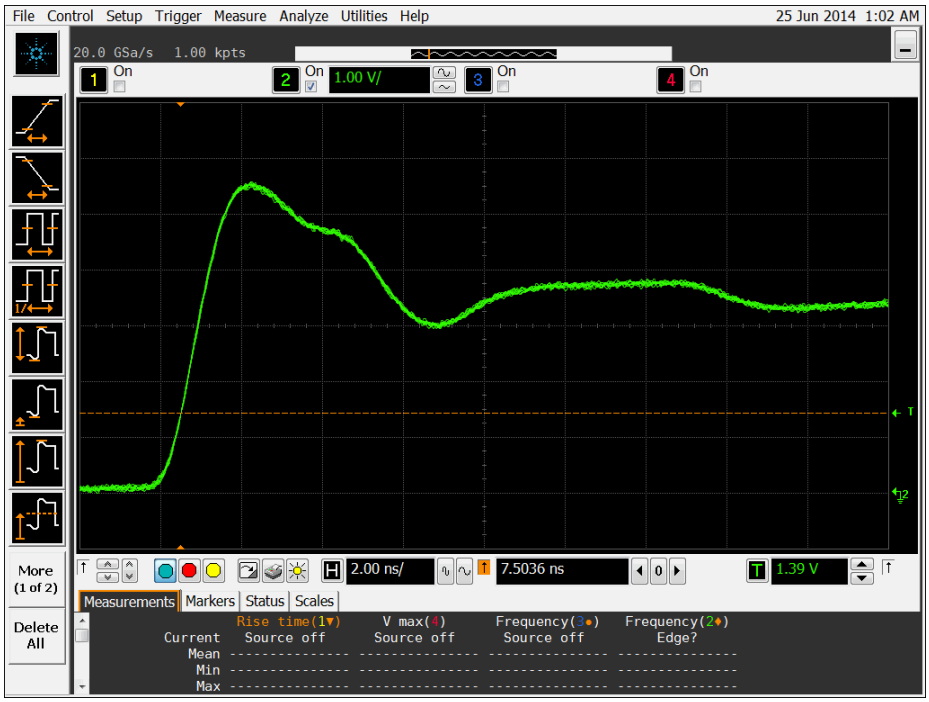

Figure 9a DUT 3991 Pre-irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

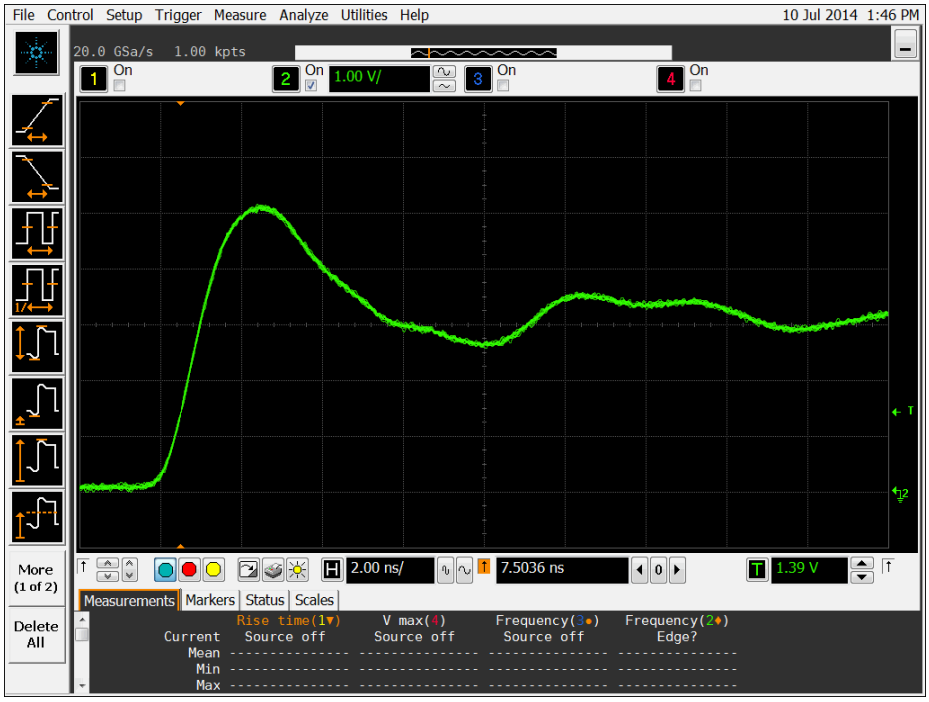

Figure 9b DUT 3991 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

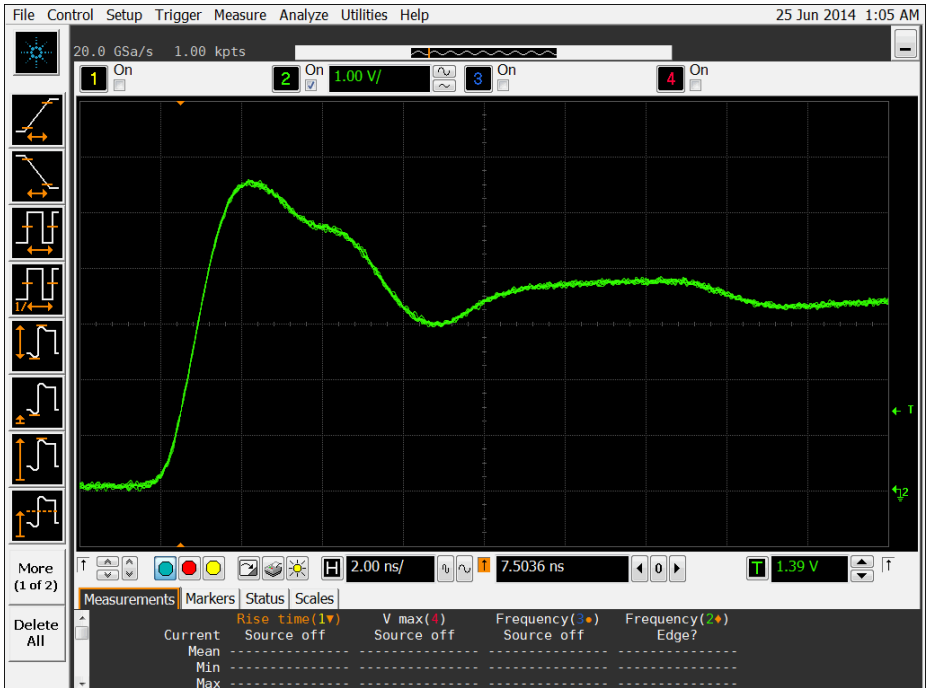

Figure 10a DUT 3993 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

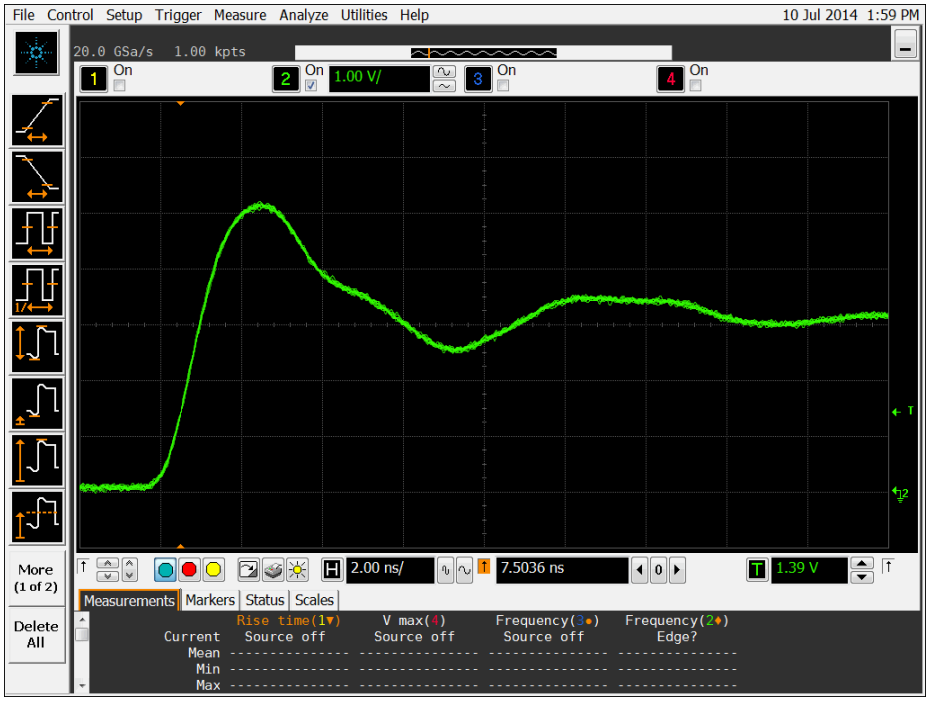

Figure 10b DUT 3993 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

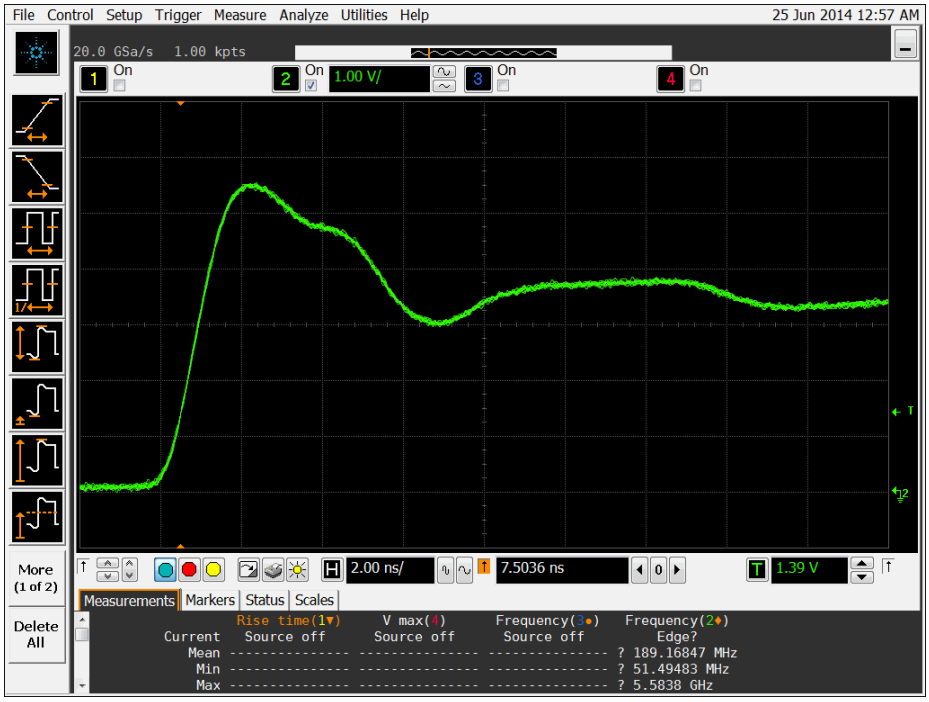

Figure 11a DUT 4005 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

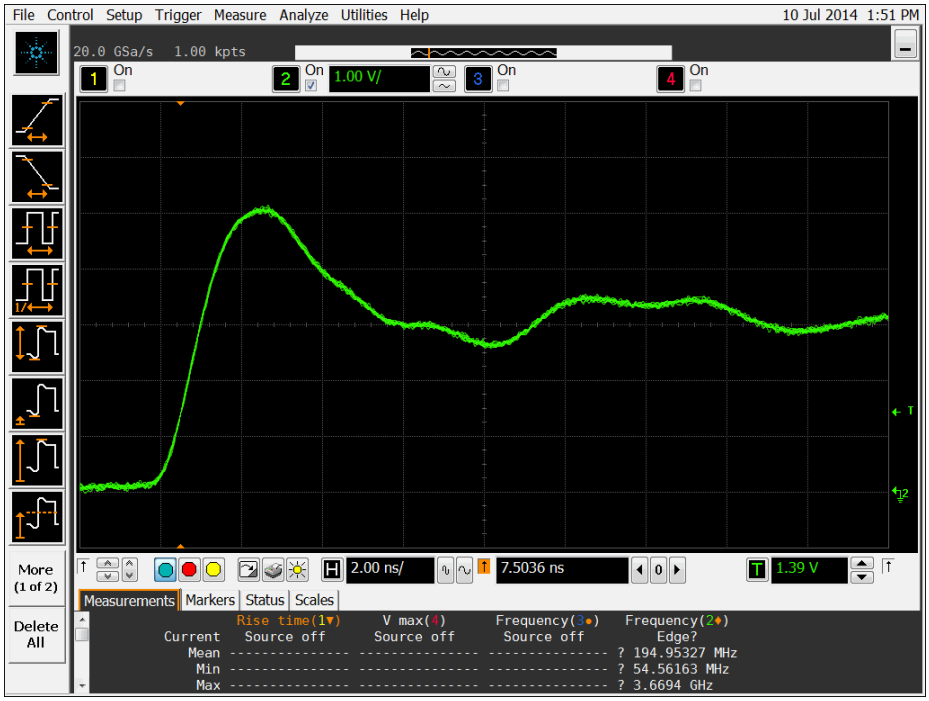

Figure 11b DUT 4005 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

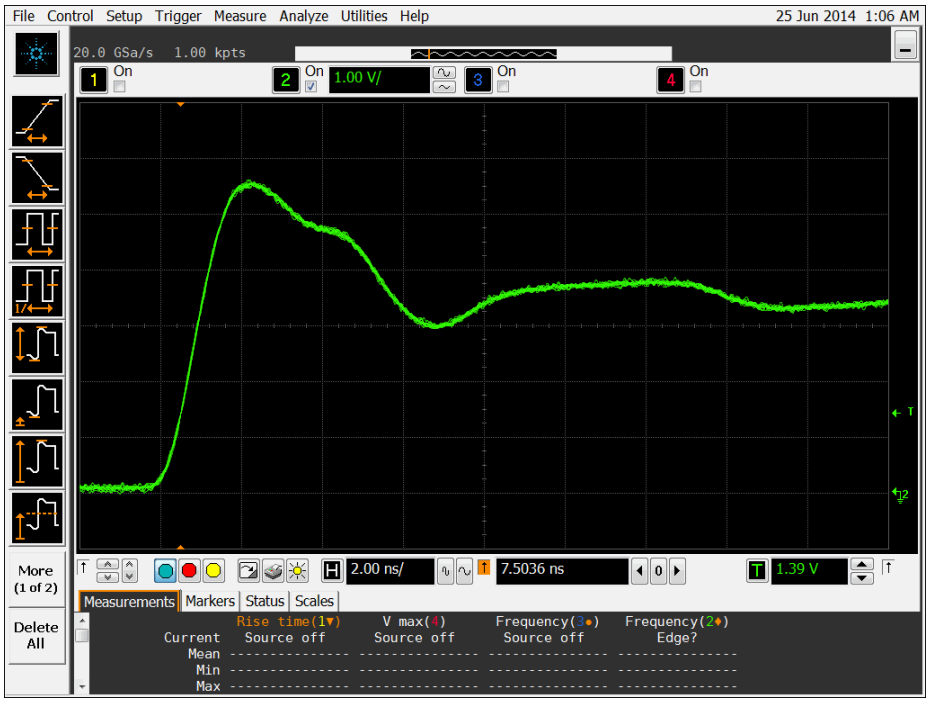

Figure 12a DUT 4017 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

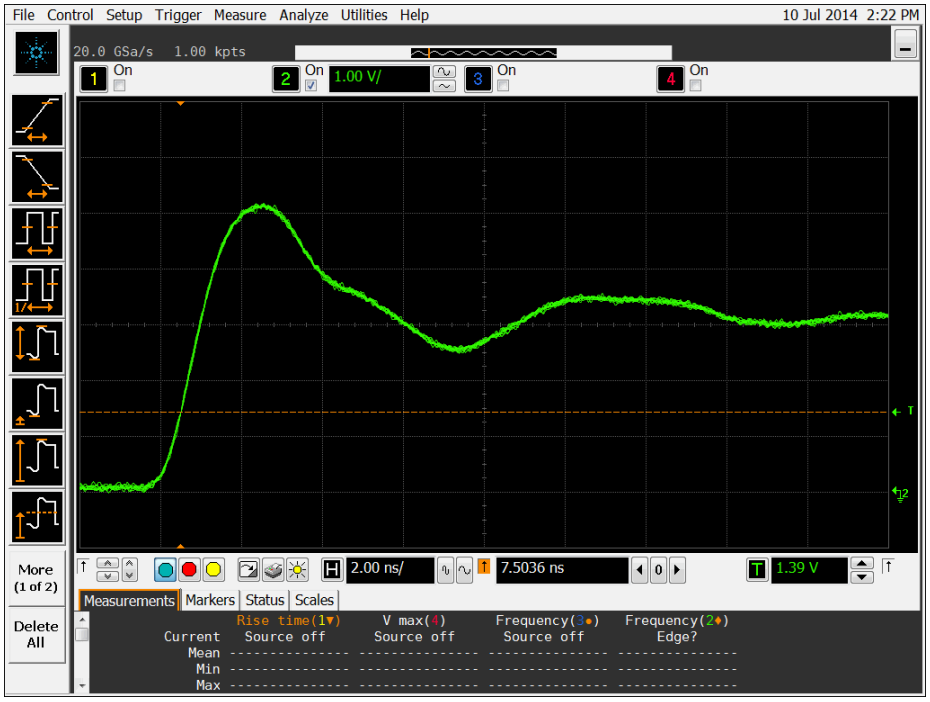

Figure 12b DUT 4017 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

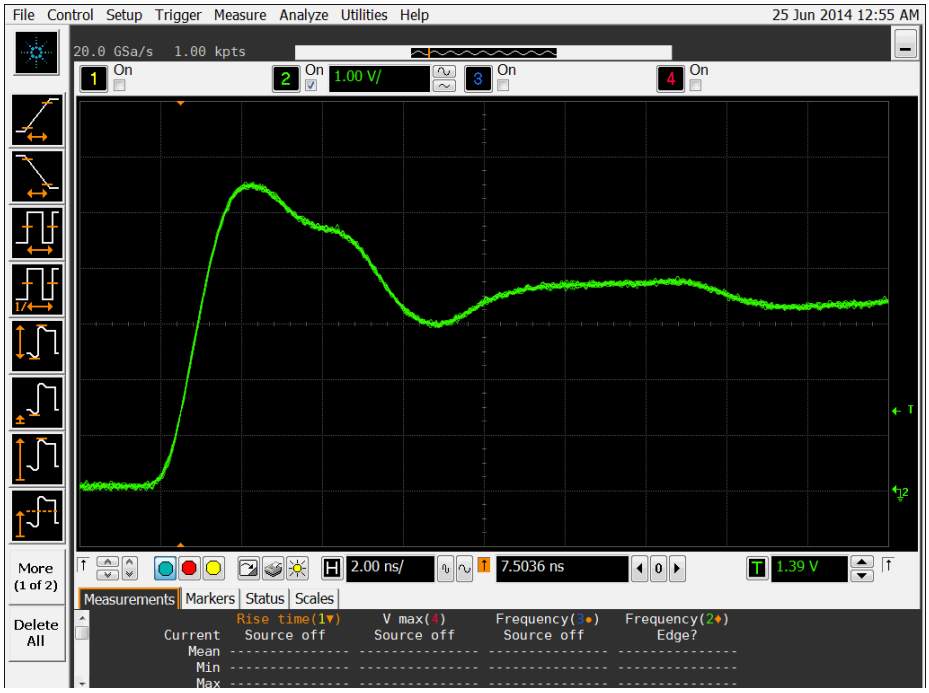

Figure 13a DUT 4020 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

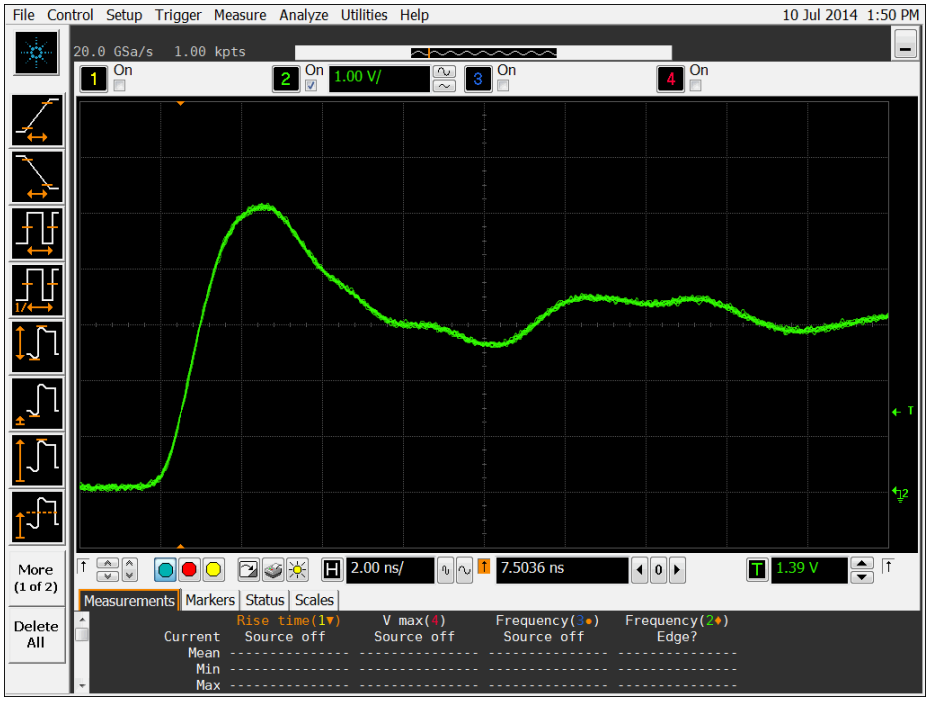

Figure 13b DUT 4020 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

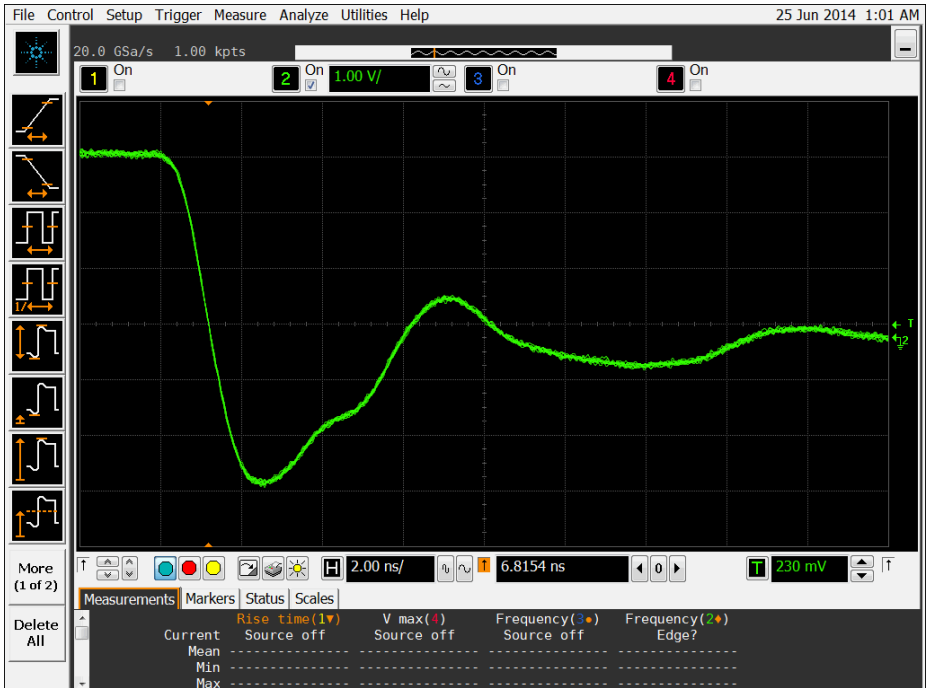

Figure 14a DUT 3989 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

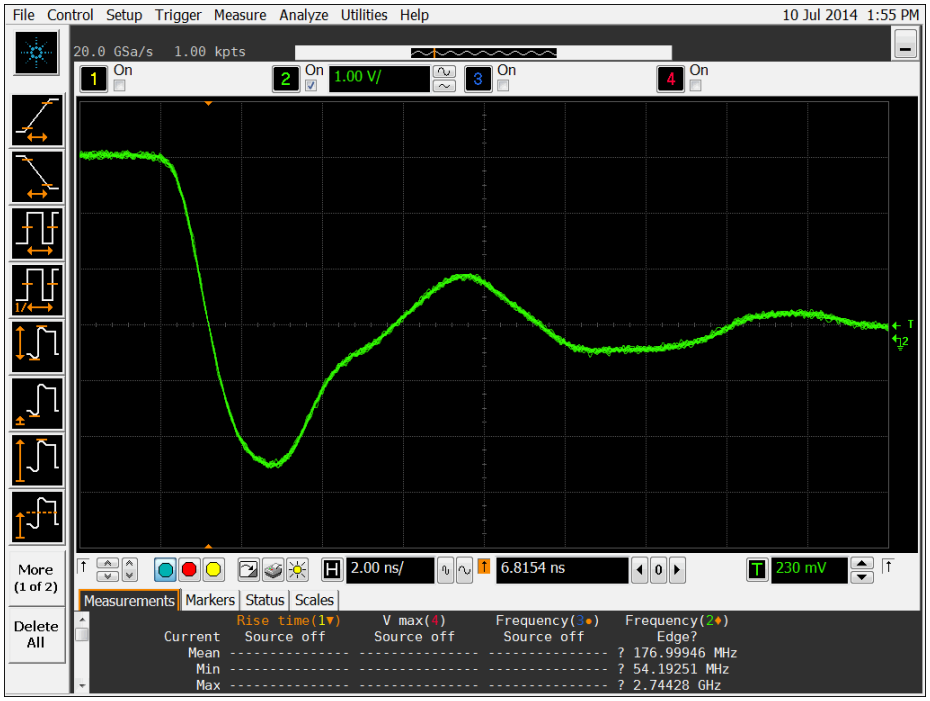

Figure 14b DUT 3989 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

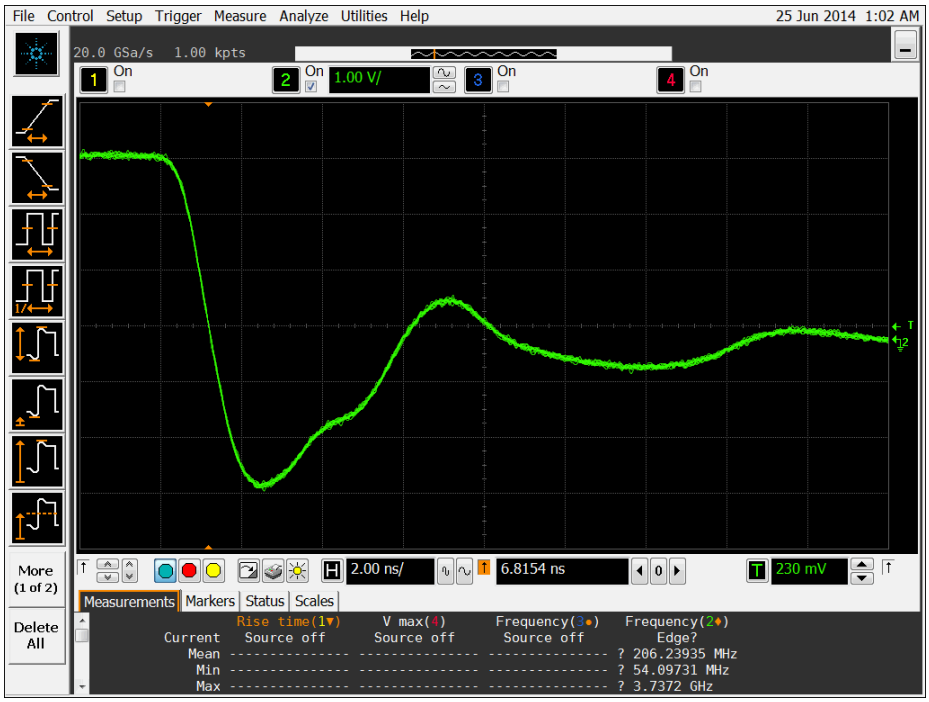

Figure 15a DUT 3991 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

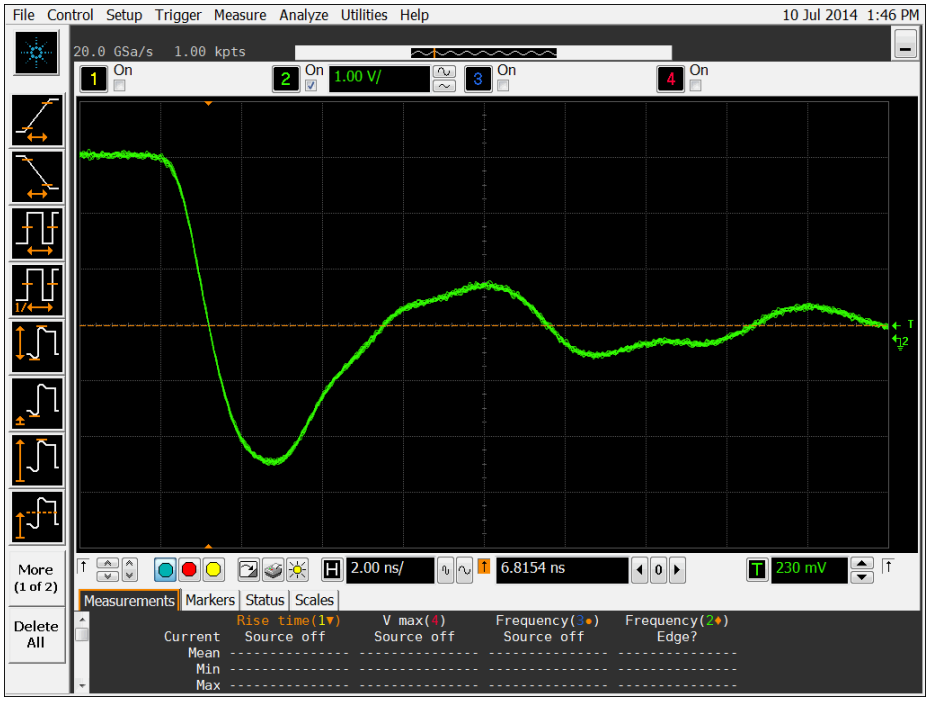

Figure 15b DUT 3991 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

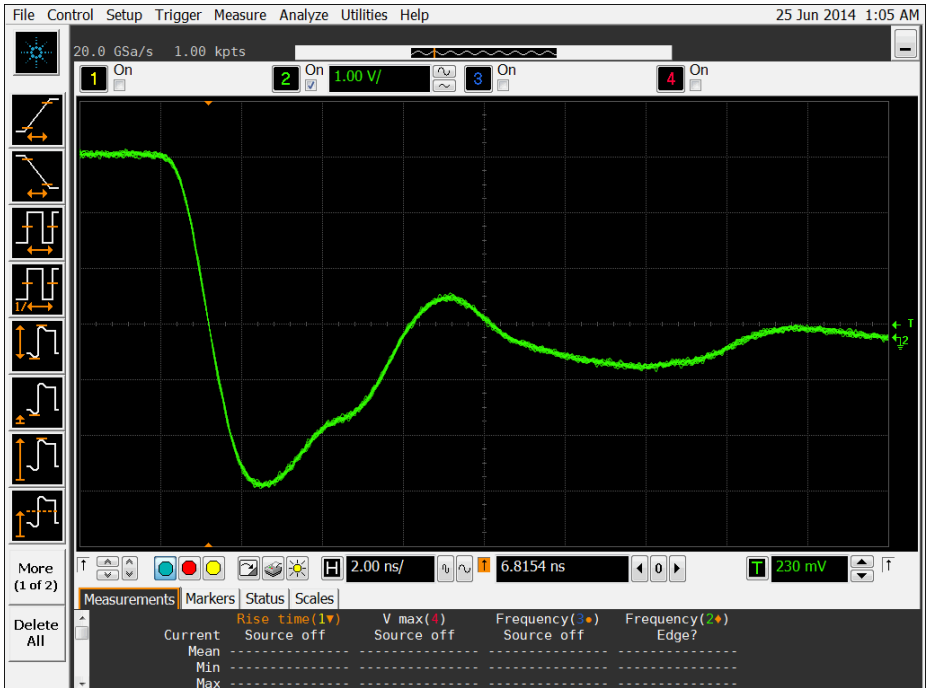

Figure 16a DUT 3993 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

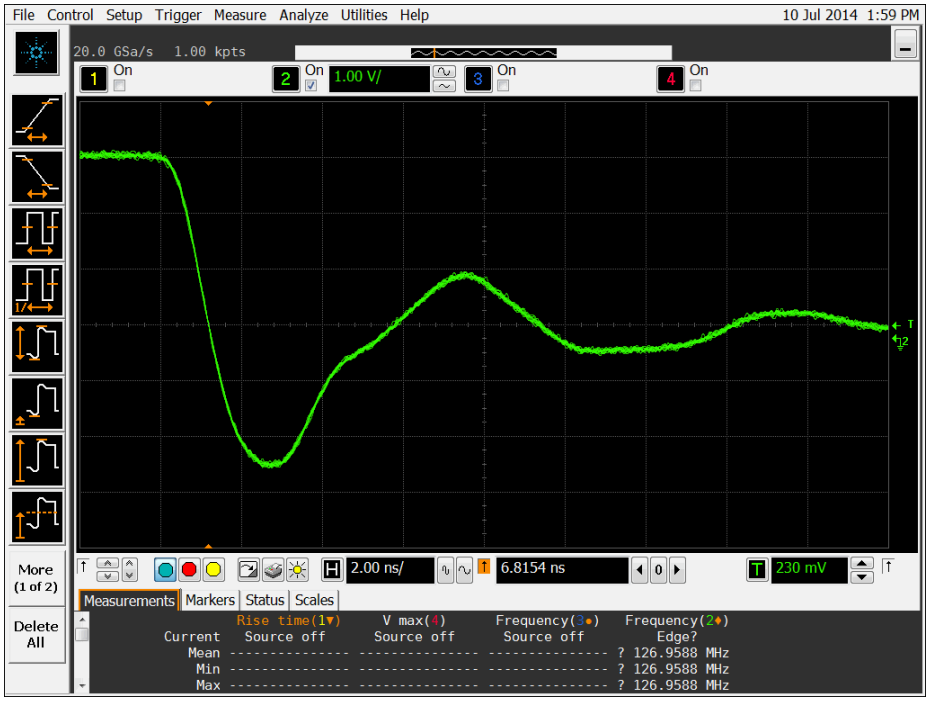

Figure 16b DUT 3993 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

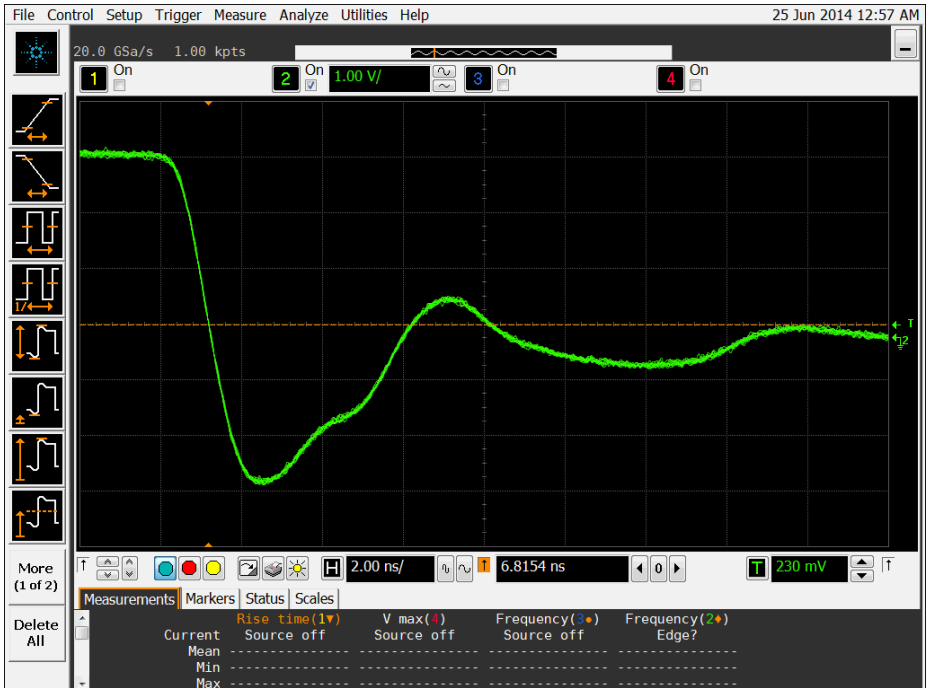

Figure 17a DUT 4005 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

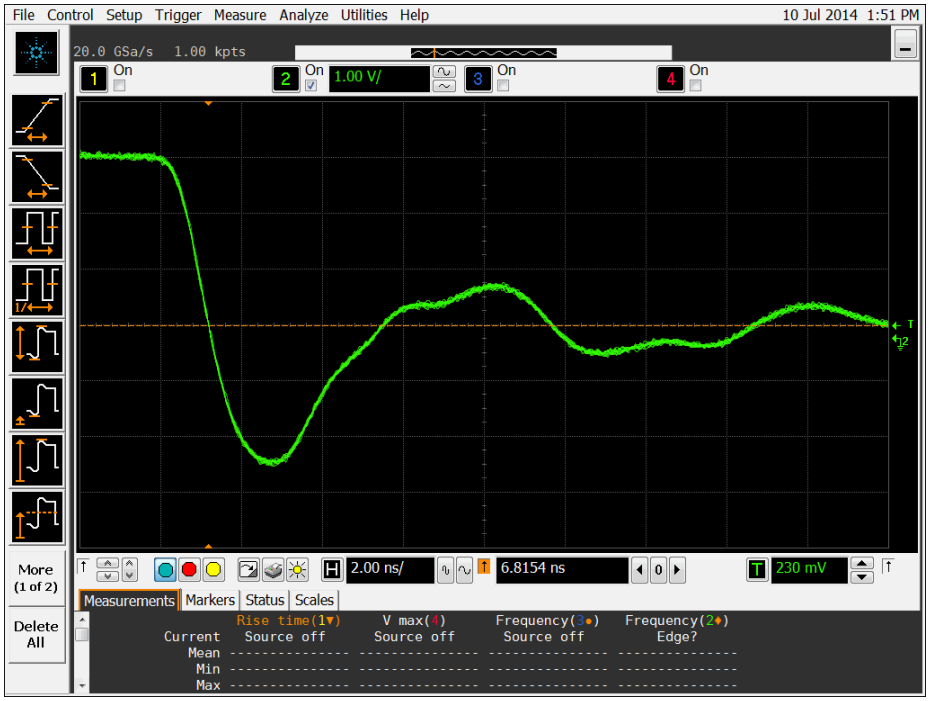

Figure 17b DUT 4005 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

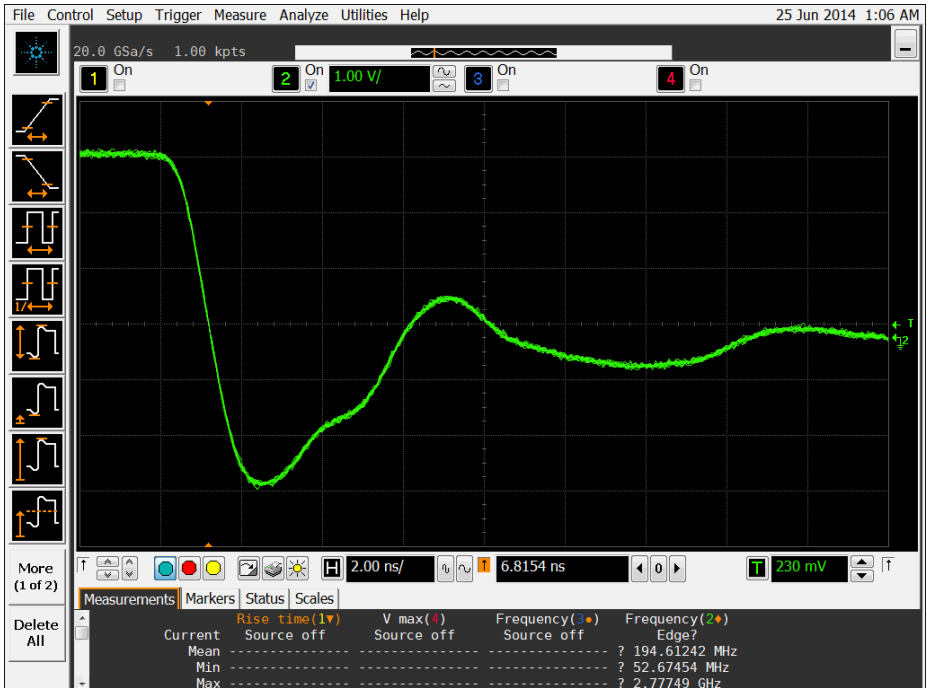

Figure 18a DUT 4017 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

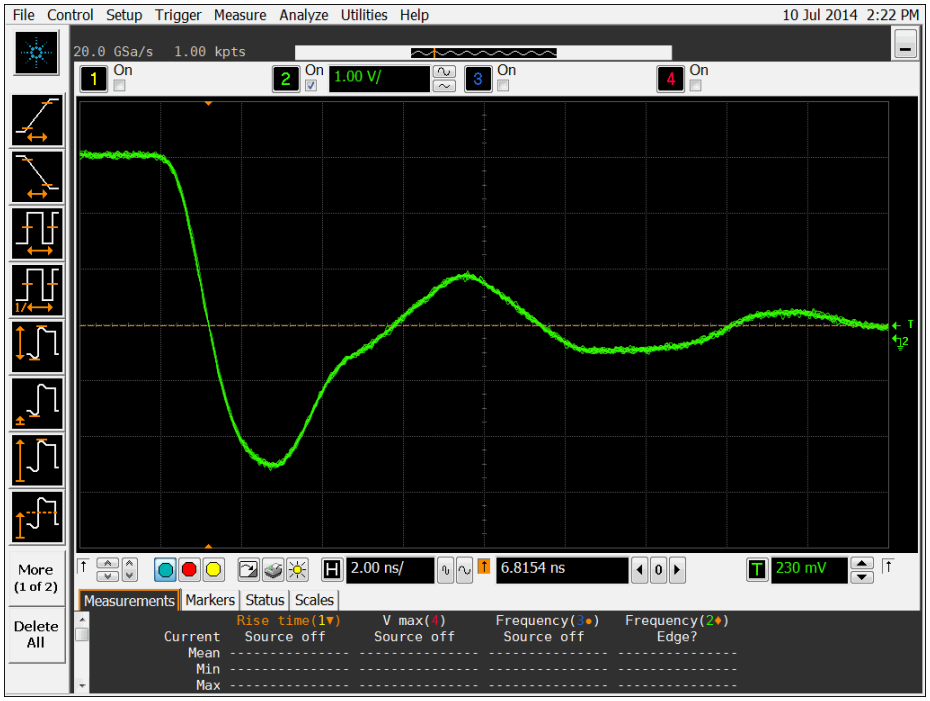

Figure 18b DUT 4017 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

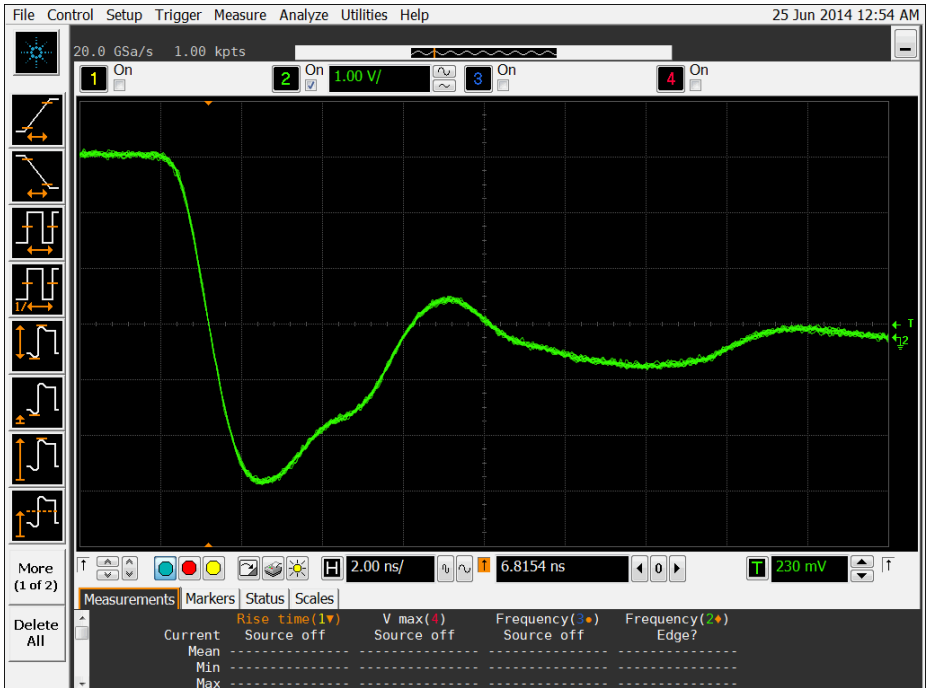

Figure 19a DUT 4020 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

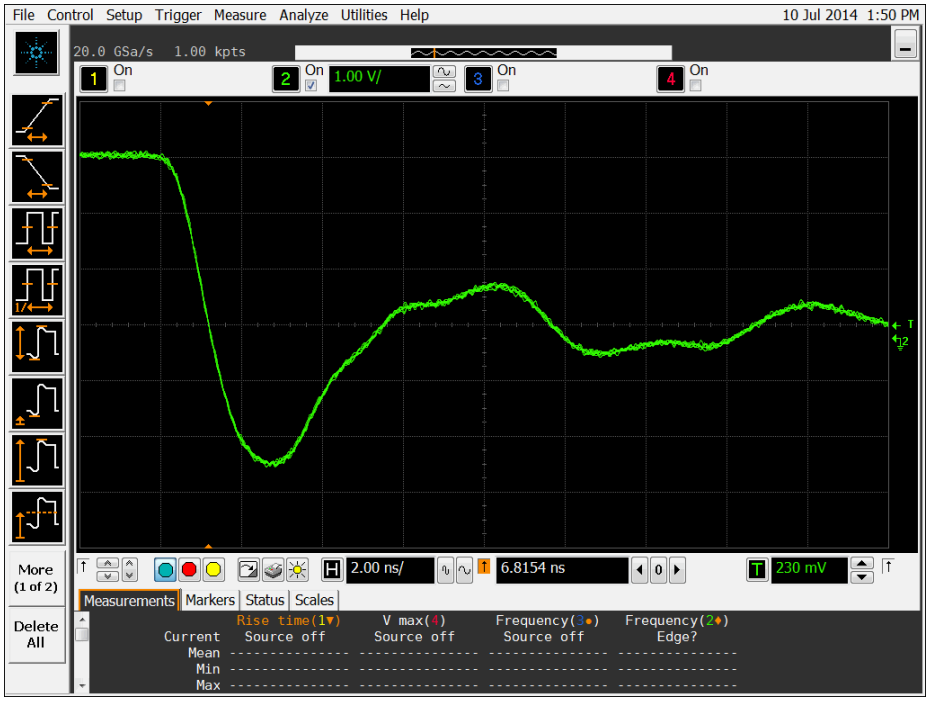

Figure 19b DUT 4020 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

Appendix A: DUT Bias Diagram

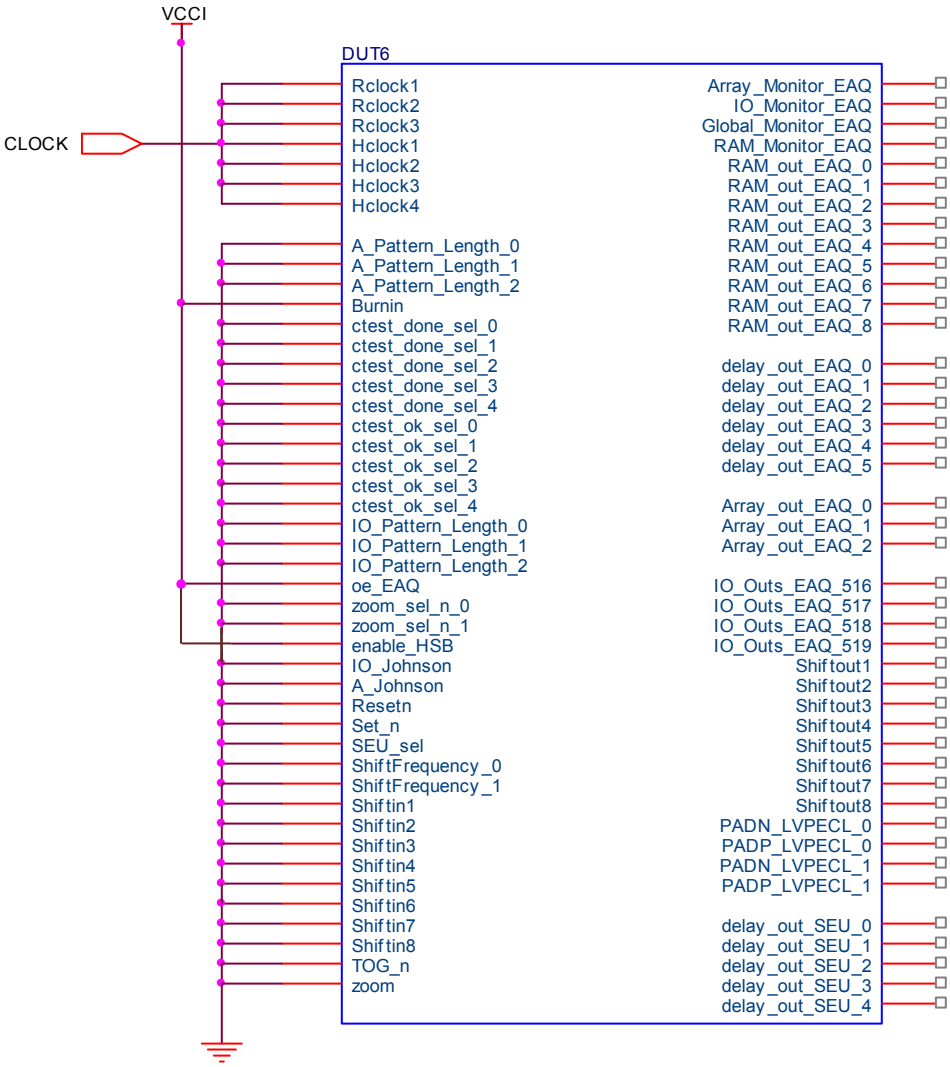

Figure A1 I/O Bias During Irradiation

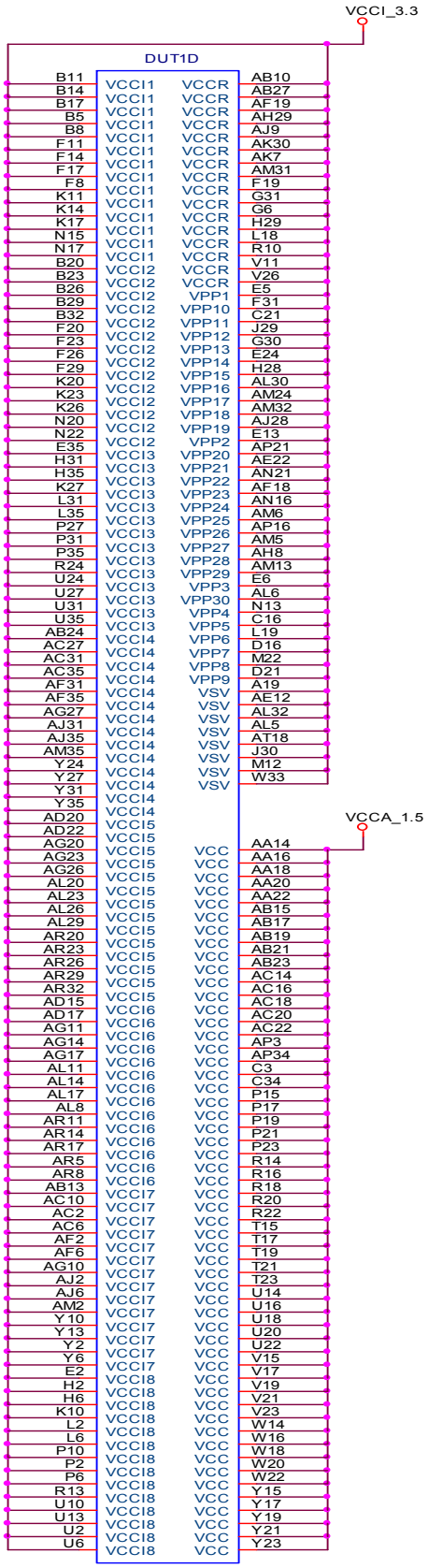

Figure A2 Power supply, Ground and Special Pins Bias During Irradiation

Appendix B: Functionality Tests

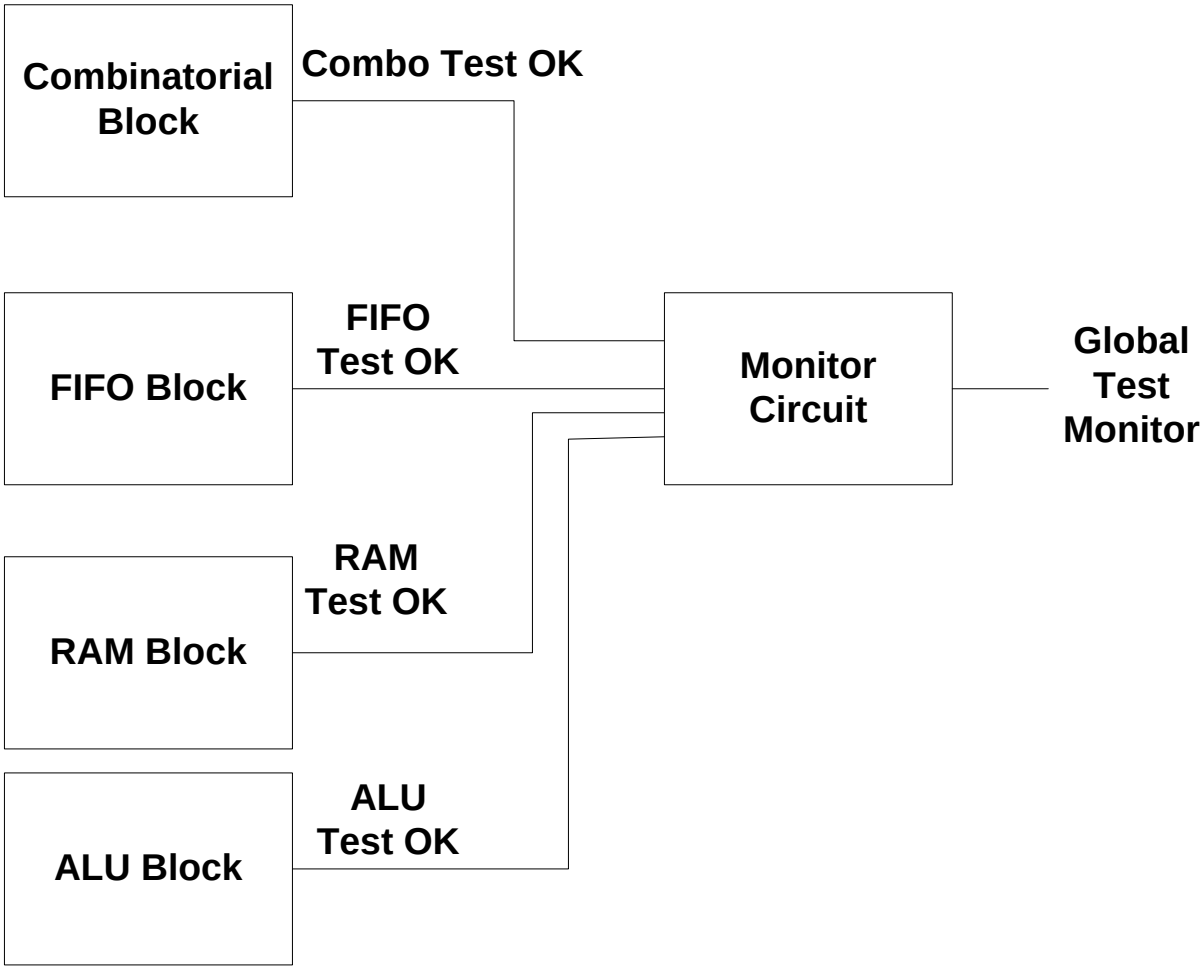

Figure B1 QBI Block – Top-Level Design

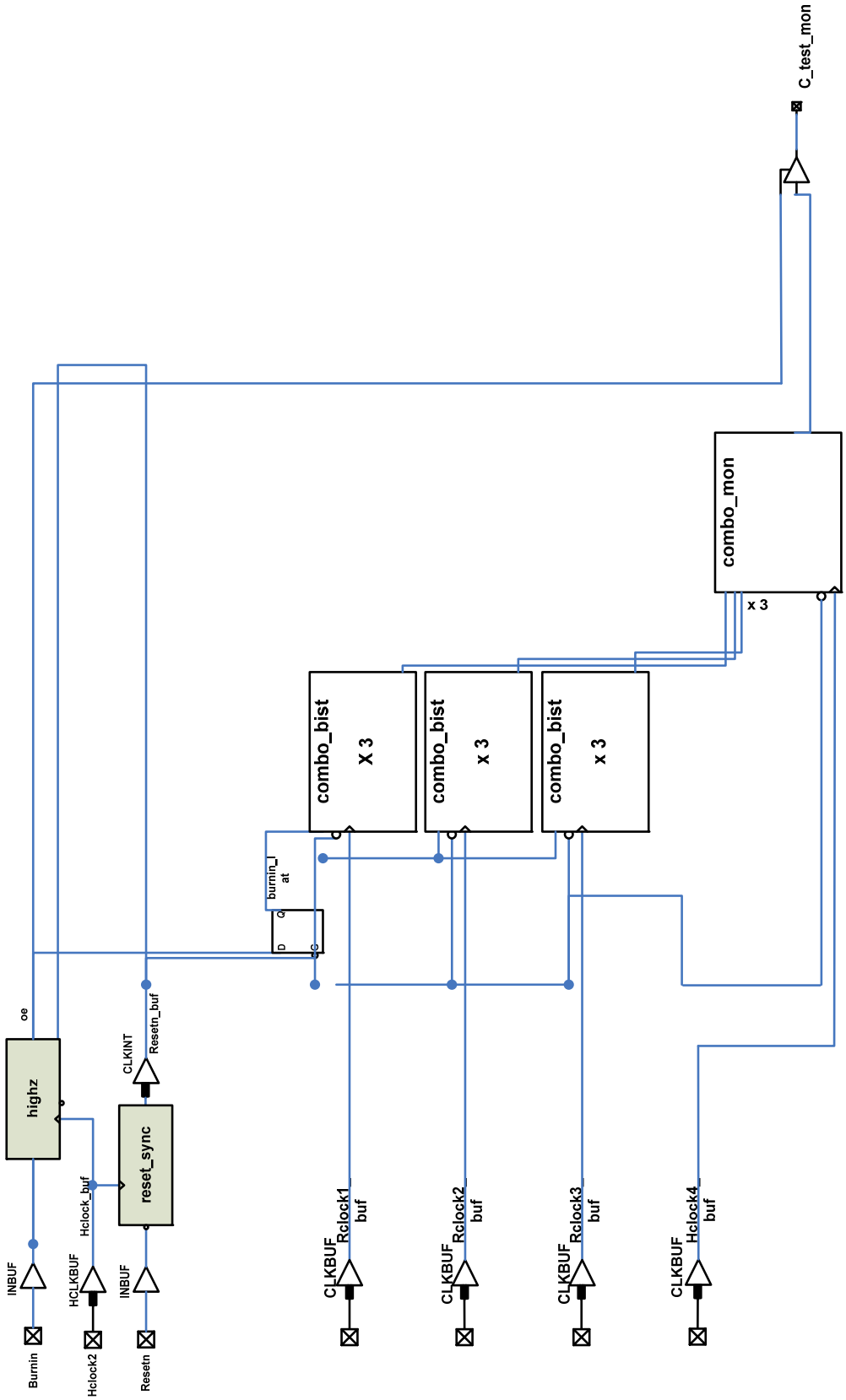

Figure B2 QBI Block – Combinatorial Test (Top Level)

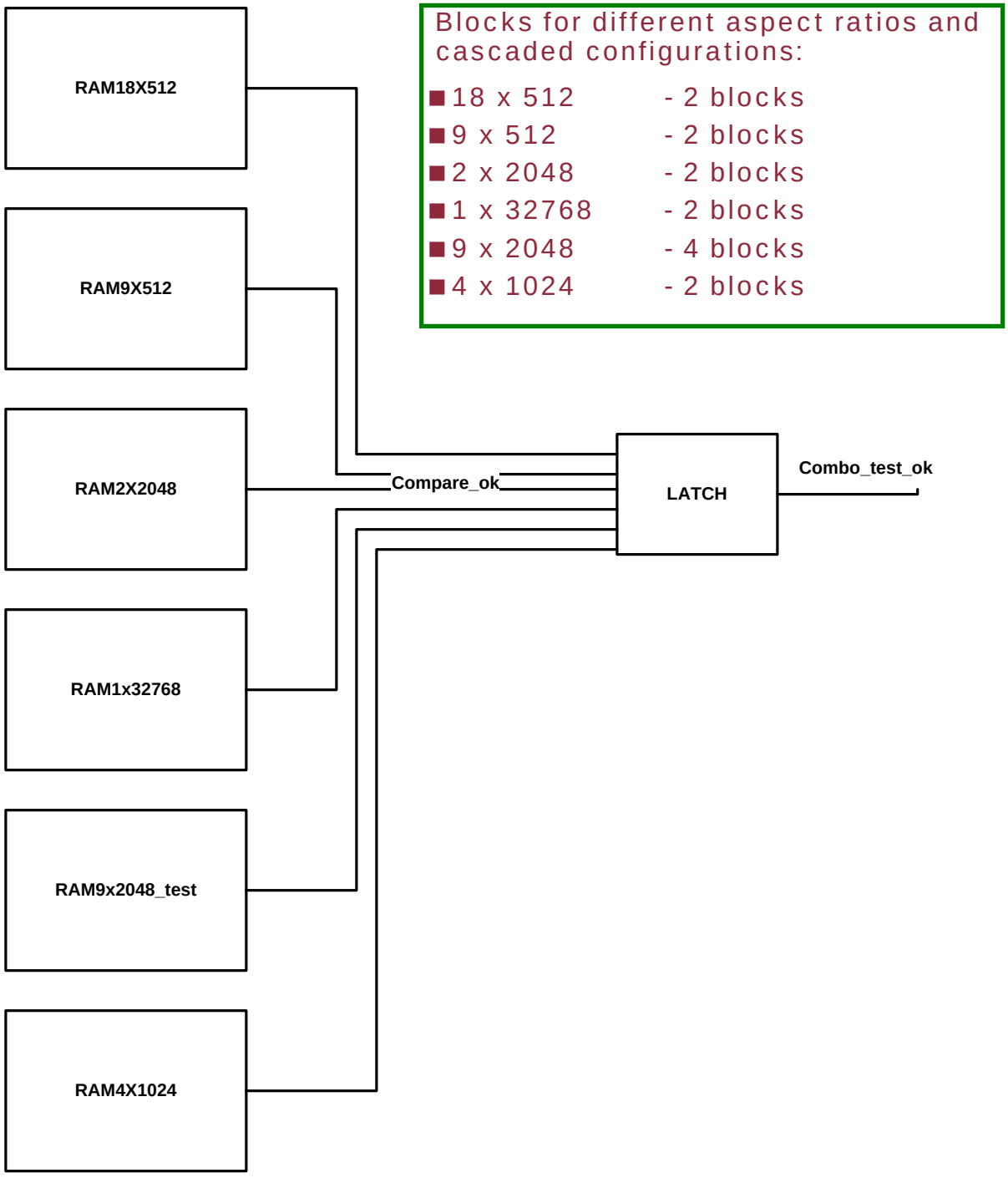

Figure B3 QBI Block – RAM Test (Top Level)

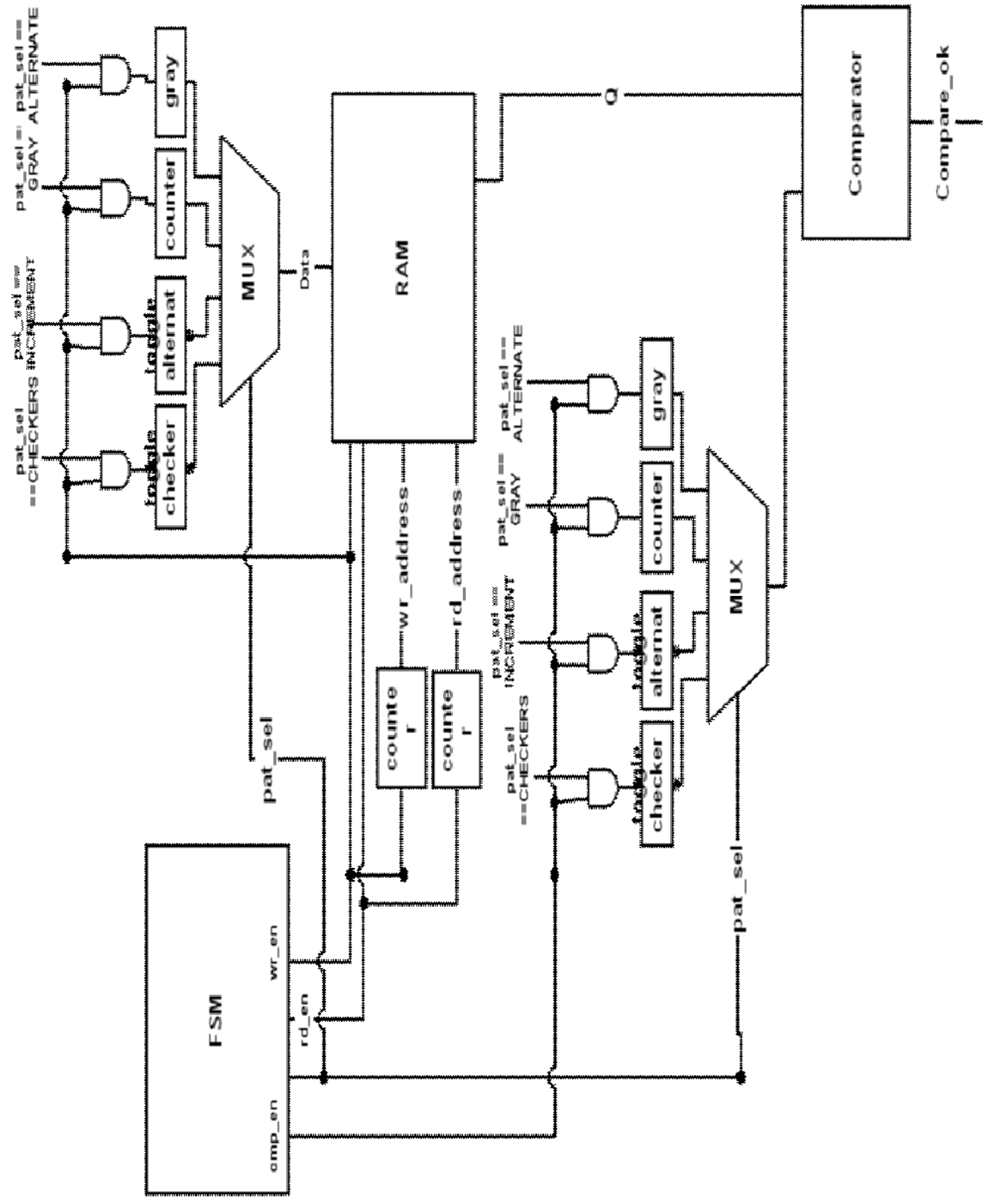

Figure B4 QBI Block – RAM Block

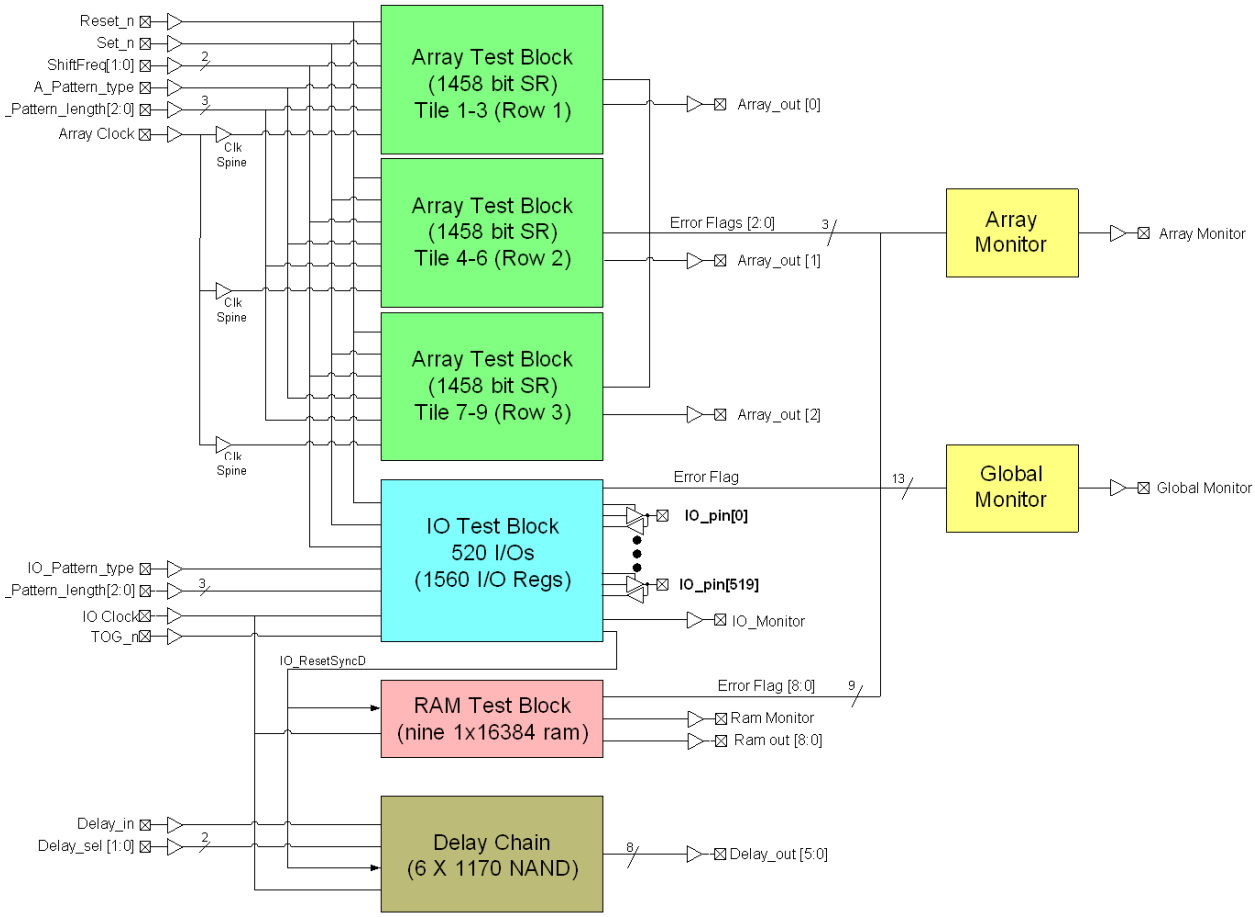

Figure B5 EAQ Block – Top Level

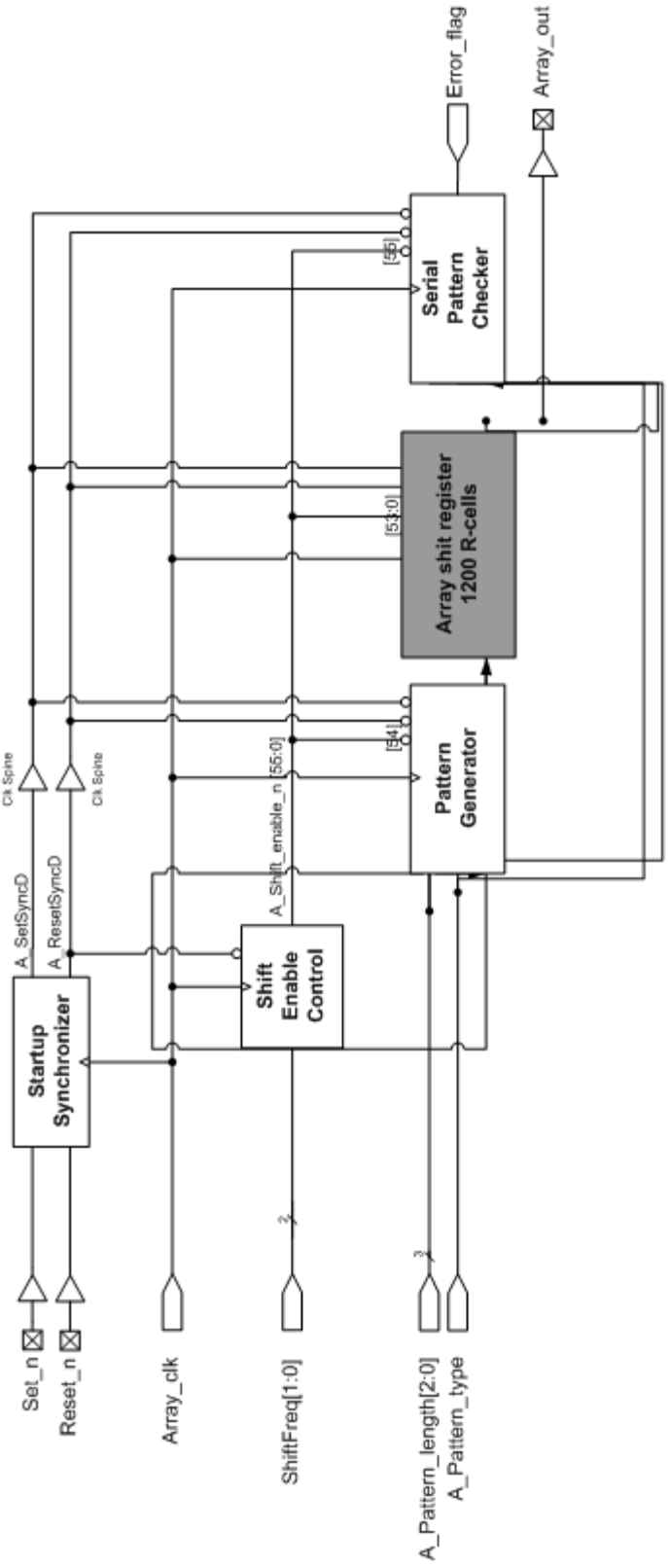

Figure B6 EAQ Block – Array Test (Shift Register)

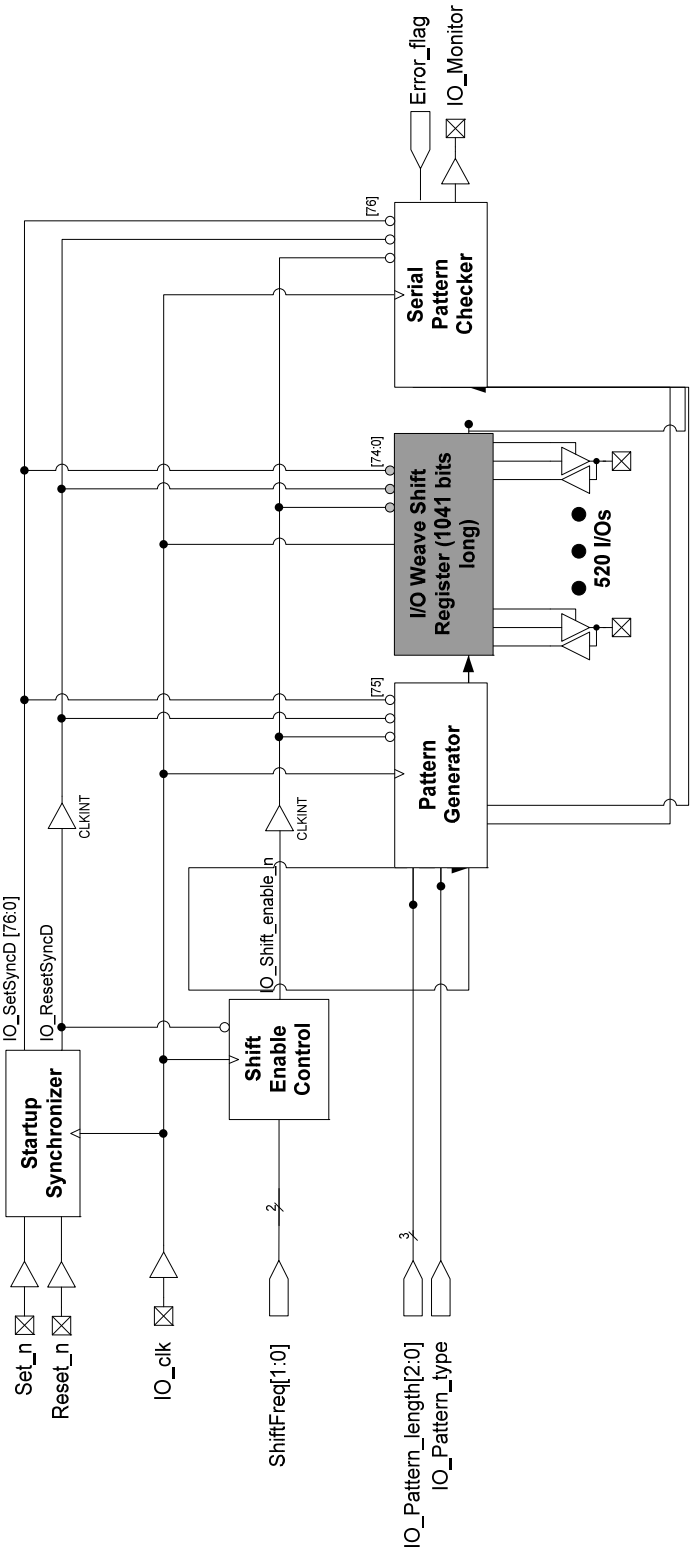

Figure B7 EAQ Block – I/O Test (Top Level)

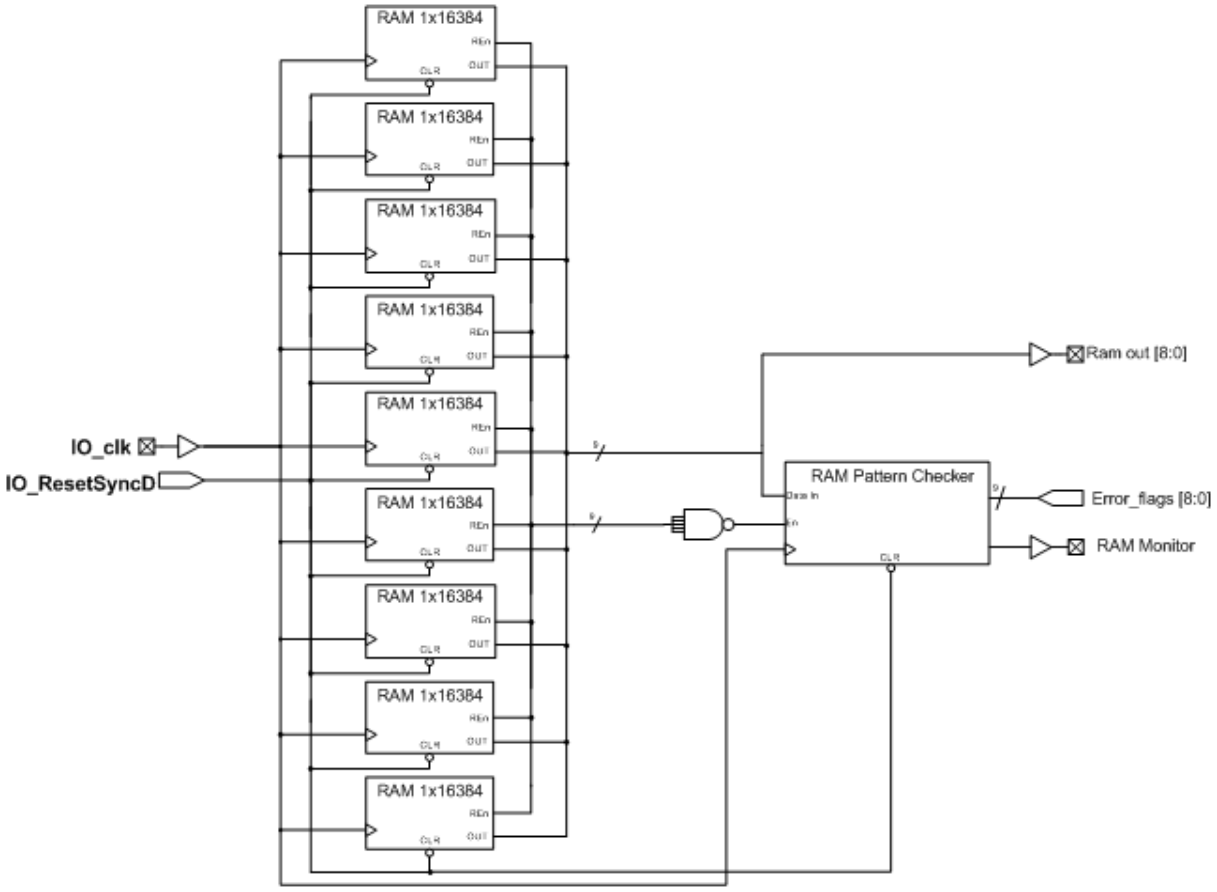

Figure B8 EAQ Block – SRAM Test (Top Level)

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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