Total Ionizing Dose Test Report

No. 16T-RTAX2000D-CQ352E-D5G821

February 17, 2016

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 200 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 200 krad (SiO_2)
6. Transition Characteristics	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation, each input and most of the output is grounded through a 1 MΩ resistor; during annealing, each input or output is tied to the ground or VCCI with a 2.7 kΩ resistor. Appendix A contains the schematics of the irradiation-bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000D
Package	CQ352E
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	TOP_AX2000S_TID
Die Lot Number	D5G821
Quantity Tested	5
Serial Number	300 krad(SiO2): 5105, 5106, 5107 200 krad(SiO2): 5112, 5113
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V

B. Test Method

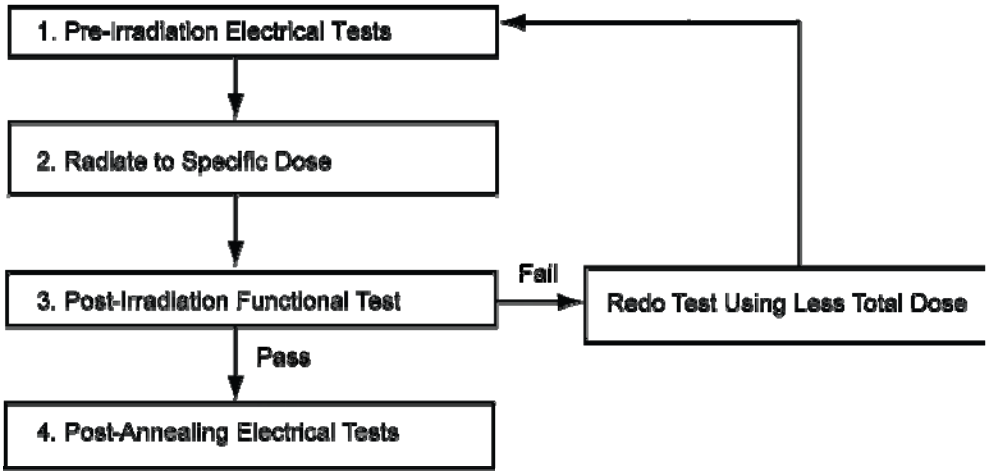

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8, is unnecessary; because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTAX2000D are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization, generic design (TOP_AX2000S_TID) to evaluate total dose effects for typical space applications. Appendix B contains the schematics and Verilog files of this design.

Table 2 lists measured electrical parameters and the corresponding logic design. The functionality is measured on the output pin (O_BS) of a combinational buffer-string with 14,000 buffers, output pins (O_ANDP_CLKF, O_ORP_CLKF, O_FF_CLKF, O_ANDC_CLKF, O_ORC_CLKF, O_ANDP_CLKG, O_ORP_CLKG, O_FF_CLKG, O_ANDC_CLKG, O_ORC_CLKG, O_ANDP_CLKH, O_ORP_CLKH, O_FF_CLKH, O_ANDC_CLKH, O_ORC_CLKH, O_ANDP_HCLKA, O_ORP_HCLKA, O_FF_HCLKA, O_ANDC_HCLKA, and O_ORC_HCLKA) of four (4) shift registers with 10,728 bits total, and half of the output pins (OUTX0, OUTX1, OUTX2, OUTX3, OUTX4, OUTX5, OUTX6 and OUTX7) of the embedded RAM configured as 16K×16.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is measured on single-ended inputs EN8, DA, IO_I1, IO_I2, IO_I3, IO_I4, IO_I5 and IO_I6, and also on differential inputs DIO_I1P, DIO_I2P, DIO_I3P, DIO_I4P, DIO_I5P, DIO_I6P and DIO_I7P. The differential inputs are configured as LVPECL instead of LVDS; because LVPECL using 3.3 VDC, is worse than LVDS which uses 2.5 VDC. During the measurement on the differential inputs, the N (negative) side of the differential pair is biased at 1.8 V. The output-drive voltage (VOL/VOH) is measured on QA0 and YQ0. The propagation delay is measured on the output (O_BS) of the buffer string; the definition is the time delay from the triggering edge at the CLOCK input to the switching edge at the output O_BS. Both the delays of low-to-high and high-to-low output transitions are measured; the reported delay is the average of these two measurements. The transition characteristics, measured on the output O_BS, are shown as oscilloscope captures.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key logic functions (O_BS, O_ANDP_CLKF, O_ORP_CLKF, O_FF_CLKF, O_ANDC_CLKF, O_ORC_CLKF, O_ANDP_CLKG, O_ORP_CLKG, O_FF_CLKG, O_ANDC_CLKG, O_ORC_CLKG, O_ANDP_CLKH, O_ORP_CLKH, O_FF_CLKH, O_ANDC_CLKH, O_ORC_CLKH, O_ANDP_HCLKA, O_ORP_HCLKA, O_FF_HCLKA, O_ANDC_HCLKA, and O_ORC_HCLKA), and outputs of embedded RAM (OUTX0, OUTX1, OUTX2, OUTX3, OUTX4, OUTX5, OUTX6 and OUTX7)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (EN8/YQ0, DA/QA0, IO_I1/IO_O1, IO_I2/IO_O2, IO_I3/IO_O3, IO_I4/IO_O4, IO_I5/IO_O5, IO_I6/IO_O6), and differential inputs (DIO_I1P/DIO_O1, DIO_I2P/DIO_O2, DIO_I3P/DIO_O3, DIO_I4P/DIO_O4, DIO_I5P/DIO_O5, DIO_I6P/DIO_O6, DIO_I7P/DIO_O7)
4. Output Drive (VOL/VOH)	Output buffer (EN8/YQ0, DA/QA0)
5. Propagation Delay	String of buffers (CLOCK to O_BS)
6. Transition Characteristic	String of buffers output (O_BS)

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests. The as-irradiated DUT is functionally tested on the output (O_FF_HCLKA) of the largest shift register.

B. Power Supply Current (ICCA and ICCI)

Figure 2 through Figure 6 plot the influx standby ICCA and ICCI versus total dose for each DUT. The post-annealing ICC for four different bit patterns, all '0', all '1', checkerboard and inverted-checkerboard, in the RAM are basically the same.

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-6 of *the RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs* datasheet:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 500 mA; the PIPL of ICCI equals to 35 + 10 + 3.7 × 2 = 52.4 (mA). Note that there are 2 pairs of differential LVPECL inputs in each DUT.

Table 3 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-Irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
5105	300 krad	1	272.46	9	41	311.93	31.44
5106	300 krad	1	290.56	11	42	342.63	48.90
5107	300 krad	1	185.58	7	43	241.64	54.01
5112	200 krad	1	24.68	2	43	108.58	29.90
5113	200 krad	0	29.47	1	39	125.36	37.06

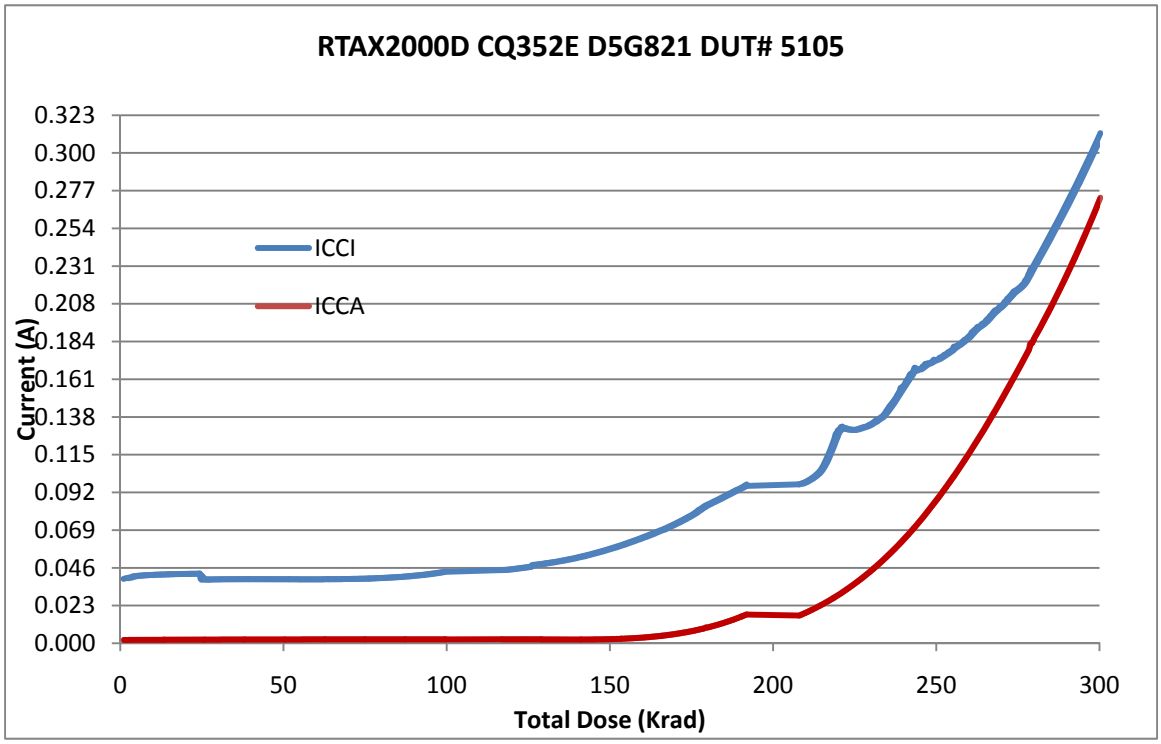

Figure 2 DUT 5105 Influx ICCA and ICCI

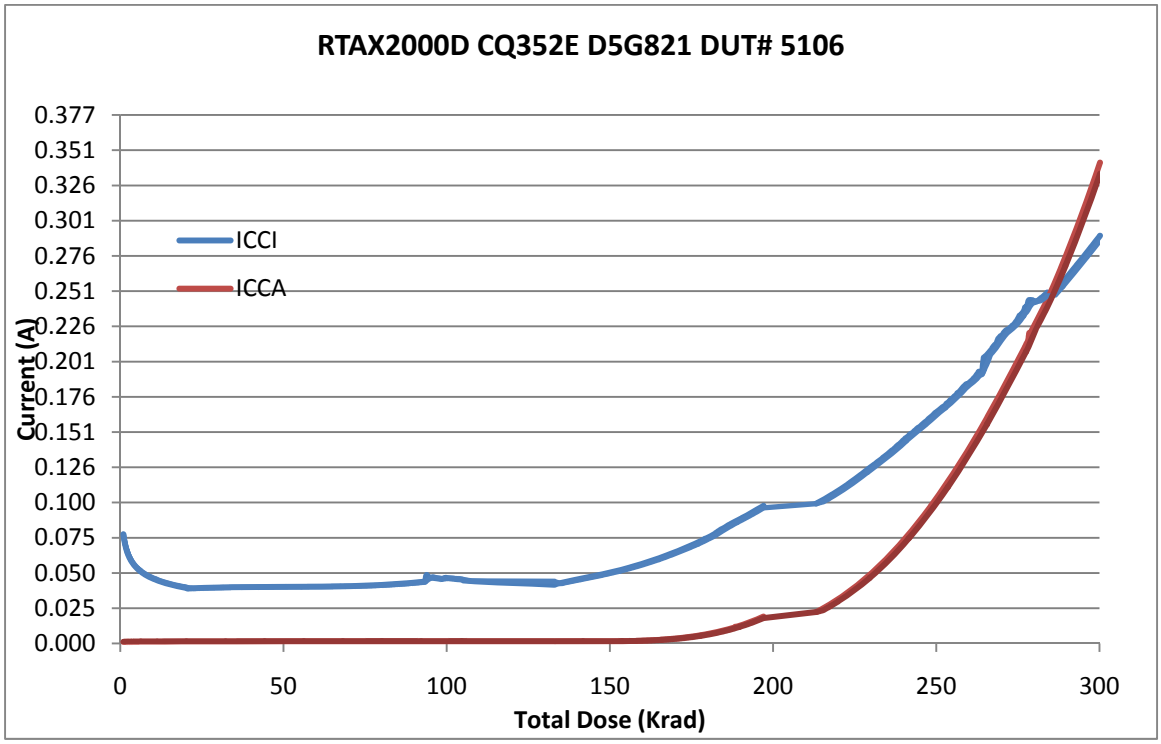

Figure 3 DUT 5106 Influx ICCA and ICCI

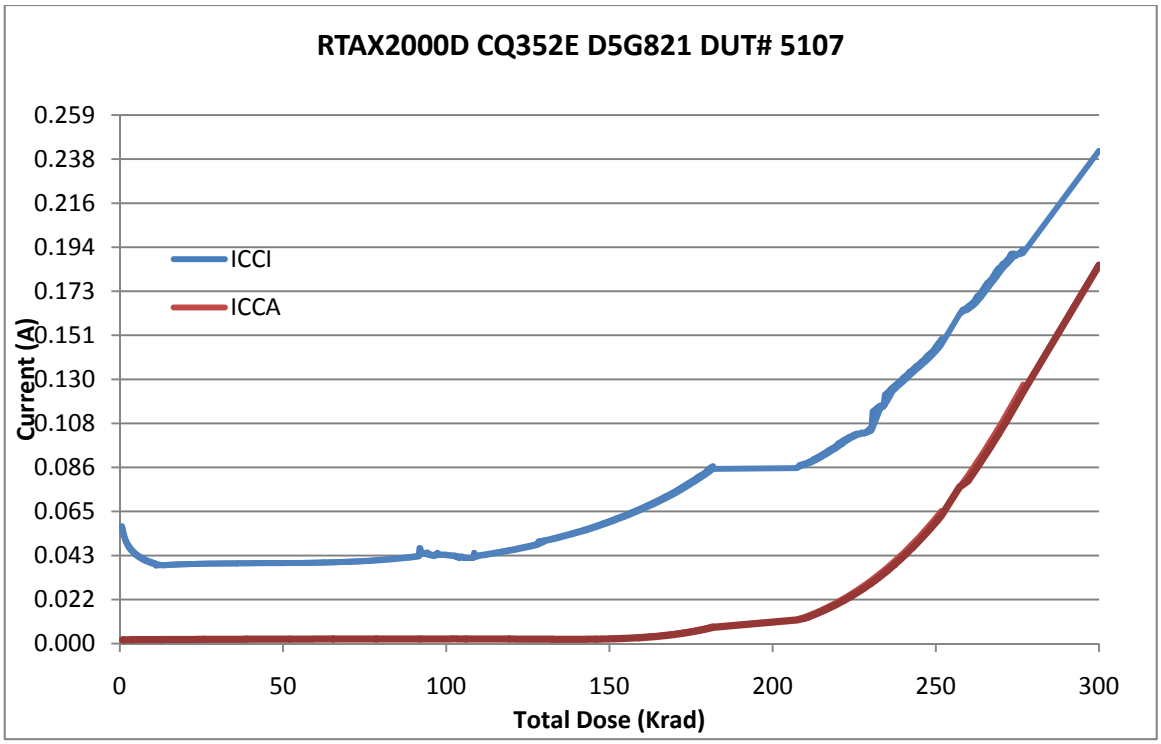

Figure 4 DUT 5107 Influx ICCA and ICCI

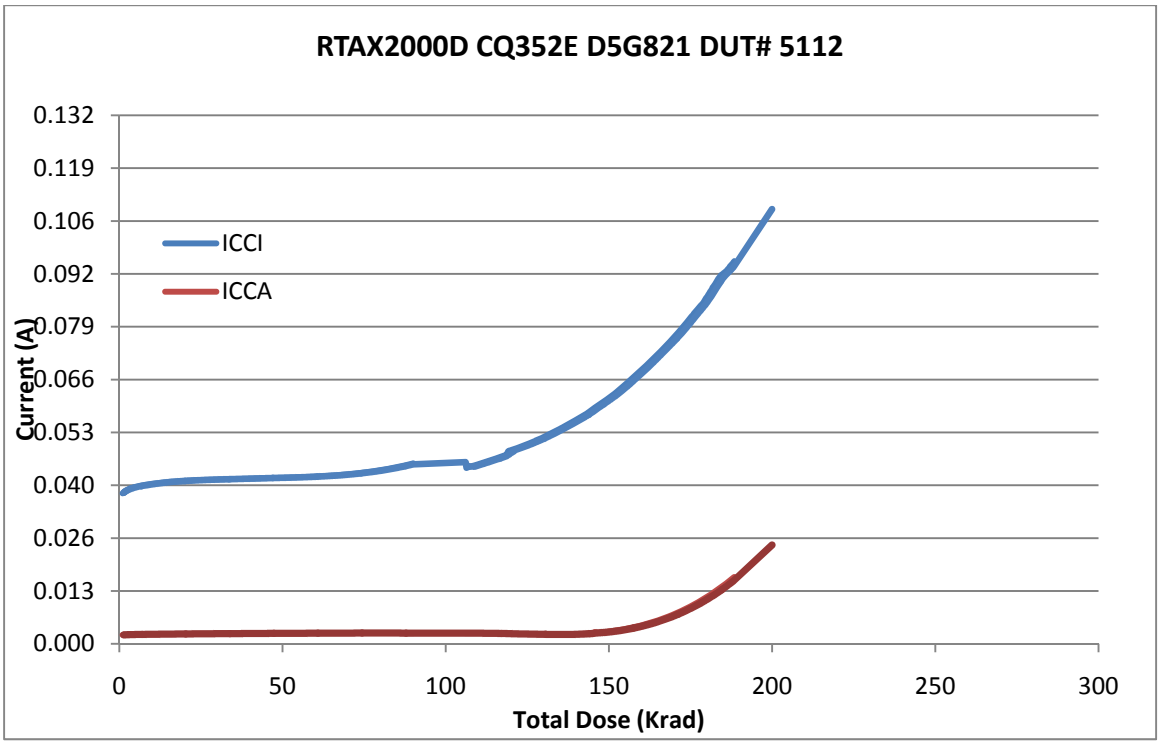

Figure 5 DUT 5112 Influx ICCA and ICCI

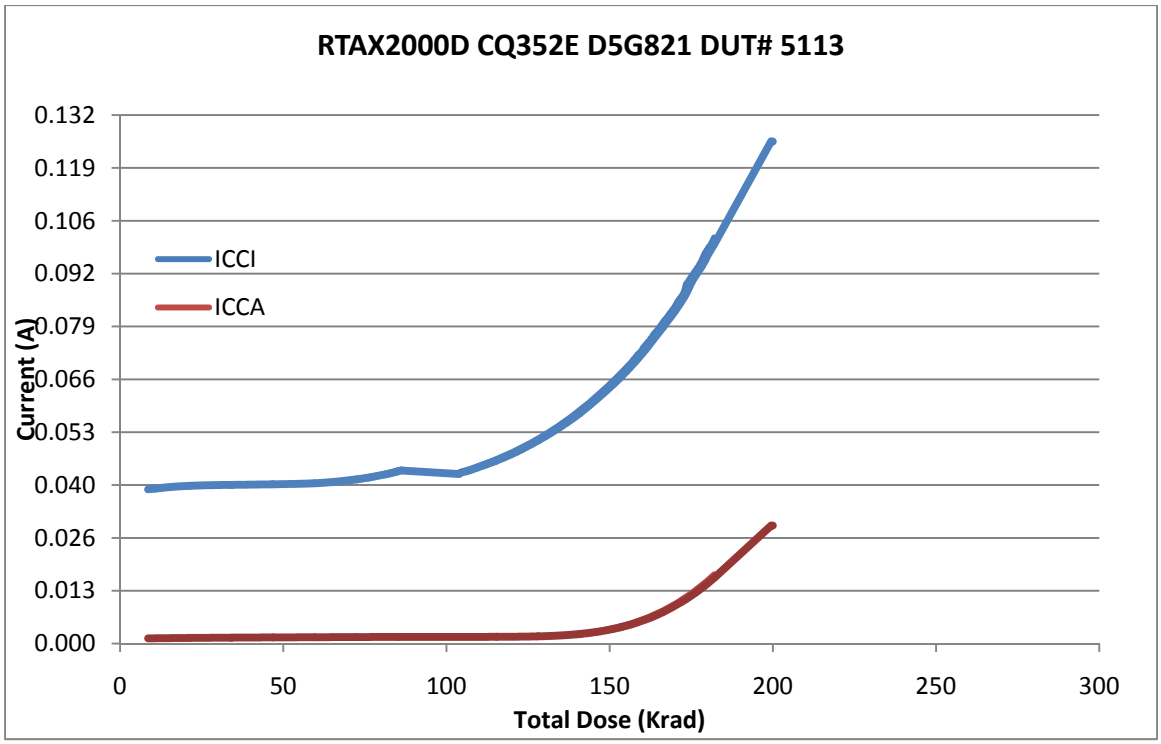

Figure 6 DUT 5113 Influx ICCA and ICCI

C. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH values for various pins are listed in Tables 4 and 5. The post-annealing data are within the specification limits.

Table 4 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Currents and Pins

Sourcing Current	Pin\DUT	5105 (300 krad)		5106 (300 krad)		5107 (300 krad)		5112 (200 krad)		5113 (200 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
24 mA	IO_Outs_EAQ_14	187	181	190	192	189	190	188	180	188	180
	ALU_test_mon_QBI	190	173	191	195	191	164	189	183	189	172
	Shiftout_0	204	197	211	203	206	197	204	198	204	199
16 mA	Array_out_EAQ_1	145	141	144	140	146	141	143	140	146	141
	IO_Outs_EAQ_19	163	160	166	162	164	158	162	157	163	158
	Math_acc_18x18_ok	150	157	154	159	154	160	152	154	153	154
12 mA	Math_acc_9x9_SIMD_ok	147	162	146	158	147	159	145	151	147	151
	IO_Outs_EAQ_0	150	147	151	145	151	144	150	145	150	145
	Ram_test_mon_QBI	151	140	152	144	153	143	151	149	152	145
8 mA	IO_Outs_EAQ_17	174	168	175	165	177	165	174	166	175	167
	Shiftout_2	181	171	183	174	183	172	181	173	182	174
	rcell_outz_HSB_0	181	171	182	174	182	172	180	172	181	173

Table 5 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Currents and Pins

Sourcing Current	Pin\DUT	5105 (300 krad)		5106 (300 krad)		5107 (300 krad)		5112 (200 krad)		5113 (200 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
24 mA	IO_Outs_EAQ_14	2721	2722	2718	2706	2719	2706	2722	2712	2720	2720
	ALU_test_mon_QBI	2718	2719	2717	2697	2718	2705	2720	2717	2718	2739
	Shiftout_0	2700	2694	2695	2690	2700	2695	2703	2698	2701	2697
16 mA	Array_out_EAQ_1	2771	2765	2772	2766	2771	2764	2773	2769	2771	2766
	IO_Outs_EAQ_19	2754	2753	2753	2747	2754	2750	2756	2754	2756	2753
	Math_acc_18x18_ok	2767	2766	2765	2763	2764	2763	2765	2765	2765	2764
12 mA	Math_acc_9x9_SIMD_ok	2763	2759	2764	2760	2762	2758	2765	2765	2763	2759
	IO_Outs_EAQ_0	2760	2757	2759	2754	2758	2754	2761	2757	2760	2755
	Ram_test_mon_QBI	2758	2754	2756	2749	2756	2752	2758	2758	2757	2746
8 mA	IO_Outs_EAQ_17	2718	2715	2716	2712	2715	2710	2720	2716	2717	2713
	Shiftout_2	2712	2706	2712	2705	2711	2707	2713	2710	2713	2708
	rcell_outz_HSB_0	2712	2709	2716	2710	2715	2711	2715	2714	2716	2714

D. Propagation Delay

The propagation delay was measured in-situ, post-irradiation, and post-annealing. The results are plotted in Figure 8, and listed in Table 6. As shown in Figure 8, the propagation delay moves with the total dose, but the change is small throughout the irradiation. Referring to influx static current plots (Figure 2 through Figure 6), a device probably heats up as the dose increases. The rising temperature could be the root cause of the increasing trend at high doses. The post-annealing data, on the other hand, show decreased delay in every case.

The radiation delta in every case is well within the 10% degradation criterion. The user can take the worst case for the design margin consideration.

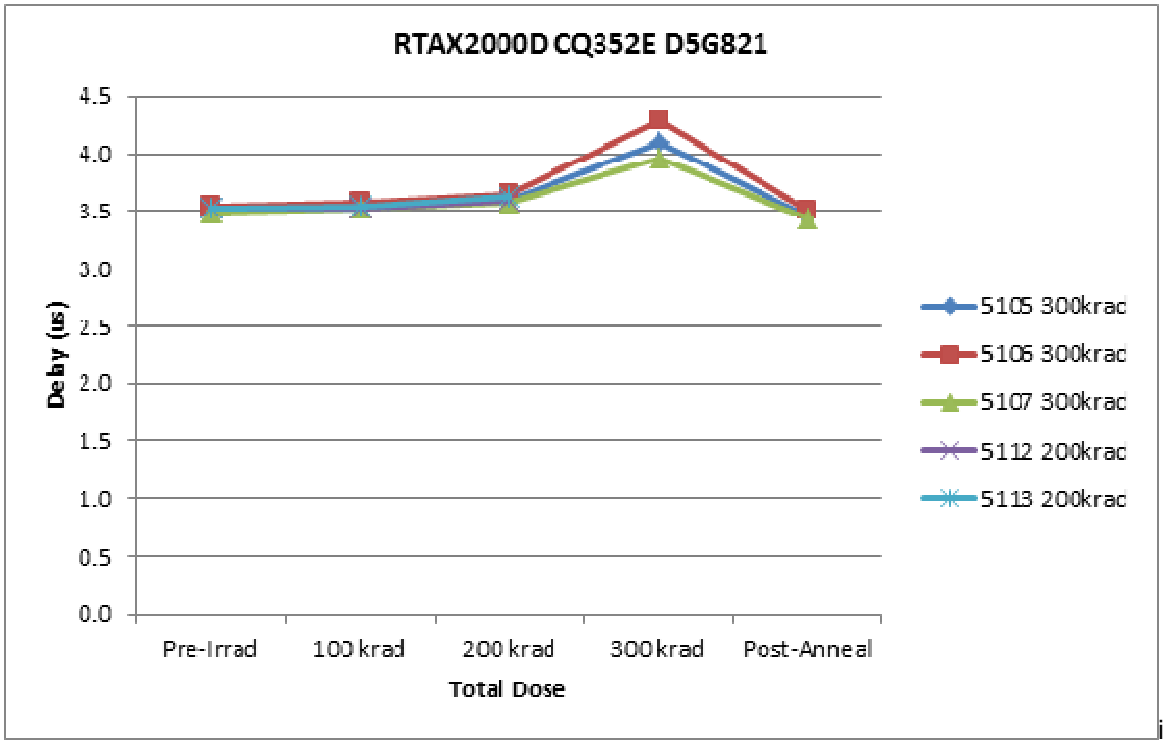

Figure 8 In-Situ Propagation Delay versus Total Dose

Table 6 Radiation-Induced Propagation Delay Degradations

Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	5105	300 krad	3.51	3.53	3.59	4.09	3.45
	5106	300 krad	3.54	3.57	3.64	4.28	3.5
	5107	300 krad	3.49	3.52	3.58	3.95	3.44
	5112	200 krad	3.52	3.53	3.59	-	3.44
	5113	200 krad	3.53	3.54	3.62	-	3.46
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	5105	300 krad	-	0.57 %	2.28 %	16.53 %	-1.7 %
	5106	300 krad	-	0.85 %	2.83 %	20.91 %	-1.12 %
	5107	300 krad	-	0.86 %	2.58 %	13.19 %	-1.43 %
	5112	200 krad	-	0.29 %	1.99 %	-	-2.27 %
	5113	200 krad	-	0.29 %	2.55 %	-	-1.98 %

E. Transition Characteristics

Figure 9a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

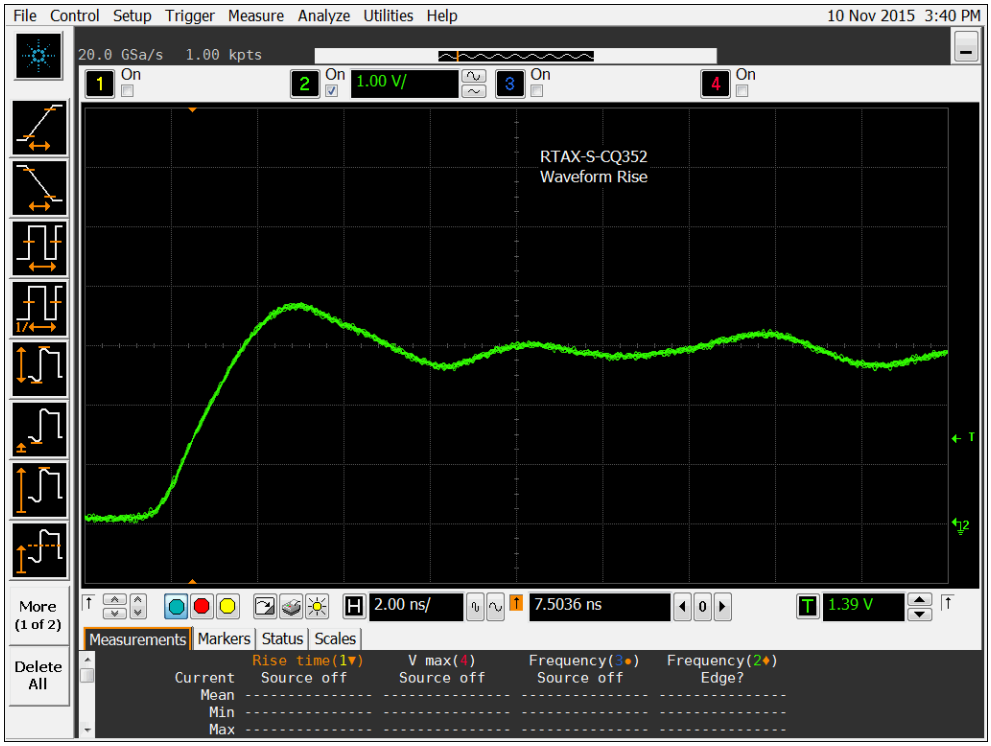

Figure 9a DUT 5105 Pre-Irradiation Rising Edge

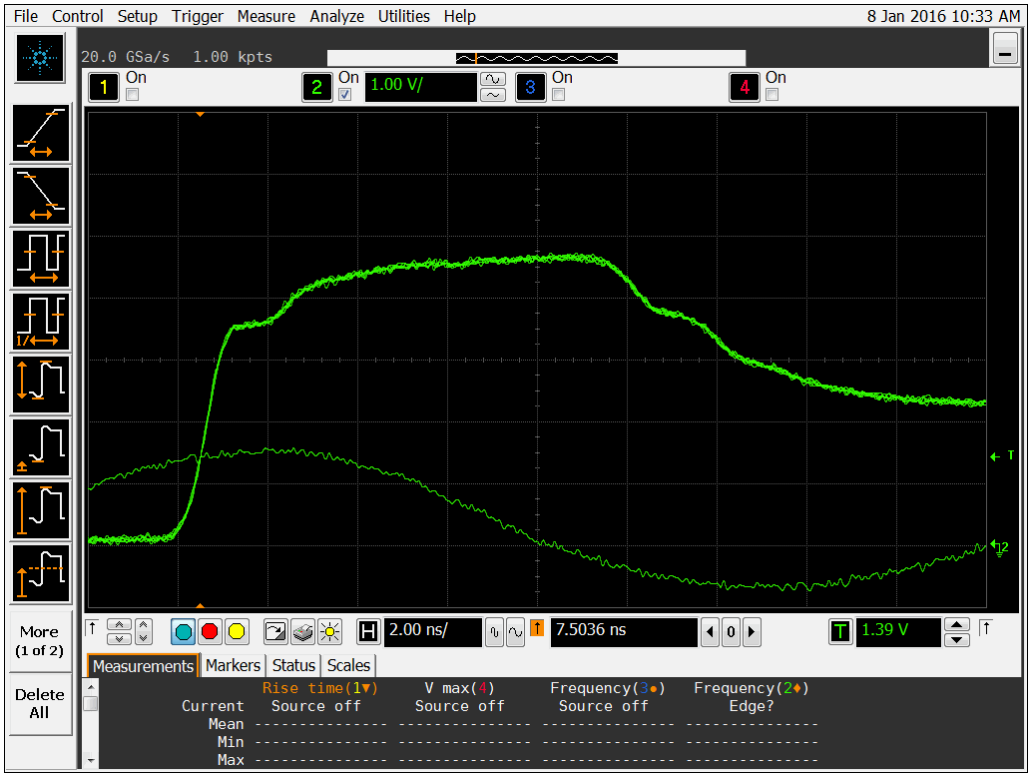

Figure 9b DUT 5105 Post-Annealing Rising Edge

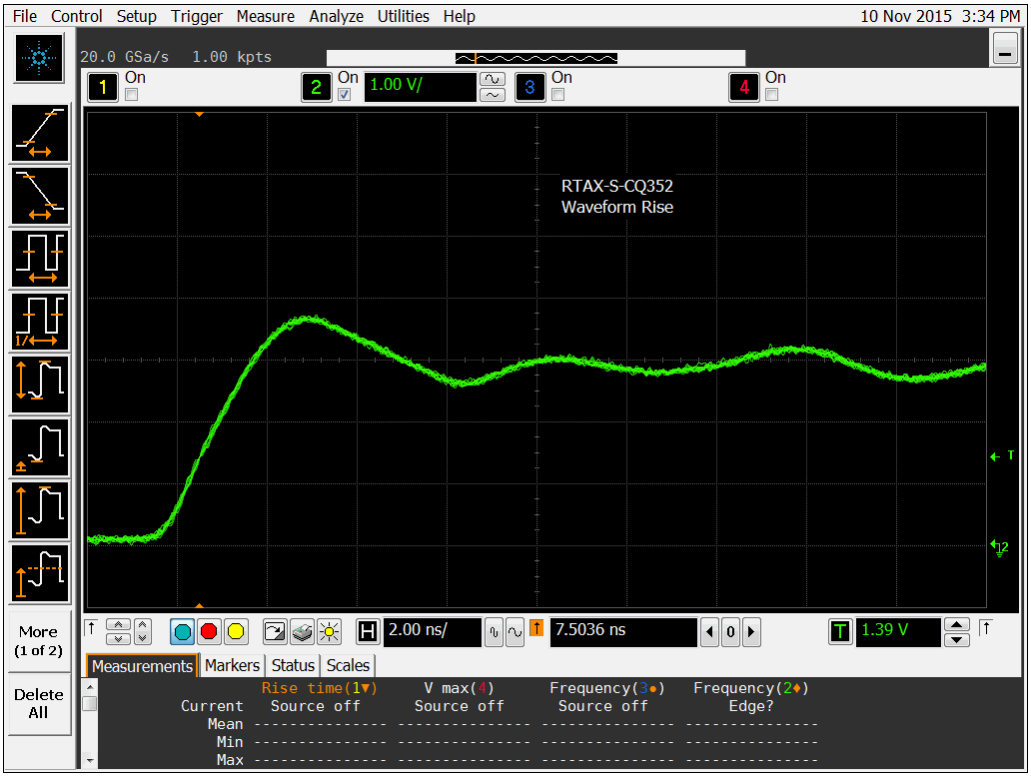

Figure 10a DUT 5106 Pre-Irradiation Rising Edge

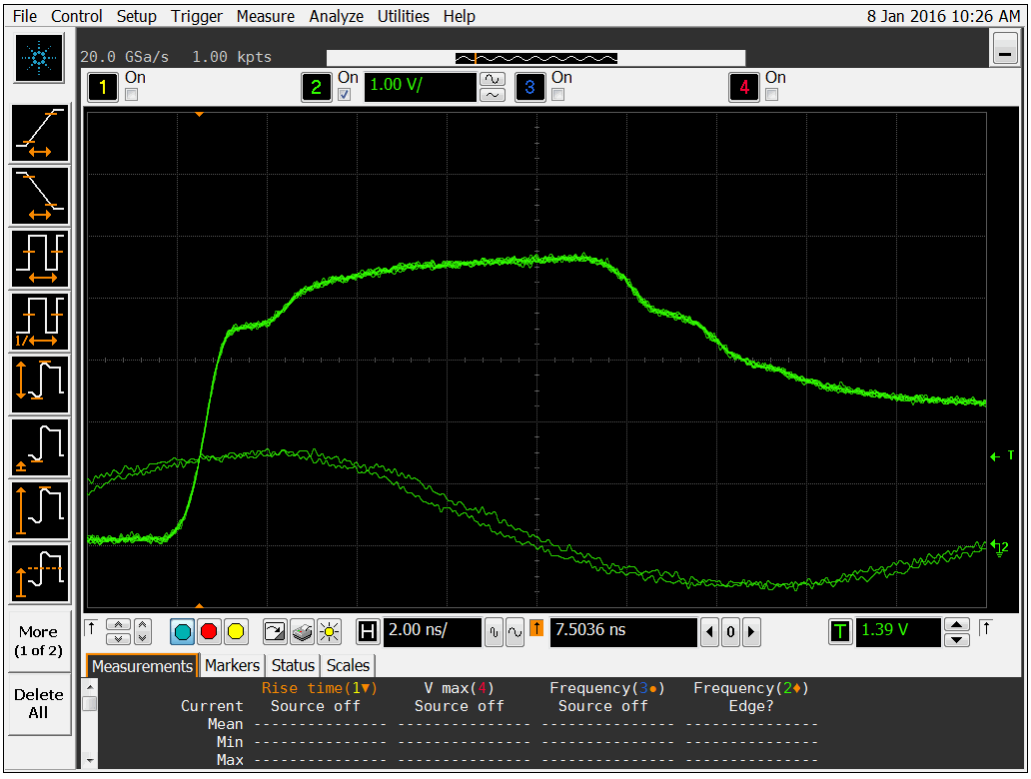

Figure 10b DUT 5106 Post-Annealing Rising Edge

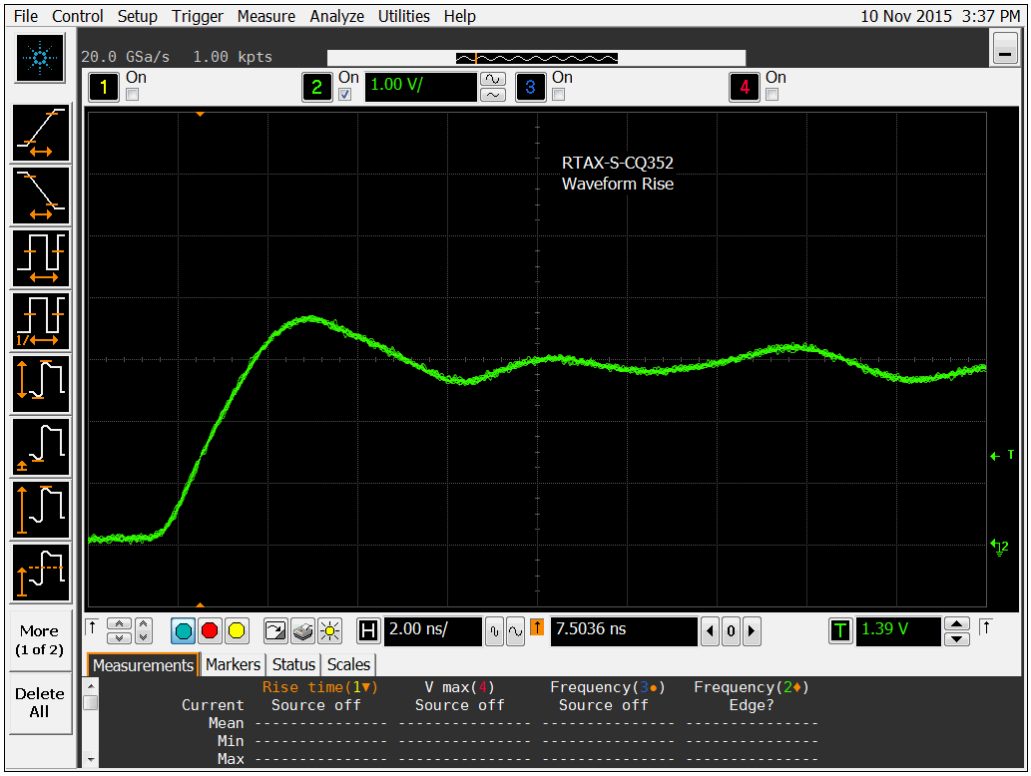

Figure 11a DUT 5107 Pre-Radiation Rising Edge

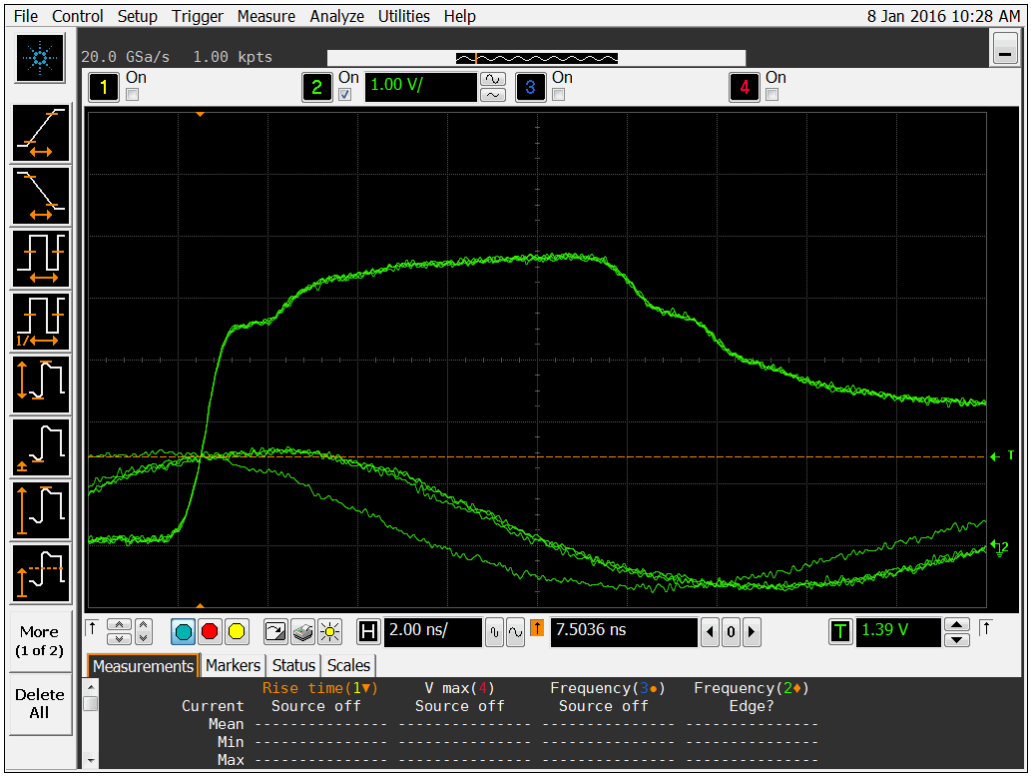

Figure 11b DUT 5107 Post-Annealing Rising edge

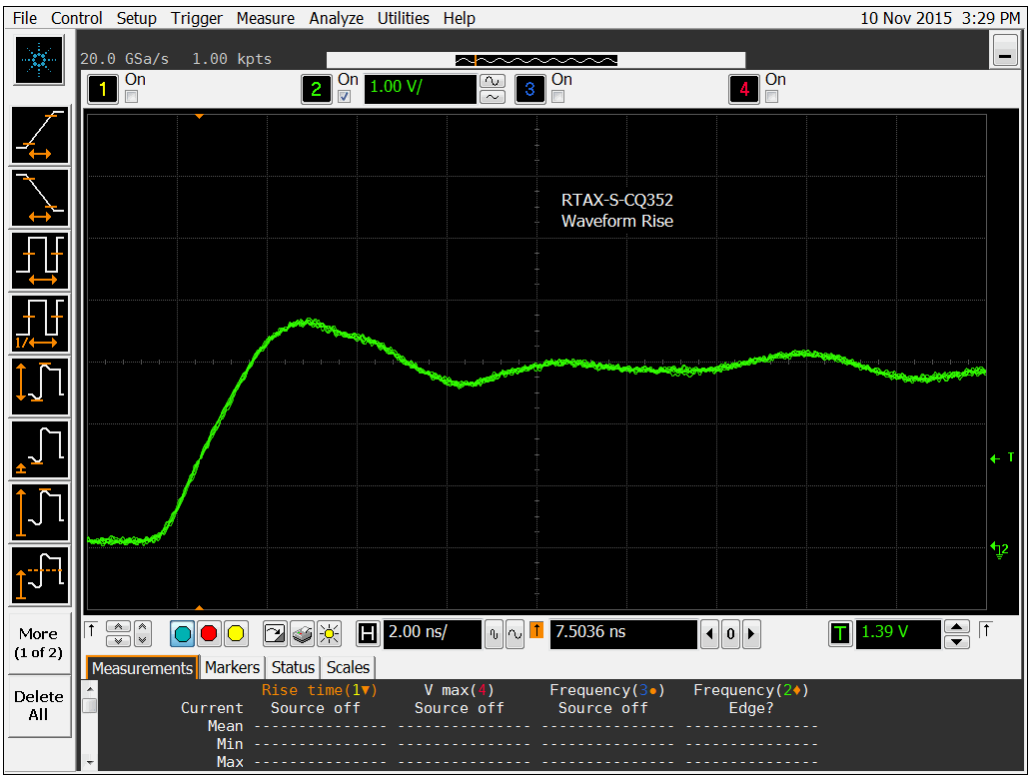

Figure 12a DUT 5112 Pre-Irradiation Rising Edge

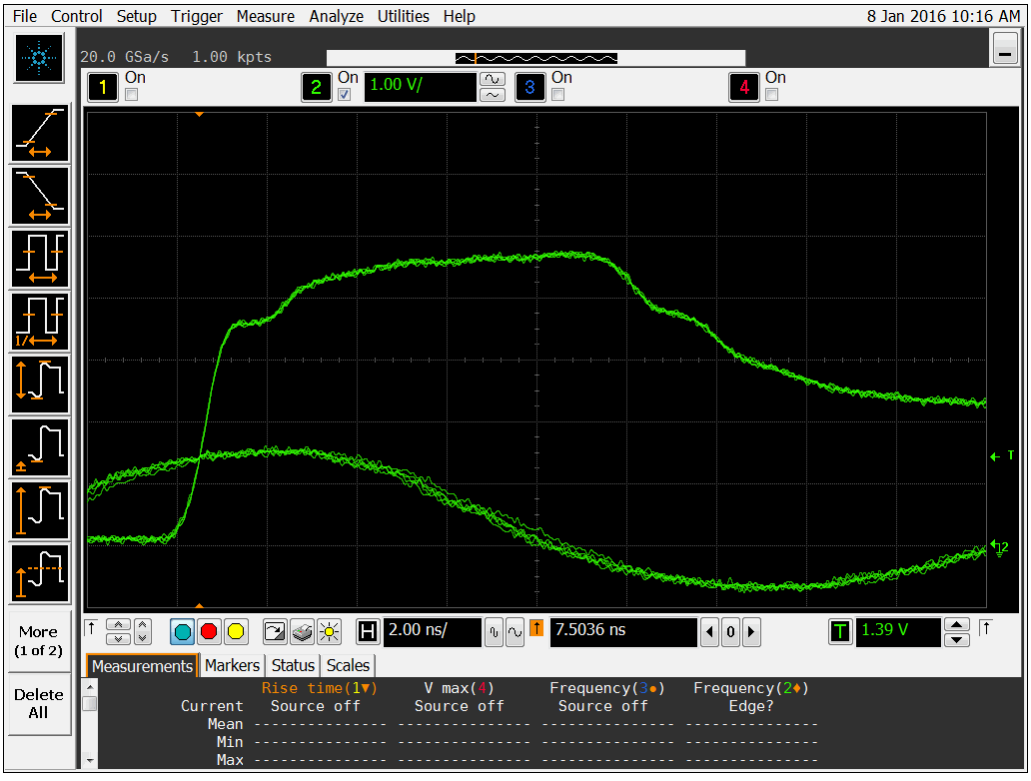

Figure 12b DUT 5112 Post-Annealing Rising Edge

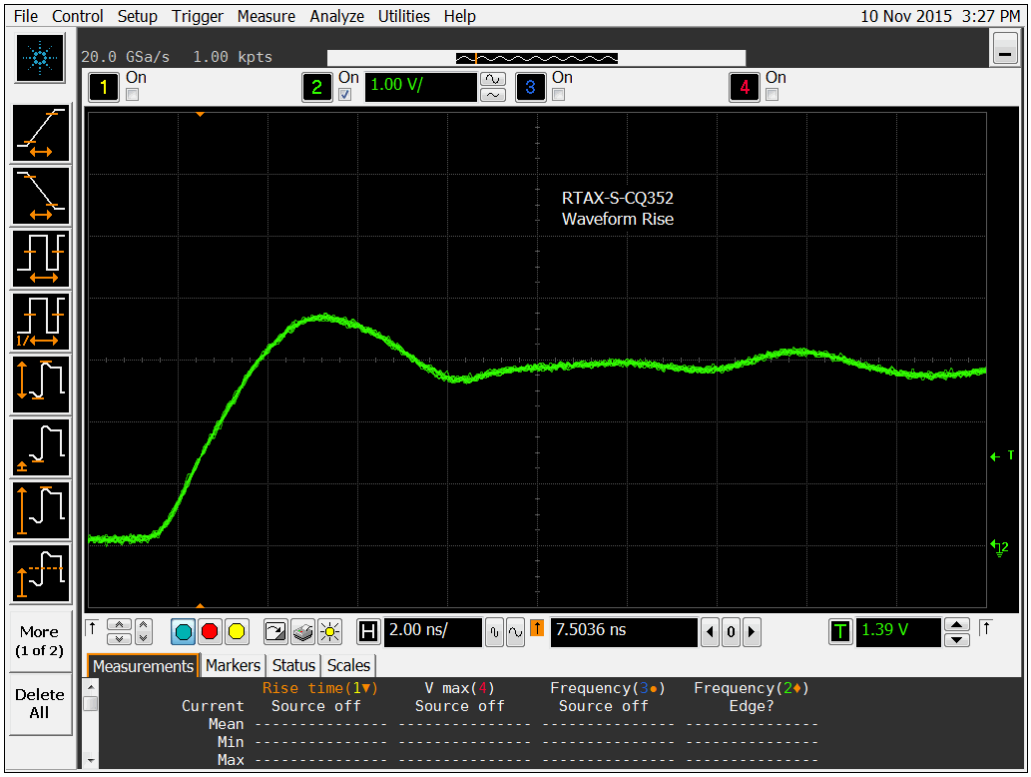

Figure 13a DUT 5113 Pre-Irradiation Rising Edge

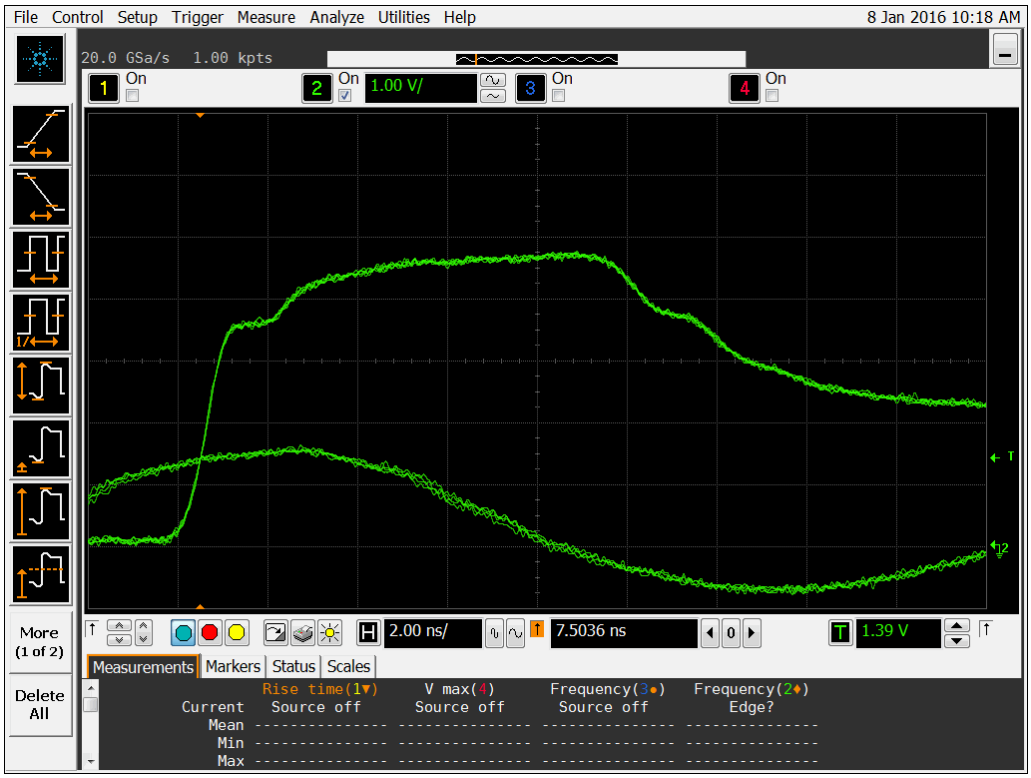

Figure 13b DUT 5113 Post-Annealing Rising Edge

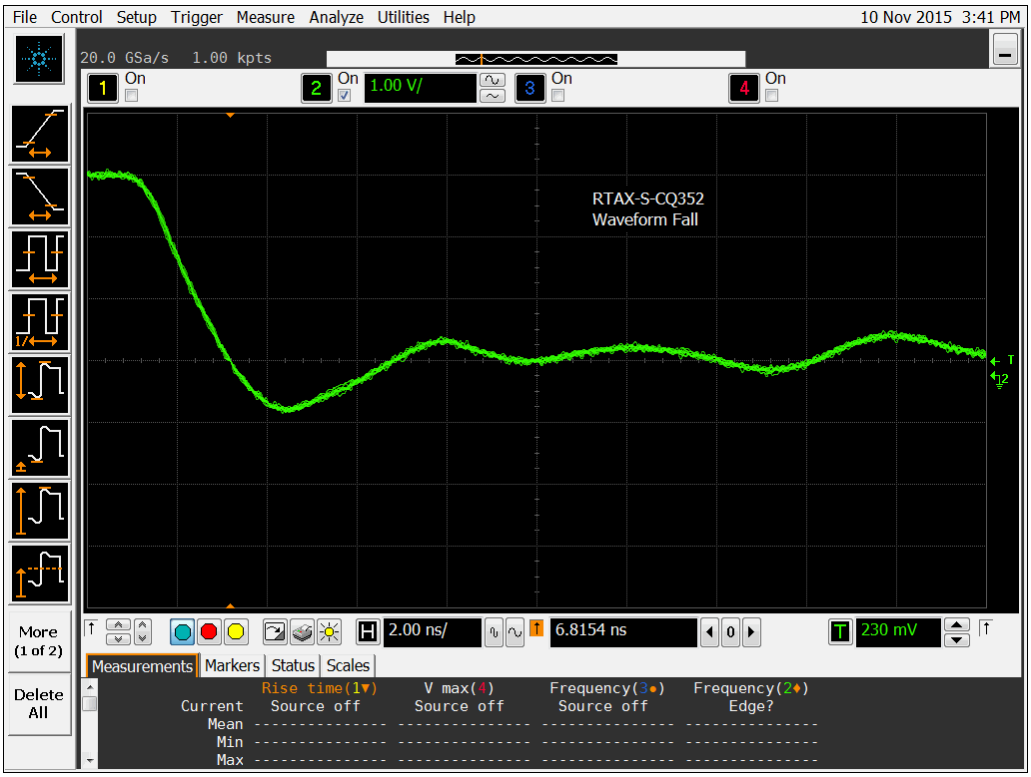

Figure 14a DUT 5105 Pre-Irradiation Falling Edge

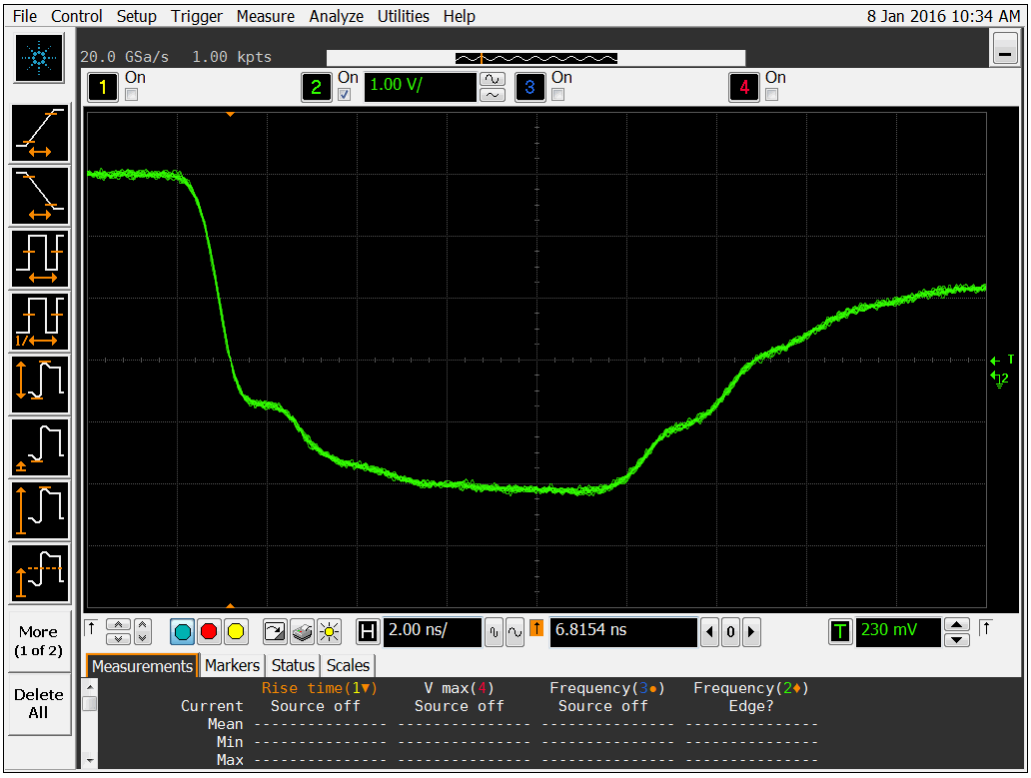

Figure 14b DUT 5105 Post-Annealing Falling Edge

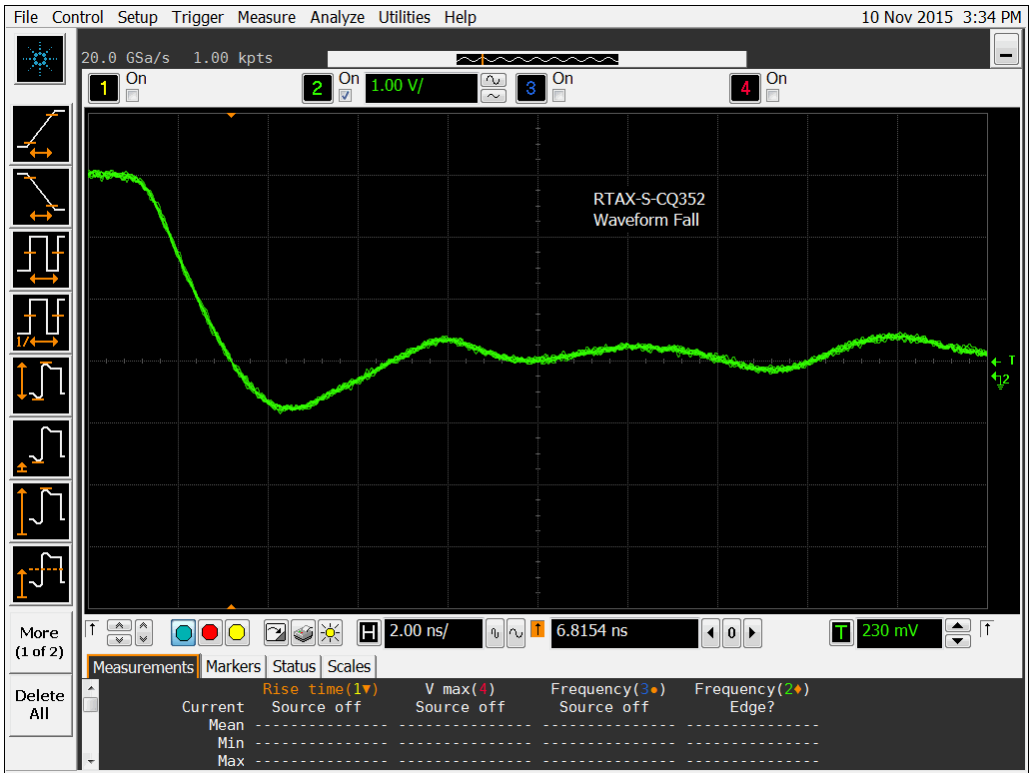

Figure 15a DUT 5106 Pre-Irradiation Falling Edge

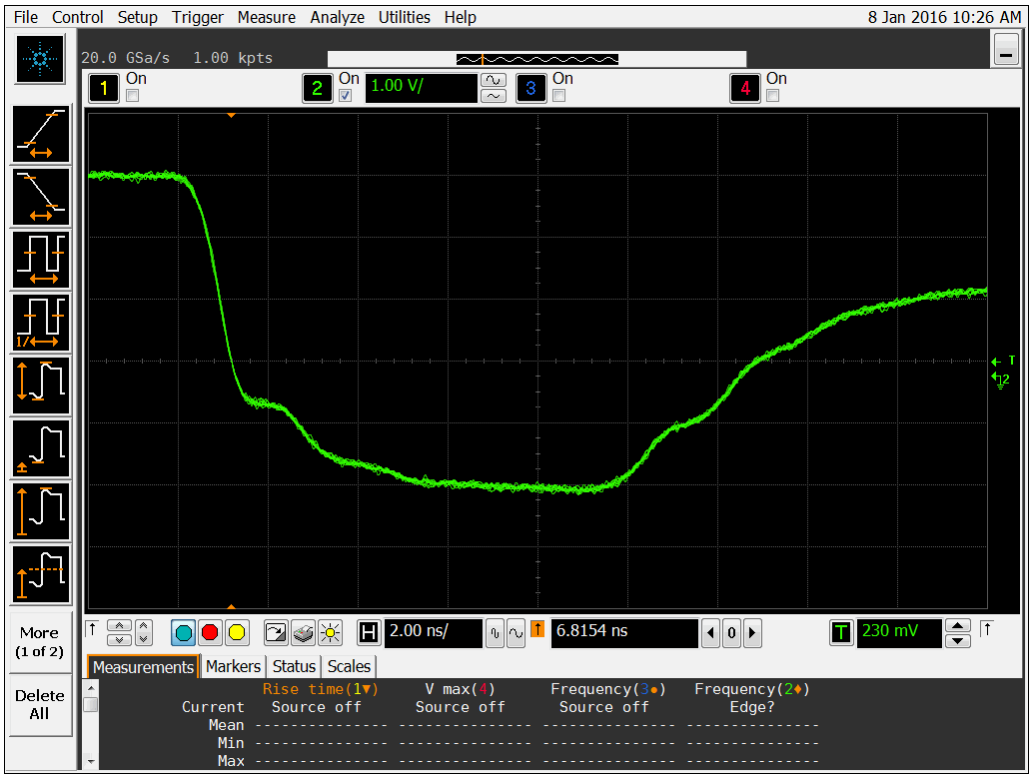

Figure 15b DUT 5106 Post-Annealing Falling Edge

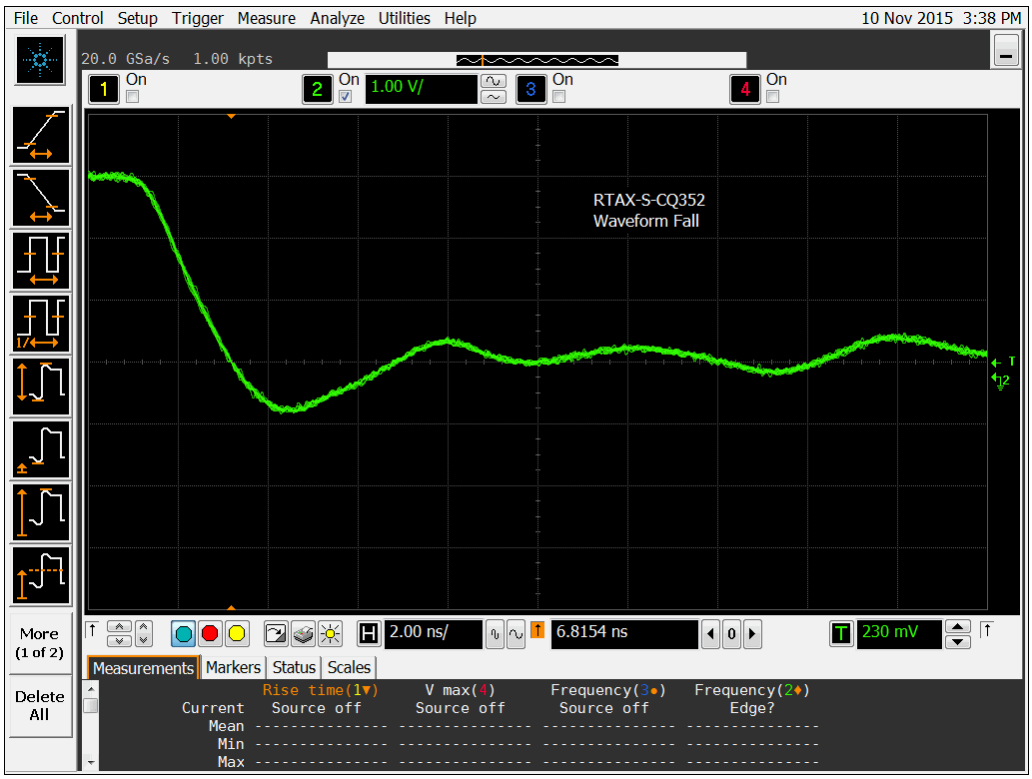

Figure 16a DUT 5107 Pre-Irradiation Falling Edge

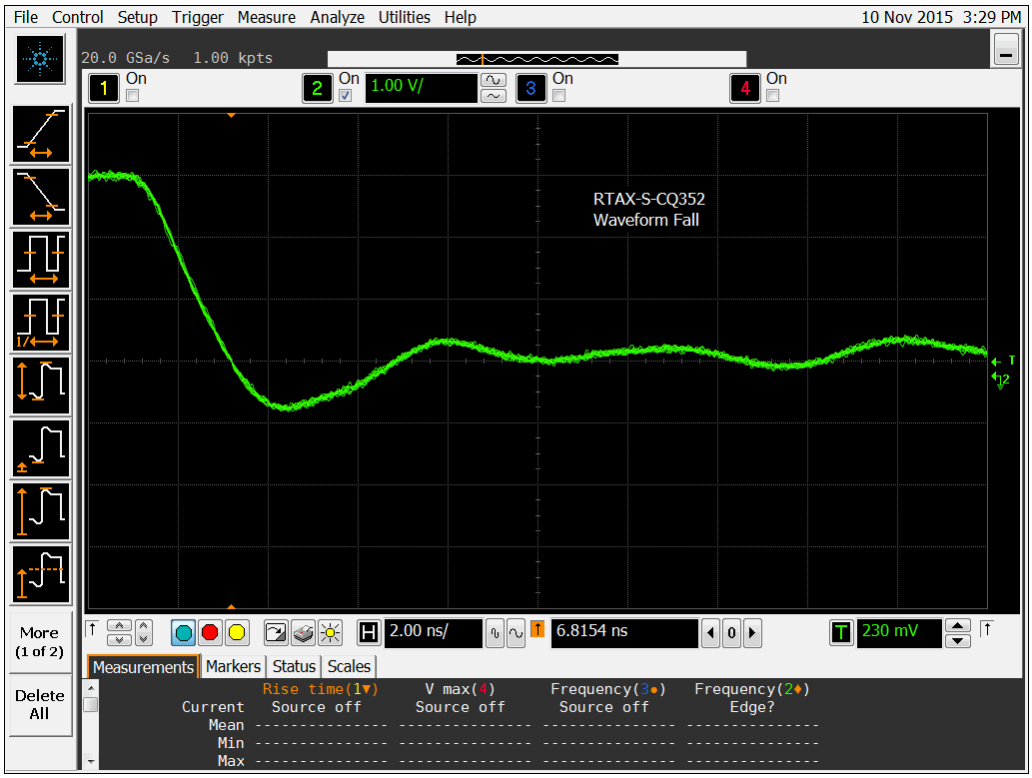

Figure 16b DUT 5107 Post-Annealing Falling Edge

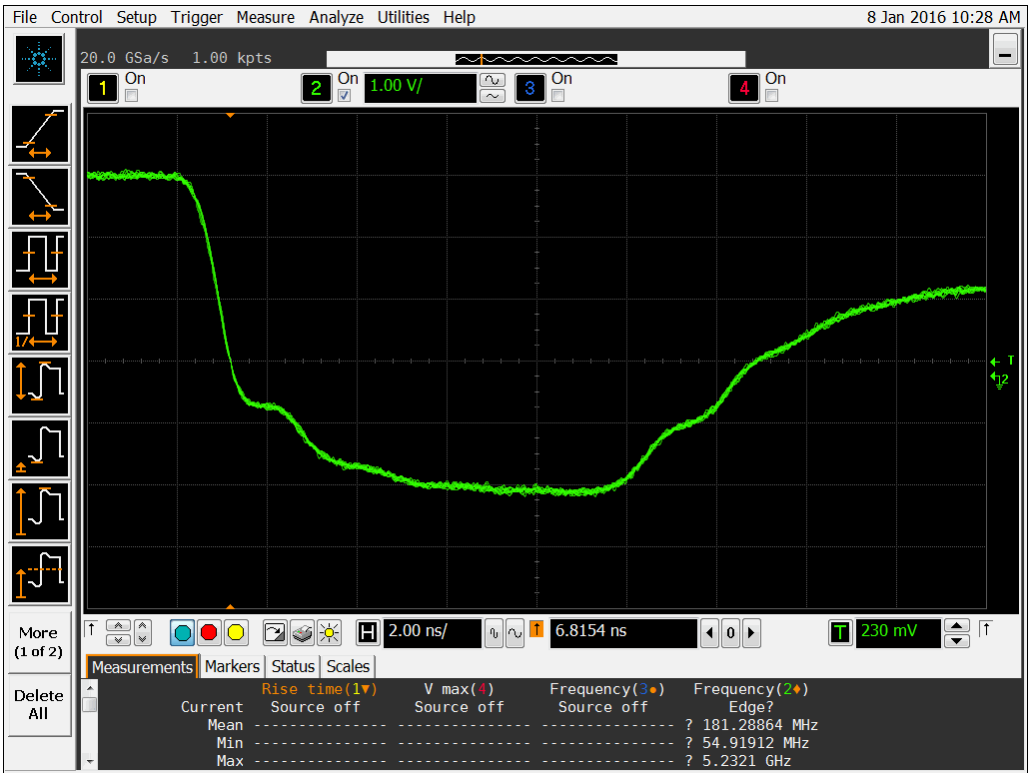

Figure 17a DUT 5112 Pre-Irradiation Falling Edge

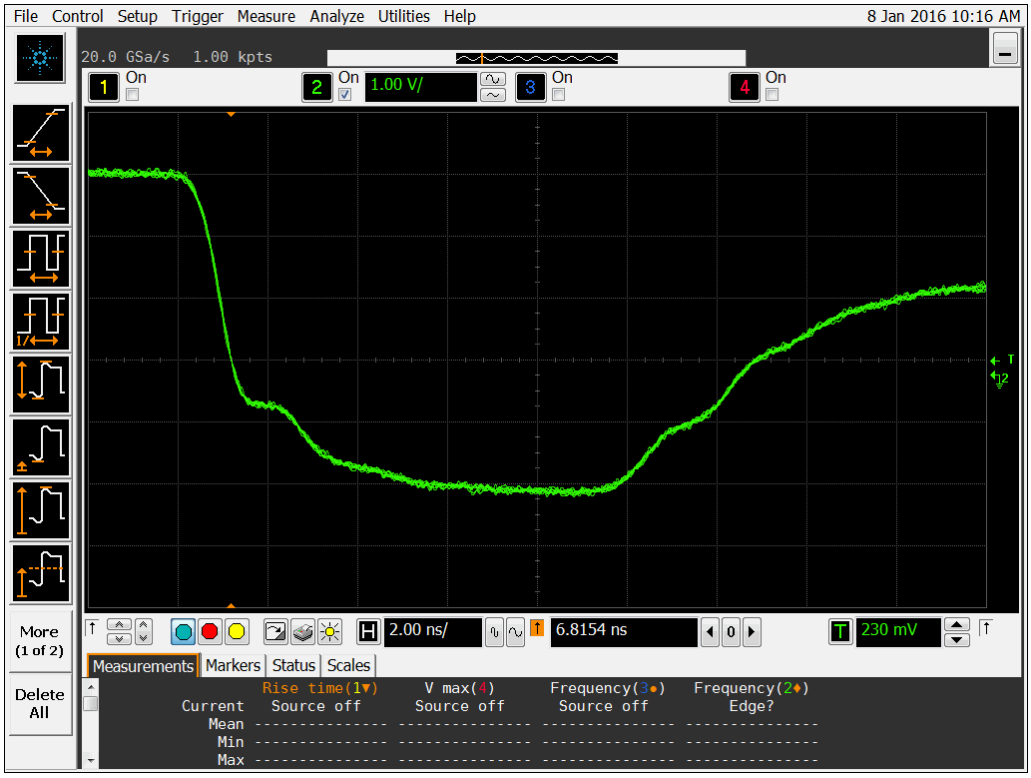

Figure 17b DUT 5112 Post-Annealing Falling Edge

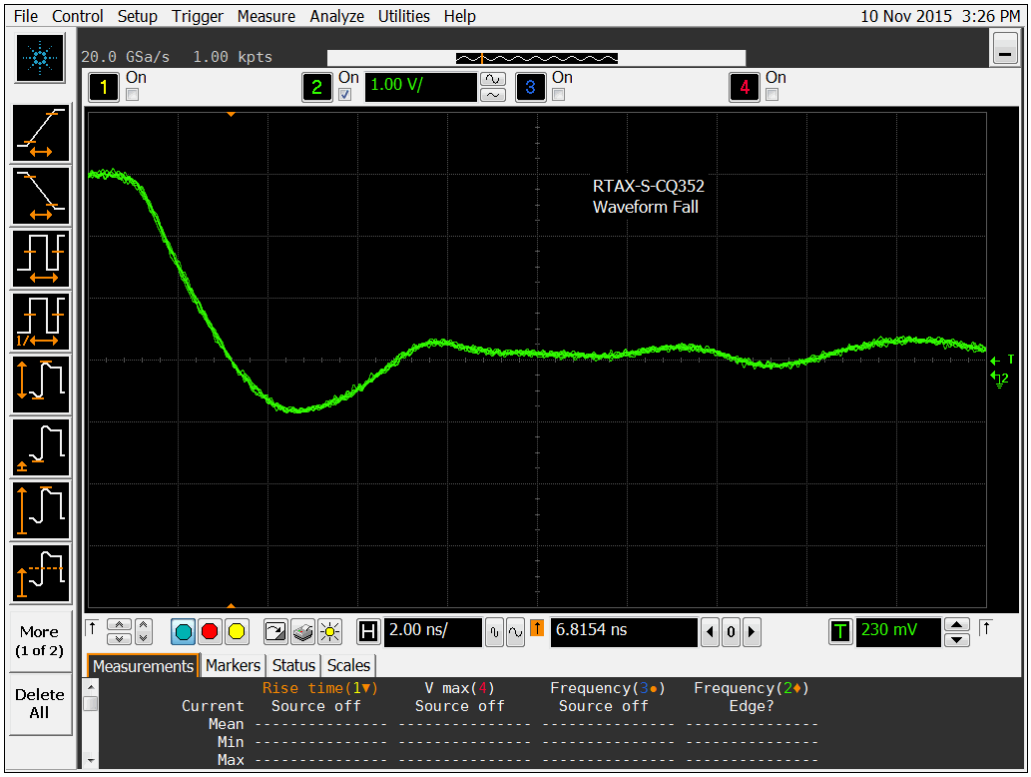

Figure 18a DUT 5113 Pre-Irradiation Falling Edge

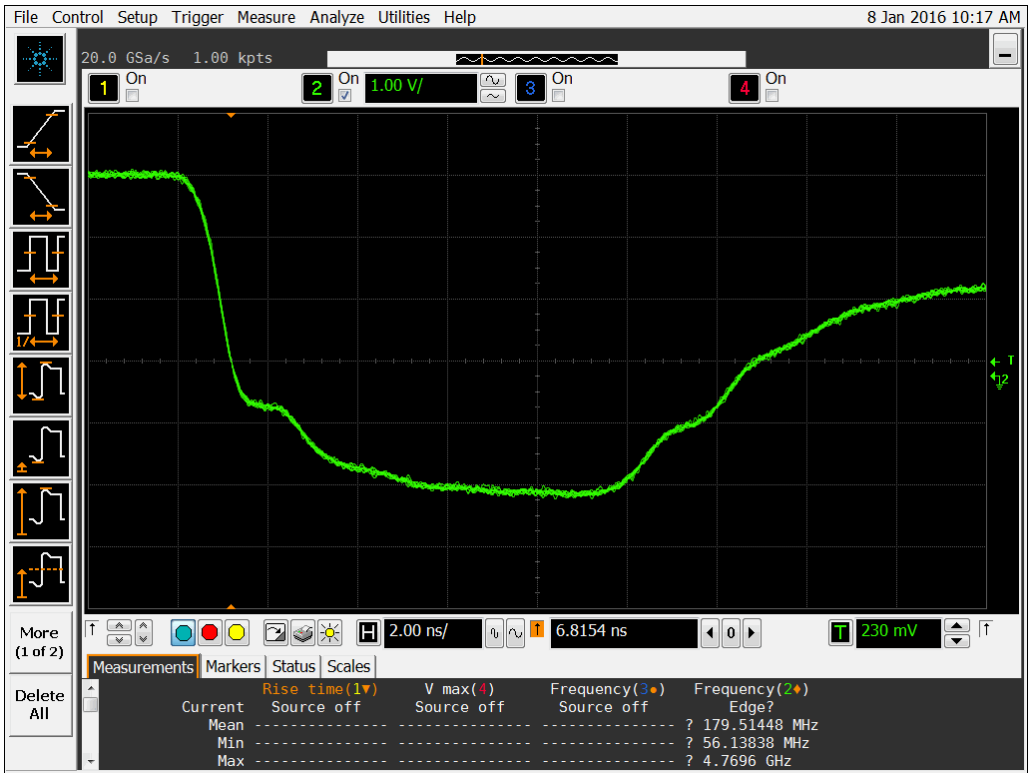

Figure 18b DUT 5113 Post-Annealing Falling Edge