AC439: RTG4 FPGAs Board Design and Layout Guidelines Application Note Addendum

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in May 2018. It was the first publication of this document.

2 Analysis of RTG4-DEV-KIT DDR3 Board Layout

This addendum to AC439: Board Design and Layout Guidelines for RTG4 FPGA Application Note, provides supplemental information, to emphasize that the DDR3 length matching guidelines published in revision 9 or later take precedence over the board layout used for the RTG4™ development kit. Initially, the RTG4 development kit was only available with Engineering Silicon (ES). After the initial release, the kit was later populated with standard (STD) speed grade and -1 speed grade RTG4 production devices. Part numbers, RTG4-DEV-KIT and RTG4-DEV-KIT-1 come with STD speed grade and -1 speed grade devices respectively.

The RTG4 Development Kit implements a 32-bit data and 4-bit ECC DDR3 interface for each of the two built-in RTG4 FDDR controllers and PHY blocks (FDDR East and West). The interface is physically organized as five data byte lanes.

The kit follows the fly by routing scheme as described in the DDR3 Layout Guidelines section of the application note. However, since this development kit was designed before publishing the application note, it does not conform to the updated length matching guidelines described in the application note. In the DDR3 specification, there is a +/- 750 ps limit on the skew between data strobe (DQS) and DDR3 clock (CK) at each DDR3 memory device during a write transaction (tDQSS).

When the length matching guidelines in the application note, AC439 revision 9 or later are followed, the RTG4 board layout will meet the tDQSS limit for both -1 and STD speed grade devices across the entire process, voltage and temperature (PVT) operating range supported by RTG4 production devices. This is accomplished by factoring in the worst-case output skew between DQS and CK at the RTG4 pins. Specifically, when using the built-RTG4 FDDR controller plus PHY, the DQS leads CK by 370 ps maximum for a -1 speed grade device and DQS Leads CK by 447 ps maximum for a STD speed grade device, in worst-case conditions.

Based on the analysis shown in the following Table 1 (see page 2), the RTG4-DEV-KIT-1 meets tDQSS limits at each memory device, at worst-case operating conditions for the RTG4 FDDR. However, as shown in the Table 2 (see page 2), the RTG4-DEV-KIT layout, populated with STD speed grade RTG4 devices, does not meet tDQSS for the fourth and fifth memory devices in the fly-by topology, at worst-case operating conditions for the RTG4 FDDR. In general, the RTG4-DEV-KIT is used at typical conditions, such as room temperature in a lab environment. Therefore, this worst-case analysis is not applicable to the RTG4-DEV-KIT used in typical conditions. The analysis serves as an example of why it is important to follow the DDR3 length matching guidelines listed in AC439, so that a user board design meets tDQSS for a flight application.

To further elaborate on this example, and demonstrate how to manually compensate for a RTG4 board layout which cannot meet the AC439 DDR3 length matching guidelines, the RTG4-DEV-KIT with STD speed grade devices can still meet tDQSS at each memory device, at worst-case conditions, because the built-in RTG4 FDDR controller plus PHY has the ability to statically delay the DQS signal per data byte lane. This static shift can be used to reduce the skew between DQS and CK at a memory device which has a tDQSS > 750 ps. See the DRAM Training section, in UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide for more information about using the static delay controls (in register REG_PHY_WR_DQS_SLAVE_RATIO) for DQS during a write transaction. This delay value can be used with Libero® SoC when instantiating an FDDR controller with automatic initialization by modifying the auto-generated CoreABC FDDR initialization code. A similar process can be applied to a user board layout which does not meet tDQSS at each memory device.

Table 1 • Evaluation of RTG4-DEV-KIT-1 tDQSS Calculation For -1 Parts and FDDR1 Interface

Path Analyzed	Clock Length (mils)	Clock Propagation Delay (ps)	Data Length (mils)	Data Propagation Delay (ps)	Difference between CLK-DQS due to Routing (mils)	tDQSS at every memory, after board skew+FPGA DQS-CLK skew (ps)
FPGA-1st Memory	2578	412.48	2196	351.36	61.12	431.12
FPGA-2nd Memory	3107	497.12	1936	309.76	187.36	557.36
FPGA-3rd Memory	3634	581.44	2231	356.96	224.48	594.48
FPGA-4th Memory	4163	666.08	2084	333.44	332.64	702.64
FPGA-5th Memory	4749	759.84	2848	455.68	304.16	674.16

Note: In worst case conditions, RTG4 FDDR DDR3 DQS-CLK skew for -1 devices is 370 ps maximum and 242 ps minimum.

Table 2 • Evaluation of RTG4-DEV-KIT tDQSS Calculation for STD Parts and FDDR1 Interface

Path Analyzed	Clock Length (mils)	Clock Propagation Delay (ps)	Data Length (mils)	Data Propagation Delay (ps)	Difference between CLK-DQS due to Routing (mils)	tDQSS at every memory, after board skew+FPGA DQS-CLK skew (ps)
FPGA-1st Memory	2578	412.48	2196	351.36	61.12	508.12
FPGA-2nd Memory	3107	497.12	1936	309.76	187.36	634.36
FPGA-3rd Memory	3634	581.44	2231	356.96	224.48	671.48
FPGA-4th Memory	4163	666.08	2084	333.44	332.64	779.64
FPGA-5th Memory	4749	759.84	2848	455.68	304.16	751.16

Note: In worst case conditions, RTG4 FDDR DDR3 DQS-CLK skew for STD devices is 447 ps maximum and 302 ps minimum.

Board propagation delay estimate of 160 ps/inch has been used in this analysis example for reference. The actual board propagation delay for a user board depends on the specific board being analyzed.

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