ZL30260-ZL30267 Configuration Sequence

Introduction

This document provides Microsemi's suggested configuration sequence for the ZL30260 through ZL30267 Any-to-Any Clock Multiplier and Frequency Synthesizer ICs. This document is not intended to replace the datasheet. Refer to the datasheet and the register map for more detailed information.

Configuration Sequence

The following sequence is suggested:

1. Wait for the device to finish auto-configuration from EEPROM or ROM (device is done when GLOBISR.BCDONE=1).
2. Enable the output divider logic for all outputs by setting the OCEN1 and OCEN2 register bits.

   On rev A devices this step should be done as soon as possible after power-on because the output drivers do not remain high-impedance unless these OCEN bits are set. If the device performs any auto-configuration from EEPROM then this step could be part of that auto-configuration. Otherwise it should be the first step in this configuration sequence.
3. If all or some outputs should be initially stopped (or stopped until they are configured) then configure participating outputs with OCxSTOP.SRC=0001 and the appropriate values for OCxSTOP.MODE and .NEGLSD and either MCR1.STOP=1 or set appropriate bits in STOPCR1 and STOPCR2.
4. Write XACR2 and XACR3, if the XA/XB pins are connected to a crystal.
5. Write MCR2.XAB[1:0] to configure the XA/XB pins, if these pins are used in the application.
6. If XAB[1:0] was set to 01 (crystal operation) above then wait 5ms for the crystal circuit to stabilize.
7. If the XA doubler is used in the application, set MCR2.DBL=1. At the same time set the input monitor reference clock sources in MCR2 bits 7:4, if input monitors are used in the application.
8. Write XACR1, IC1CR1, IC2CR1 and IC3CR1 to configure the input clocks.
9. Enable input clocks by setting ICEN register bits.
10. Set output bank source fields in OCMUX1 and OCMUX2 registers.
11. Configure the GPIO pins using the GPIOCR1 through GPIO3SS registers.
12. Configure the APLL1 registers (0x100 through 0x11C).
13. Configure the APLL1 low-level analog as instructed for the application in the *APLL Analog Configuration* section below.
14. Configure the APLL1 fractional output divider registers (0x140 through 0x14E)
15. Configure the APLL1 fractional output divider low-level analog as instructed for the application in the *Fractional Output Divider Analog Configuration* section below.
16. Configure the APLL2 registers (0x180 through 0x19C).
17. Configure the APLL2 low-level analog as instructed for the application in the *APLL Analog Configuration* section below.
18. Configure the APLL2 fractional output divider registers (0x1C0 through 0x1CE)
19. Configure the APLL2 fractional output divider low-level analog as instructed for the application in the *Fractional Output Divider Analog Configuration* section below.

20. Configure the output divider registers (0x200 through 0x29A)
21. APLL1 relock sequence: Set 0x430[3:2] = 00 then 11 then 00.
22. APLL2 relock sequence: Set 0x435[3:2] = 00 then 11 then 00.
23. Wait 2ms
24. Align participating APLL1 outputs: ACR1.DALIGN=0 then 1
25. Align participating APLL2 outputs: A2CR1.DALIGN=0 then 1
26. Set MCR1.ROSCD bit to 1 to disable the ring oscillator.
27. Set interrupt enable bits and clear latched status bits as needed in the status registers (addresses 0x40 through 0x59).
28. Set MCR1.STOP=0 and/or clear appropriate bits in STOPCR1 and STOPCR2 to start outputs as desired.

APLL Analog Configuration

The writes below are used for configuration steps 13 and 17 above.

For APLL1 offset is 0. For APLL2 offset is 0x80.

For APLL1 DTCR is 0x423. For APLL2 DTCR is 0x424.

If spread spectrum is enabled:

Write address offset+0x120 with 0xC1
If VDDH is 3.3V Write address offset+0x121 with 0x60
If VDDH is 2.5V Write address offset+0x121 with 0x48
Write address offset+0x122 with 0xA8
Write address offset+0x123 with 0x00
Write address offset+0x124 with 0x00
Write address offset+0x125 with 0xB3
Write address offset+0x126 with 0x98
Write address offset+0x127 with 0x90
Write address DTCR with 0x1B

Else If not NCO mode and AFBDIV is an integer:

Write address offset+0x120 with 0xC0
If APLL input frequency after the divider is >= 50MHz
    If VDDH is 3.3V Write address offset+0x121 with 0x40
    If VDDH is 2.5V Write address offset+0x121 with 0x08
Else
    If VDDH is 3.3V Write address offset+0x121 with 0x60
    If VDDH is 2.5V Write address offset+0x121 with 0x48
Write address offset+0x122 with 0x7F
Write address offset+0x123 with 0x00
Write address offset+0x124 with 0x04
Write address offset+0x125 with 0xB3
Write address offset+0x126 with 0xD8
Write address offset+0x127 with 0x90
Write address DTCR with 0x08

Else If not NCO mode and AFBDIV fractional part is exactly 0.5 (examples: 37.5, 38.5, 39.5):

If APLL input frequency after the divider is >= 50MHz
    Write address offset+0x120 with 0xC3
Else
    Write address offset+0x120 with 0xC7
If VDDH is 3.3V Write address offset+0x121 with 0x40
If VDDH is 2.5V Write address offset+0x121 with 0x08

Write address offset+0x122 with 0x7F
Write address offset+0x123 with 0x00
Write address offset+0x124 with 0x04
Write address offset+0x125 with 0xB3
Write address offset+0x126 with 0xD8
If APLL input frequency after the divider is > 50MHz
    Write address offset+0x127 with 0x90
Else
    Write address offset+0x127 with 0x50
Write address DTCR with 0x08

Else // NCO mode or AFBDIV is not a multiple of 0.5

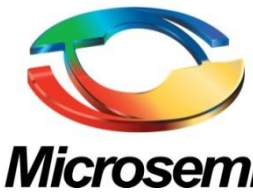
Write address offset+0x120 with 0xC7
If VDDH is 3.3V Write address offset+0x121 with 0x40
If VDDH is 2.5V Write address offset+0x121 with 0x08
Write address offset+0x122 with 0x5F
Write address offset+0x123 with 0x00
Write address offset+0x124 with 0x04
Write address offset+0x125 with 0xB3
Write address offset+0x126 with 0x98
If APLL input frequency after the divider is > 80MHz
    Write address offset+0x127 with 0x90
Else
    Write address offset+0x127 with 0x50
Write address DTCR with 0x1B

Fractional Output Divider Analog Configuration

The writes below are used for configuration steps 15 and 19 above.

For APLL1 offset is 0. For APLL2 offset is 0x80.

Write address offset+0x151 with 0x15
Write address offset+0x152 with 0x01
Write address offset+0x153 with 0x00
If fdivPeriod < 3.7 Write address offset+0x154 with 0x40
If 3.7 ≤ fdivPeriod < 5.7 Write address offset+0x154 with 0x50
If 5.7 ≤ fdivPeriod < 7.7 Write address offset+0x154 with 0x60
If 7.7 ≤ fdivPeriod Write address offset+0x154 with 0x70
If APLL1
    Write address offset+0x155 with 0xCE
Else
    Write address offset+0x155 with 0x0E
(where fdivPeriod is the period of the clock signal produced by the fractional divider in ns)



Microsemi Corporate Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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