Total Ionizing Dose Test Report

No. 18T-RT4G150-LG1657-KYJWW

March 5, 2018

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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 1. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	KYJWW
Quantity Tested	6
Serial Number (Dose)	4595 (125 krad), 4650 (125 krad), 4674 (125 krad), 4691 (125 krad), 4750 (125 krad), 4764 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

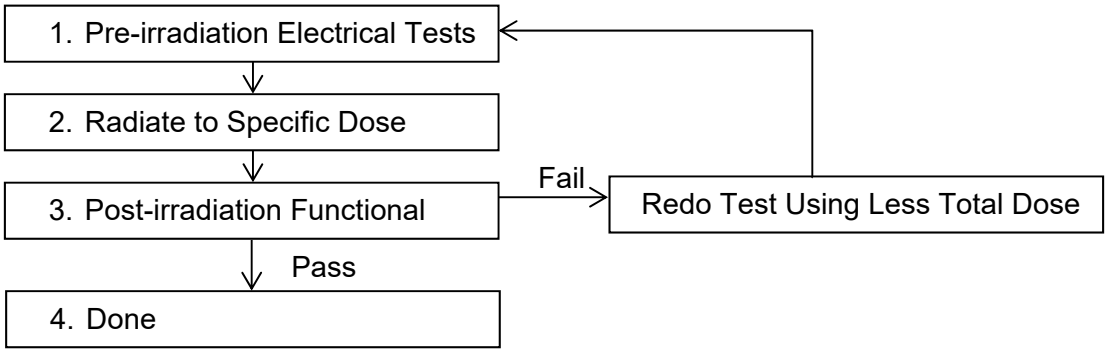

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 2. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 3. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
4595	125 krad	0.2903	0.3004	3.48
4650	125 krad	0.2675	0.2705	1.12
4674	125 krad	0.2641	0.2673	1.21
4691	125 krad	0.2605	0.2701	3.69
4750	125 krad	0.2873	0.2918	1.57
4764	125 krad	0.2697	0.2766	2.56

Table. 4. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
4595	125 krad	0.0098	0.0123	25.51
4650	125 krad	0.0092	0.0116	26.09
4674	125 krad	0.0094	0.0119	26.60
4691	125 krad	0.0088	0.0111	26.14
4750	125 krad	0.0081	0.0103	27.16
4764	125 krad	0.0091	0.0115	26.37

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
4595	125 krad	0.0348	0.0376	8.05
4650	125 krad	0.0344	0.0374	8.72
4674	125 krad	0.0347	0.0378	8.93
4691	125 krad	0.0340	0.0370	8.82
4750	125 krad	0.0336	0.0364	8.33
4764	125 krad	0.0340	0.0370	8.82

Table. 6. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
4595	125 krad	0.0155	0.0345	122.58
4650	125 krad	0.0158	0.0228	44.30
4674	125 krad	0.0157	0.0230	46.50
4691	125 krad	0.0156	0.0242	55.13
4750	125 krad	0.0155	0.0210	35.48
4764	125 krad	0.0155	0.0367	136.77

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

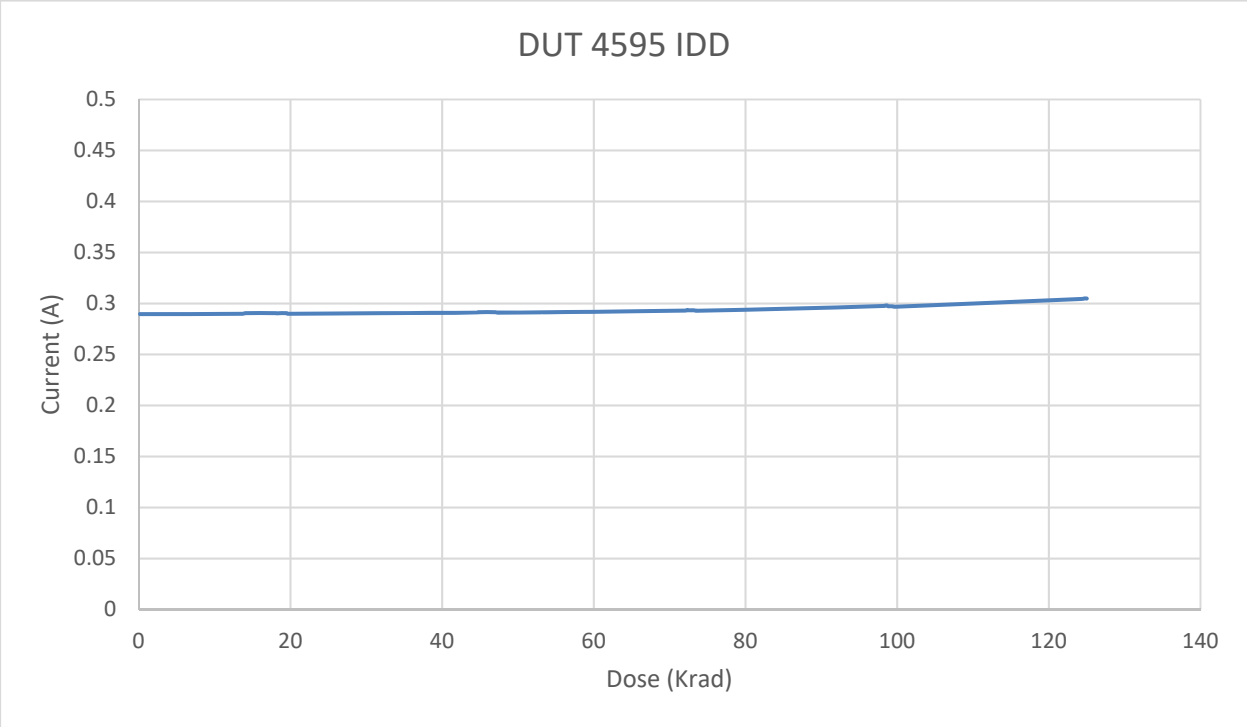

Fig. 2. DUT 4595 core power supply current (I_{DD}) versus TID

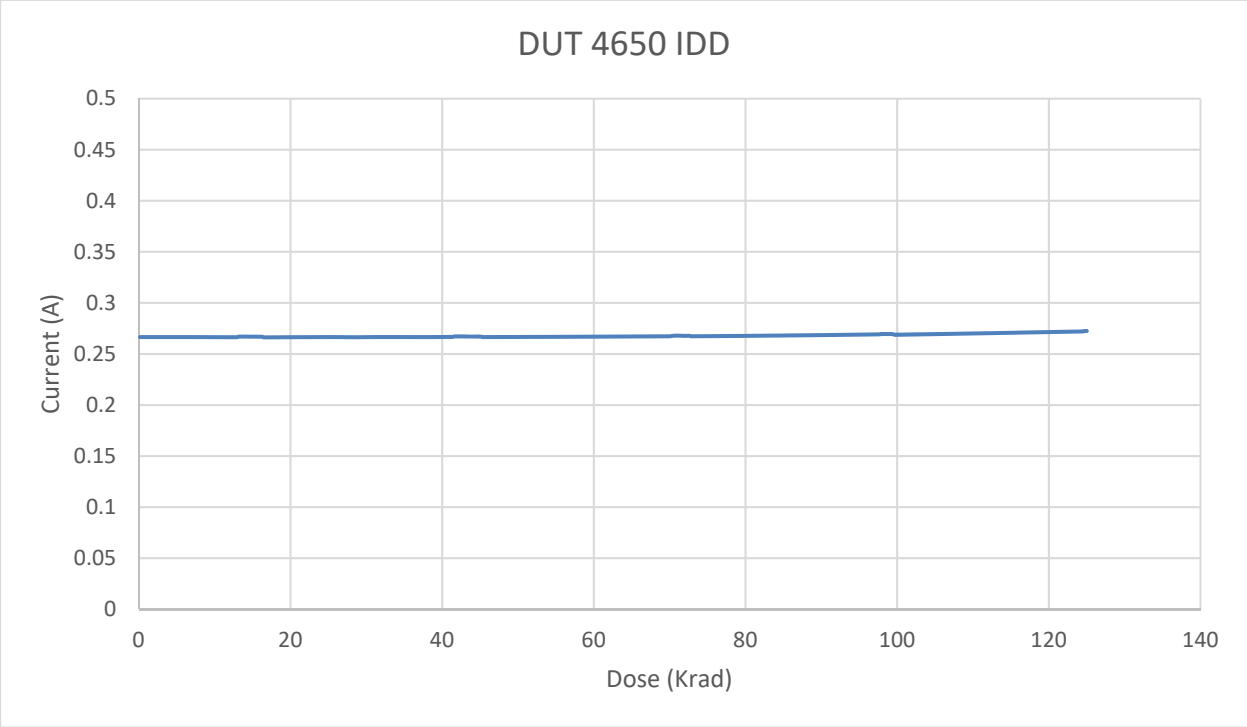

Fig. 3. DUT 4650 core power supply current (I_{DD}) versus TID

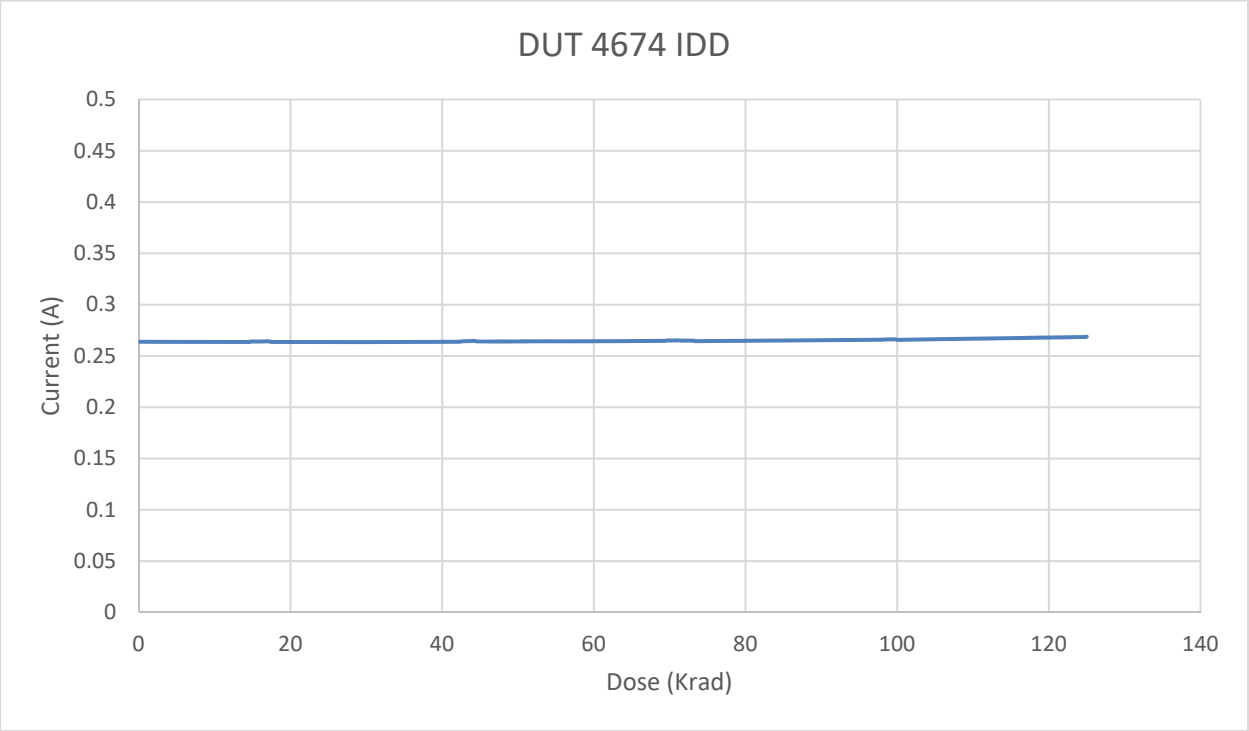

Fig. 4. DUT 4674 core power supply current (I_{DD}) versus TID

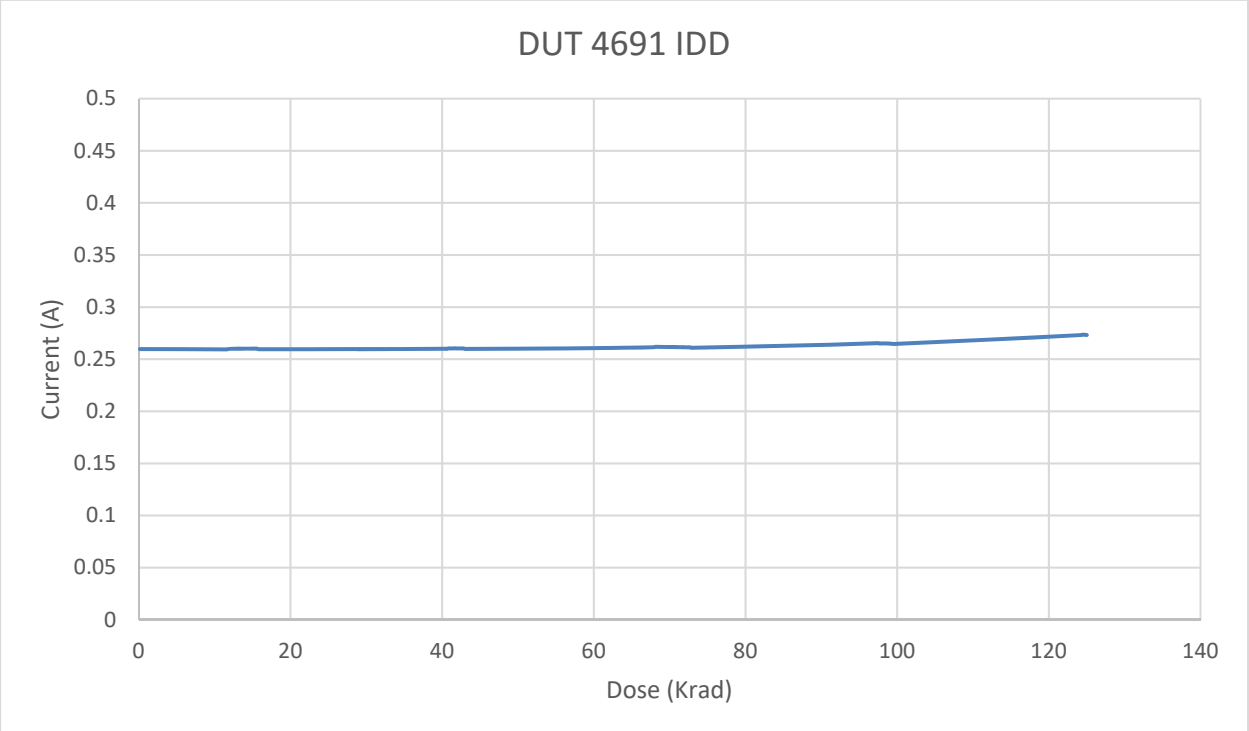

Fig. 5. DUT 4691 core power supply current (I_{DD}) versus TID

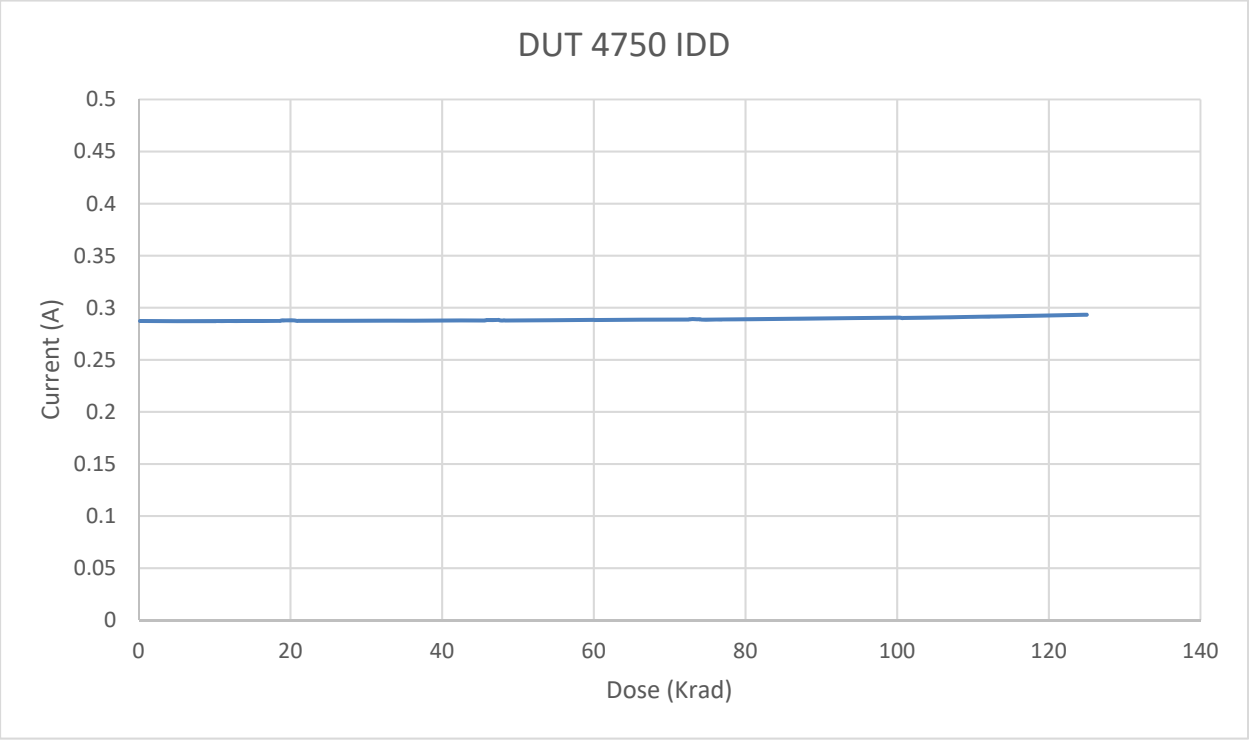

Fig. 6. DUT 4750 core power supply current (I_{DD}) versus TID

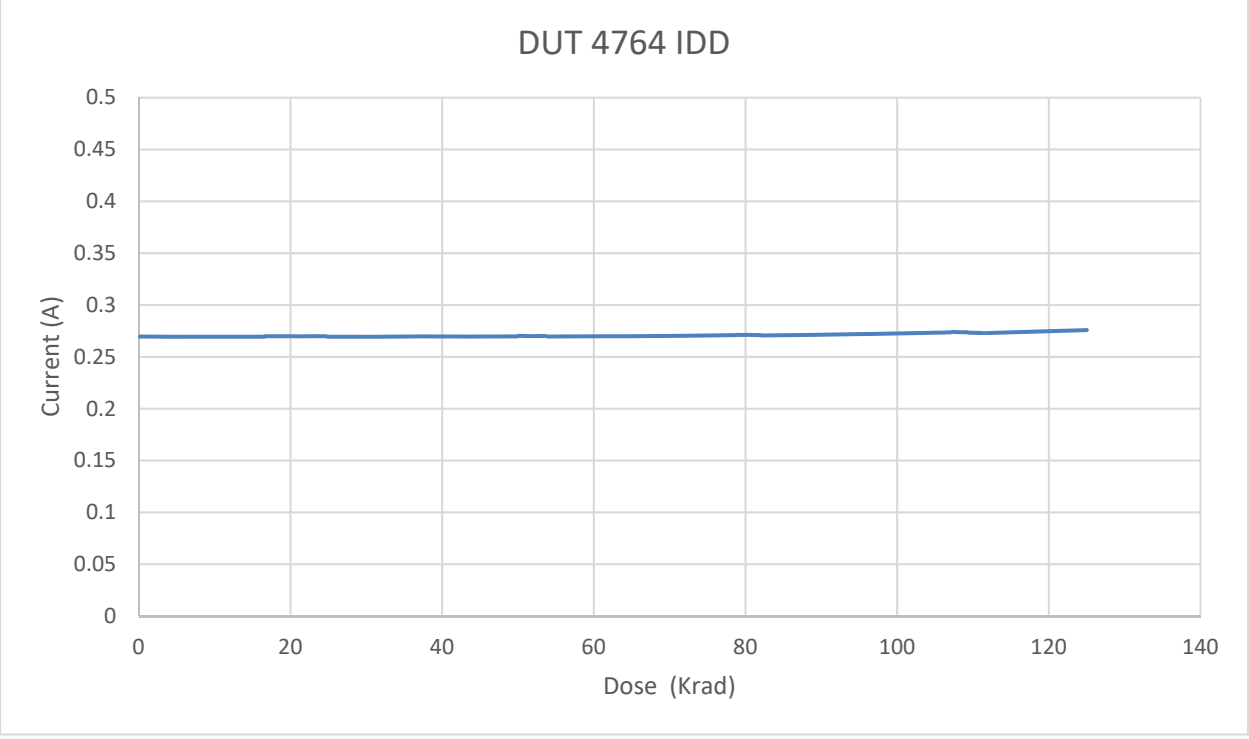

Fig. 7. DUT 4764 core power supply current (I_{DD}) versus TID

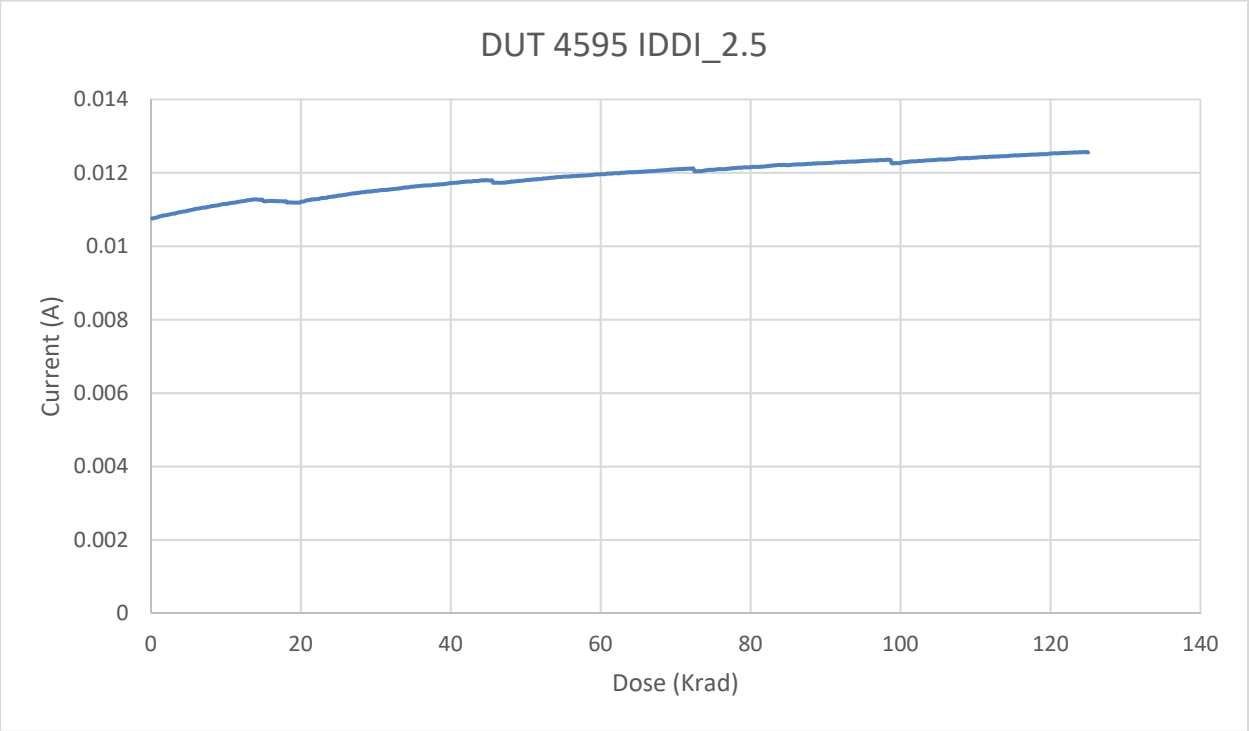

Fig. 8. DUT 4595 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

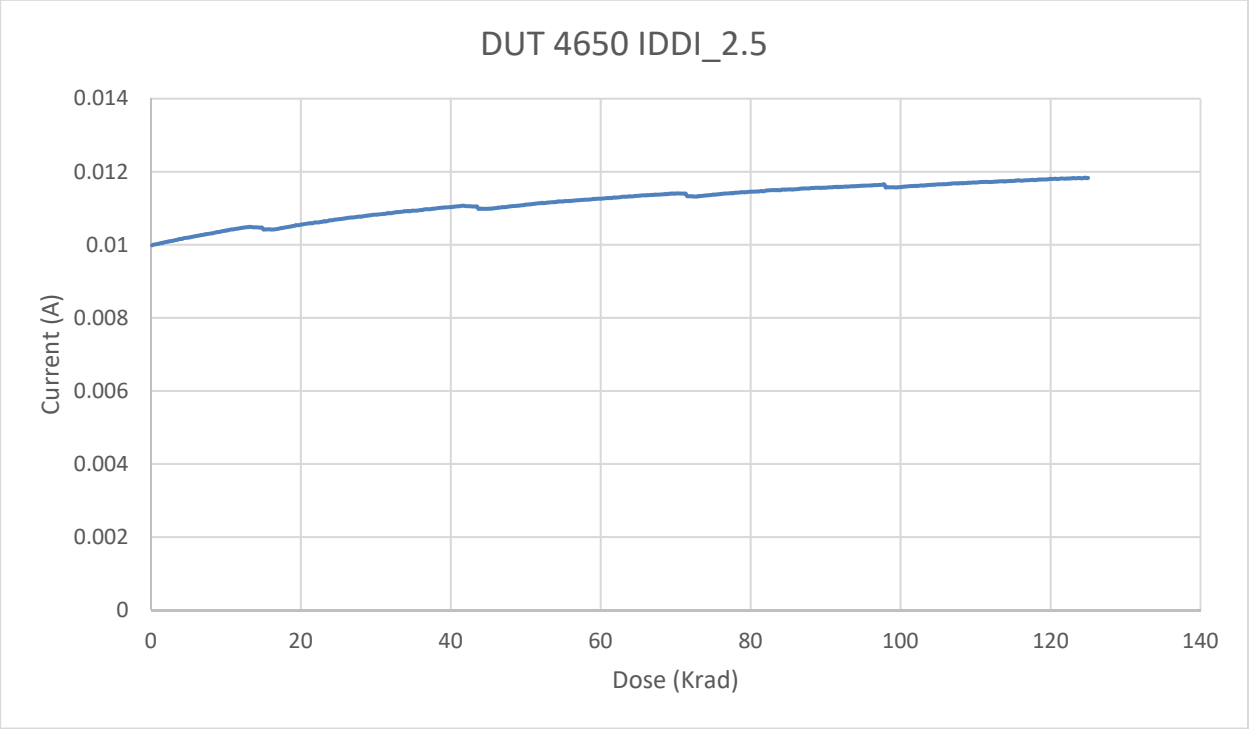

Fig. 9. DUT 4650 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

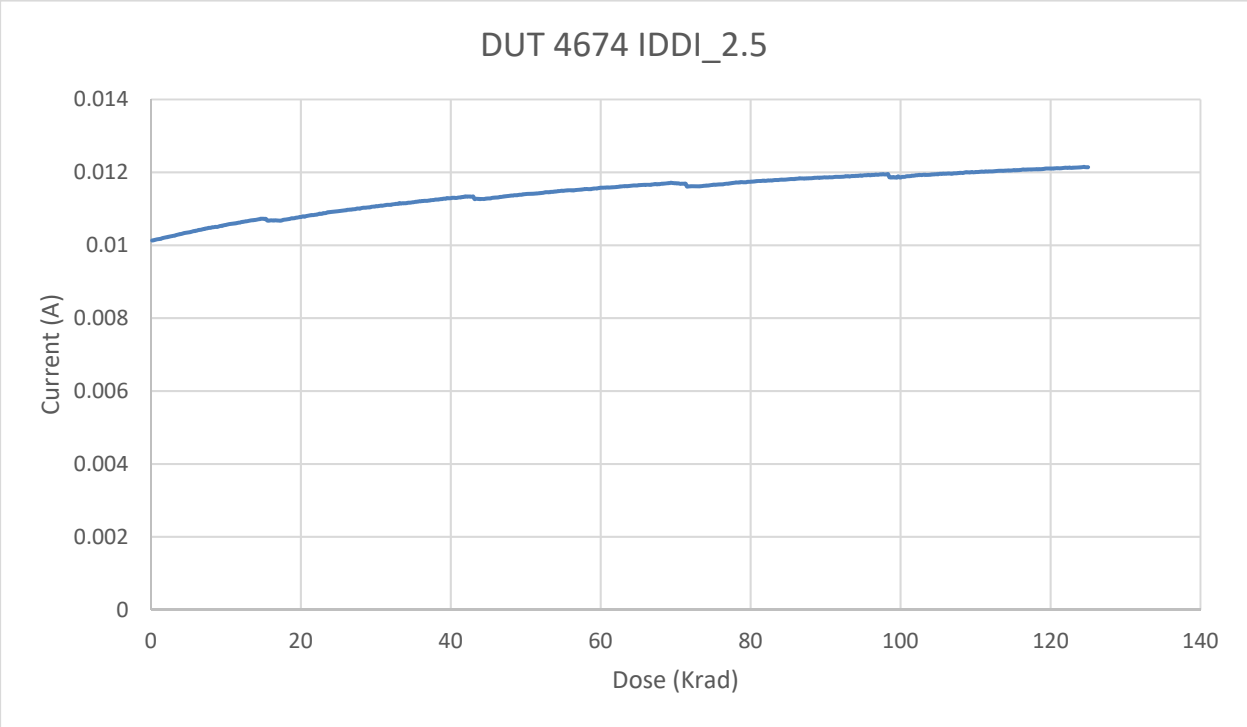

Fig. 10. DUT 4674 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

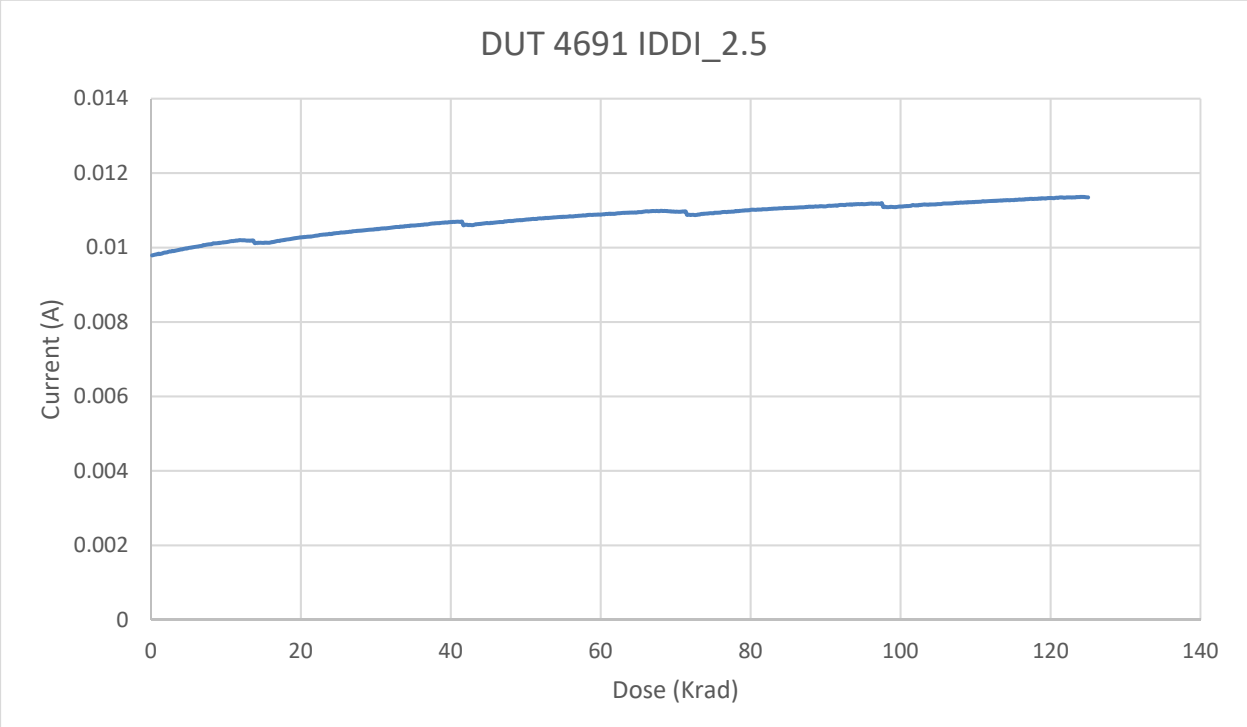

Fig. 11. DUT 4691 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

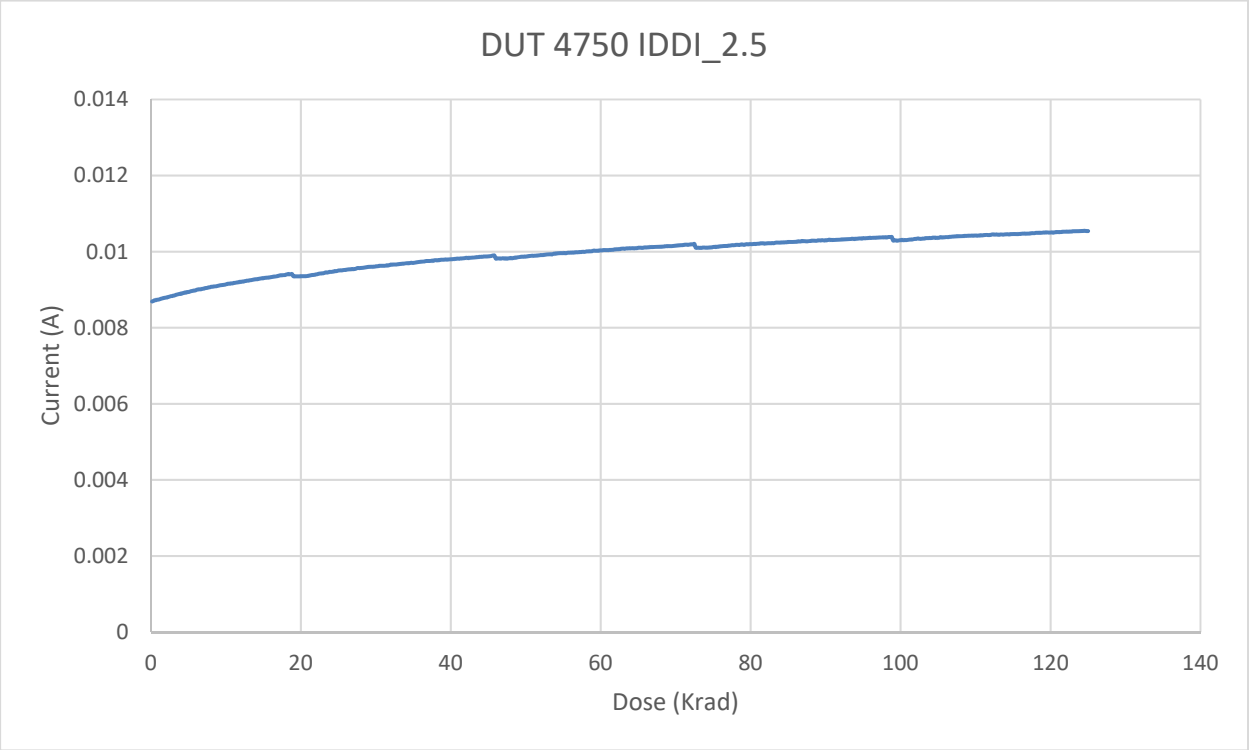

Fig. 12. DUT 4750 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

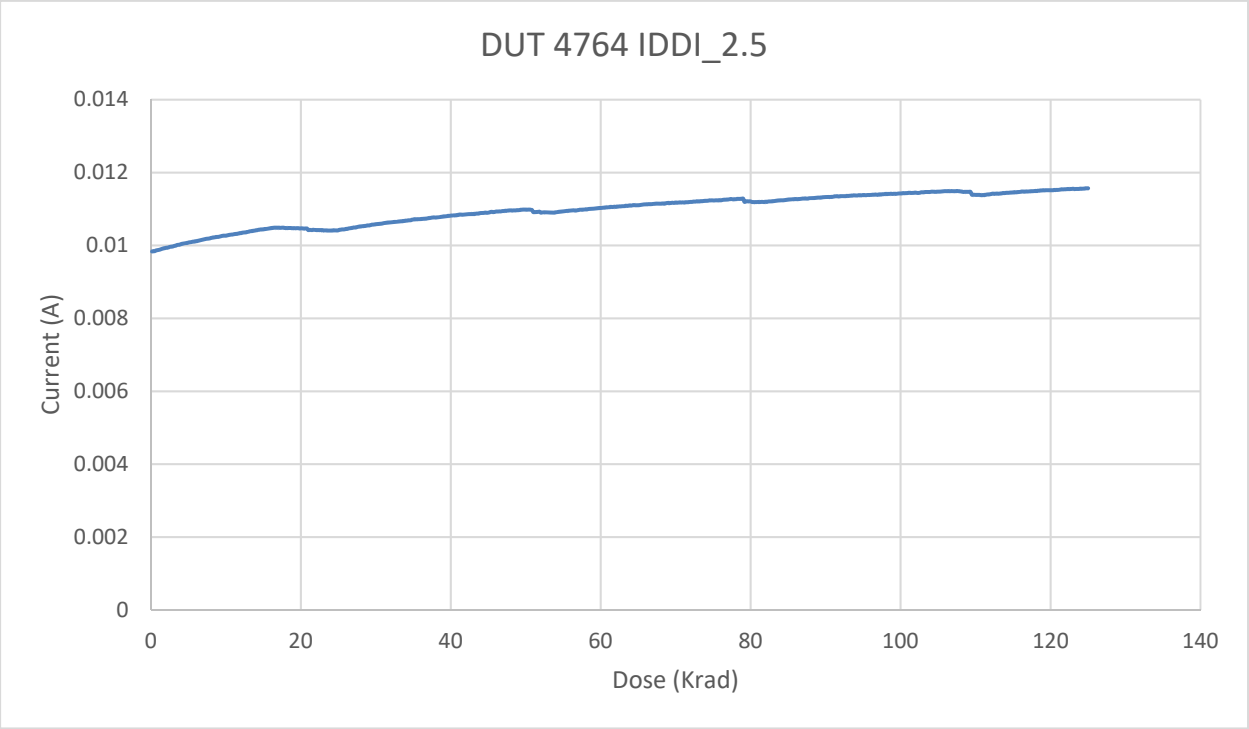

Fig. 13. DUT 4764 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

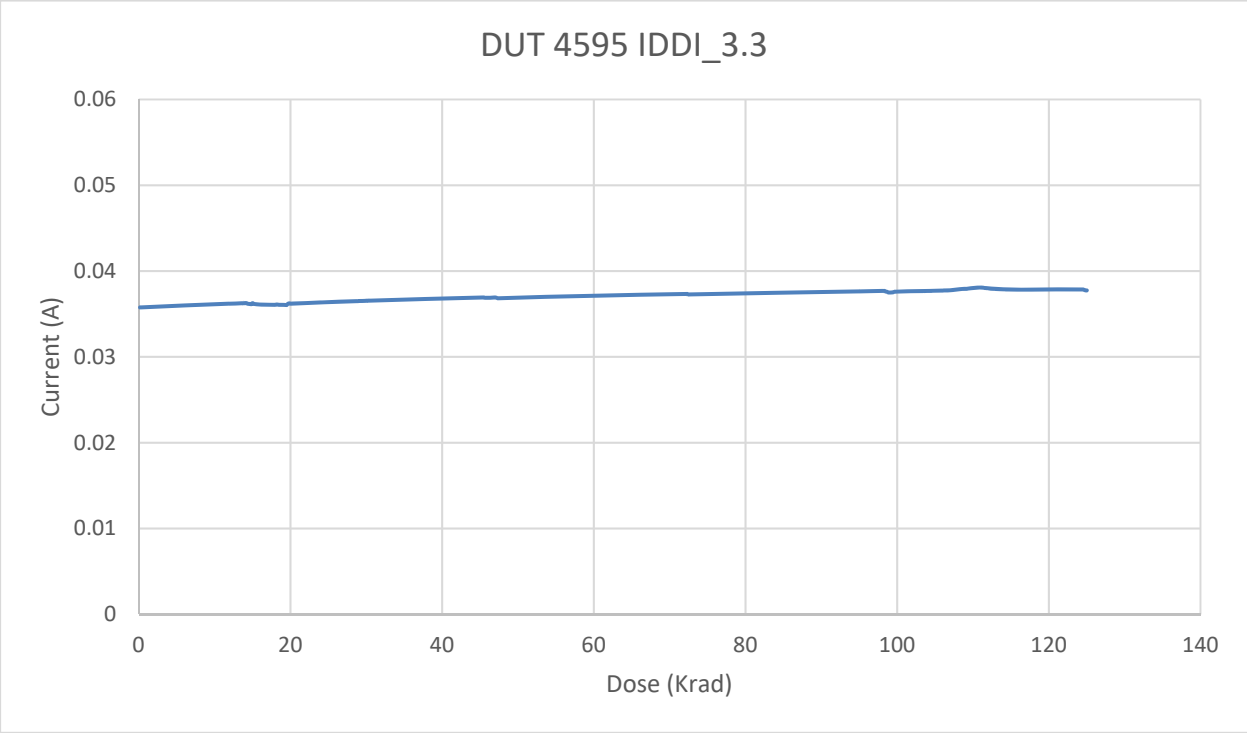

Fig. 14. DUT 4595 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

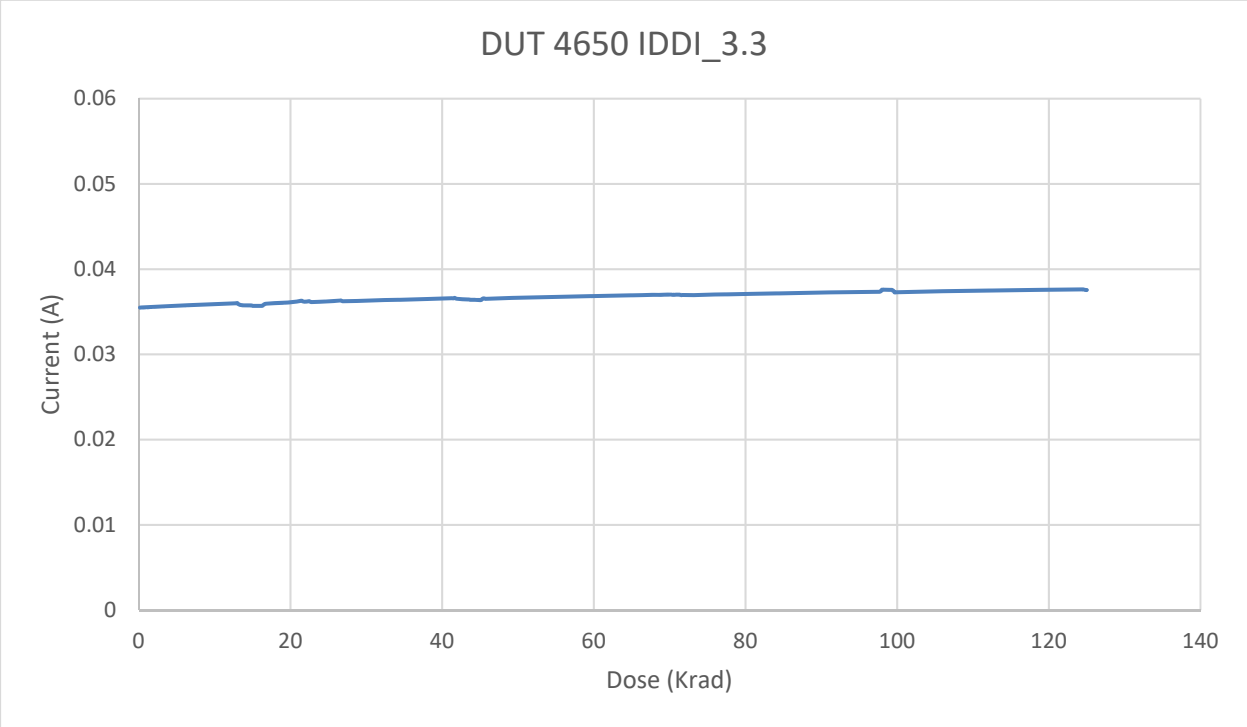

Fig. 15. DUT 4650 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

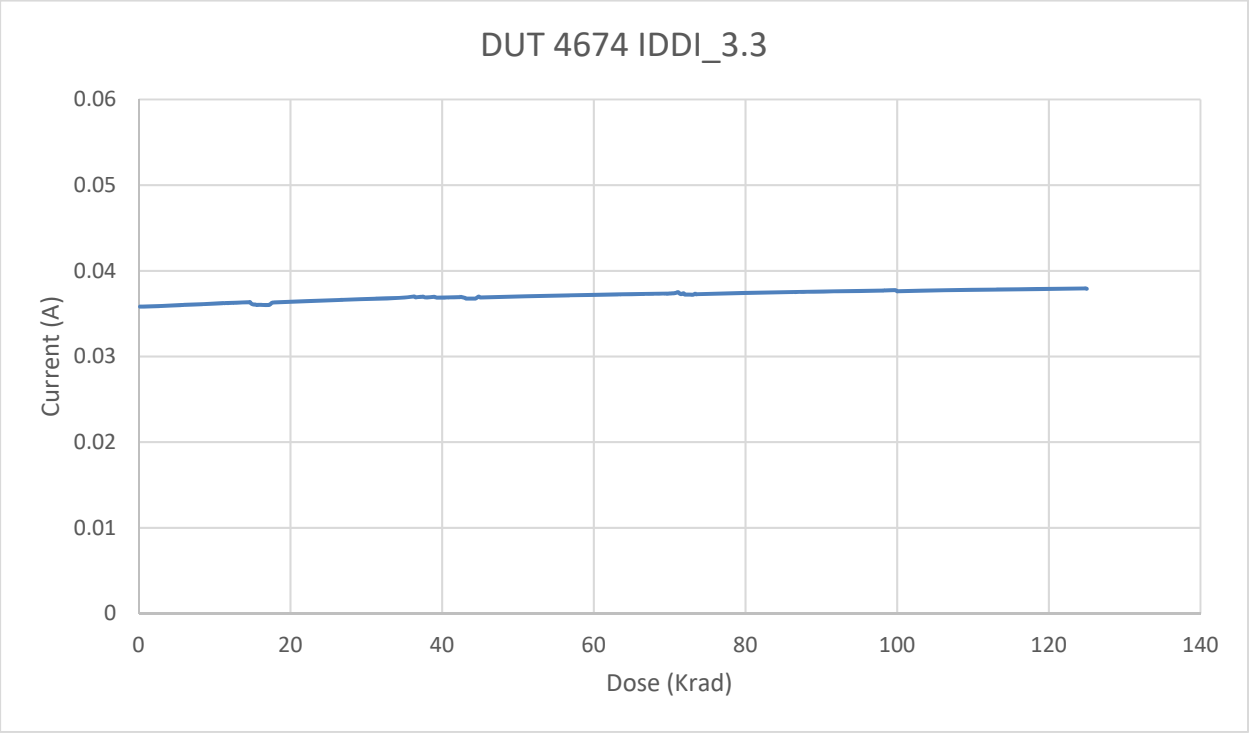

Fig. 16. DUT 4674 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

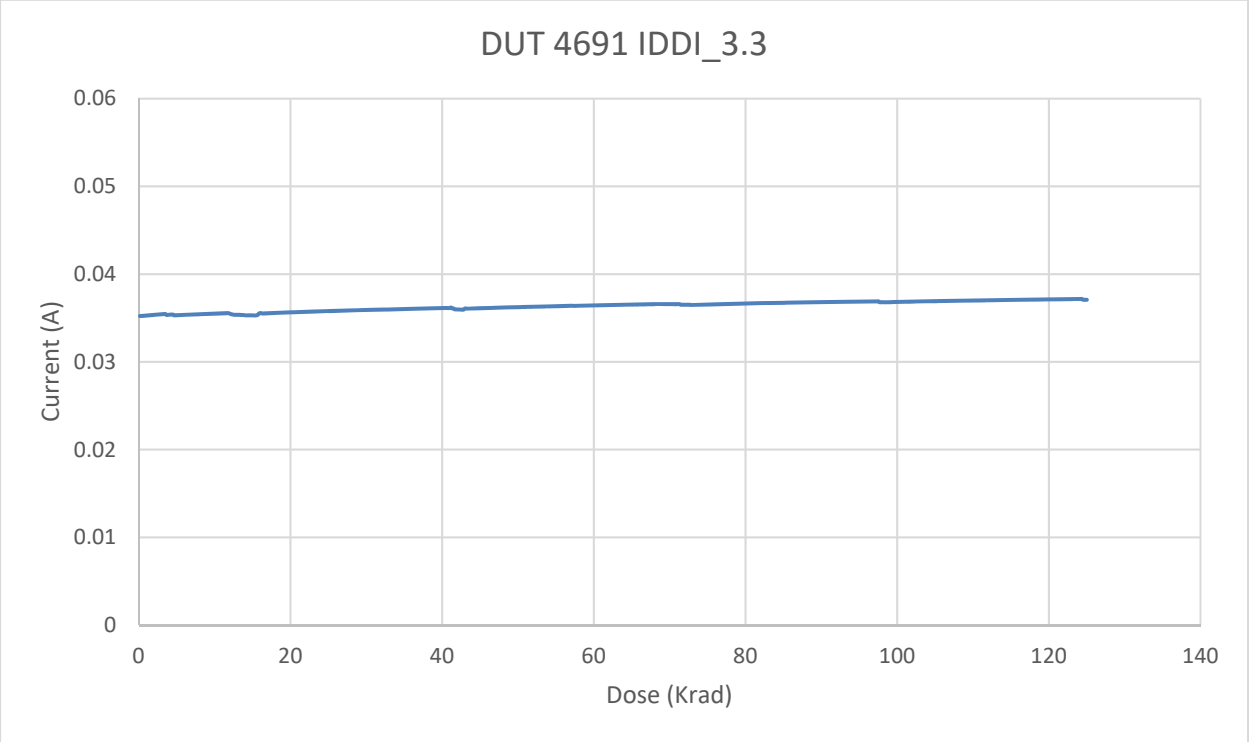

Fig. 17. DUT 4691 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

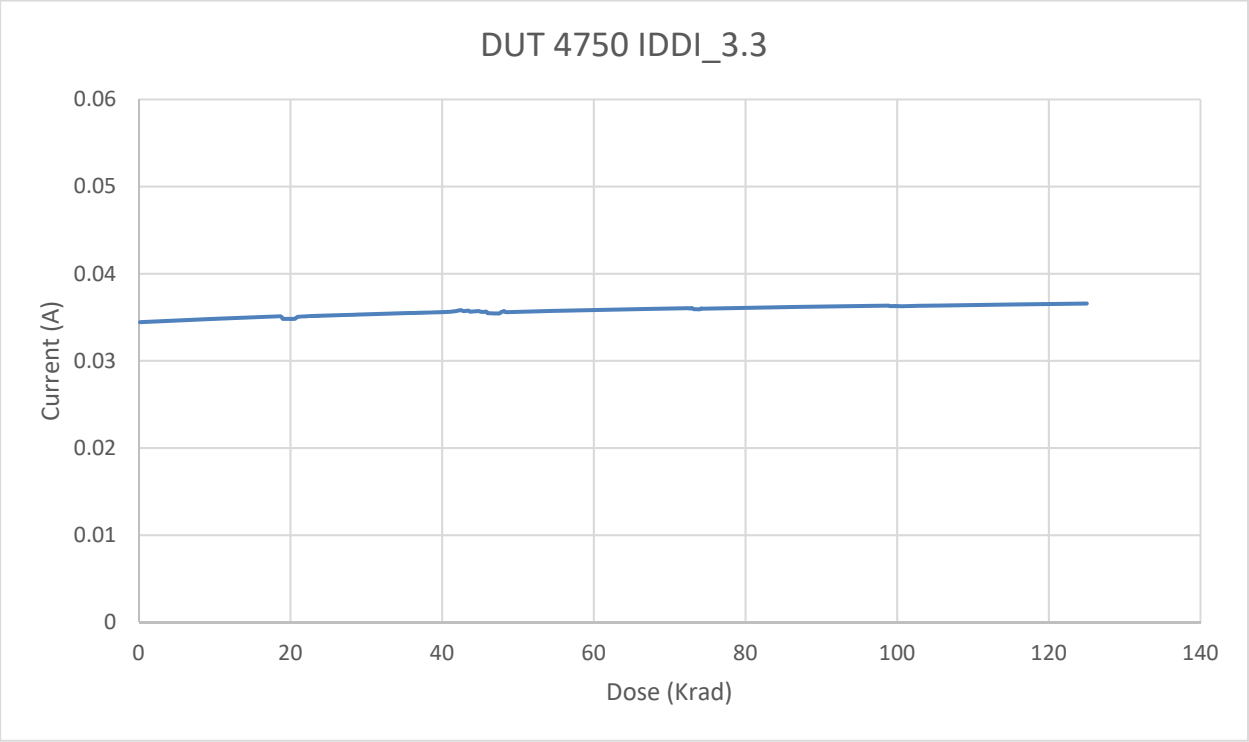

Fig. 18. DUT 4750 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

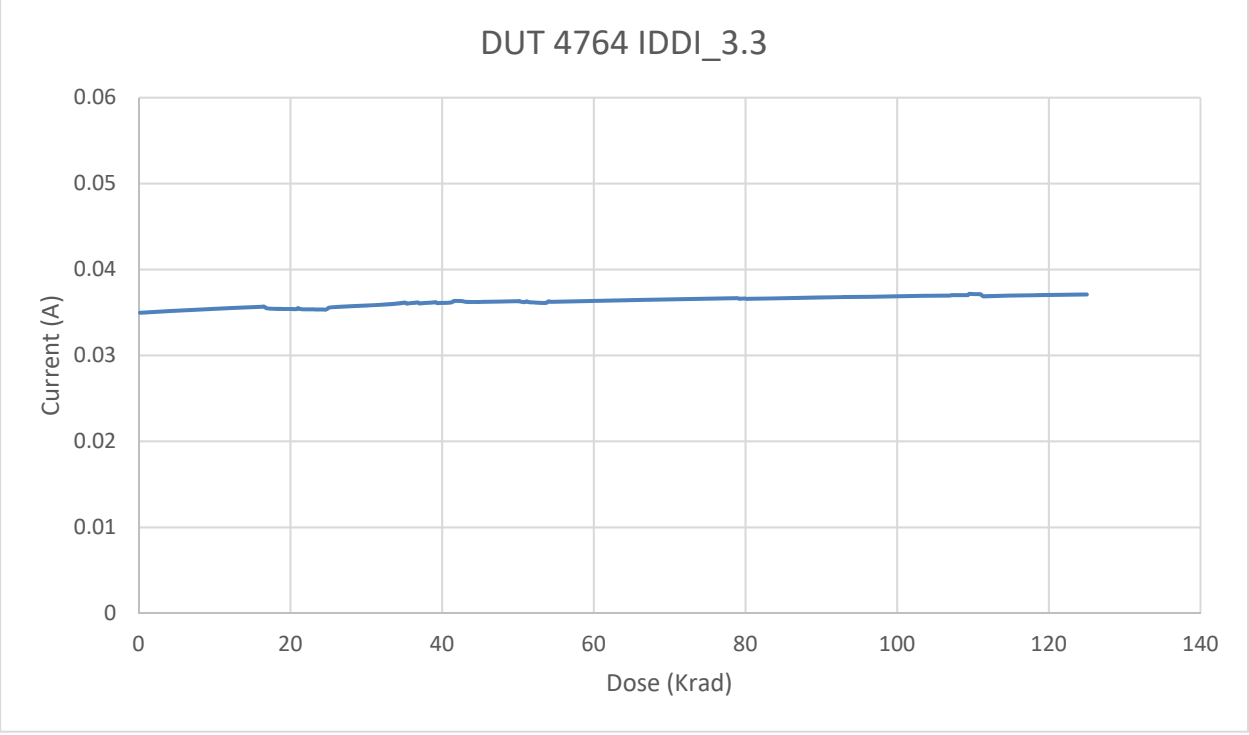

Fig. 19. DUT 4764 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

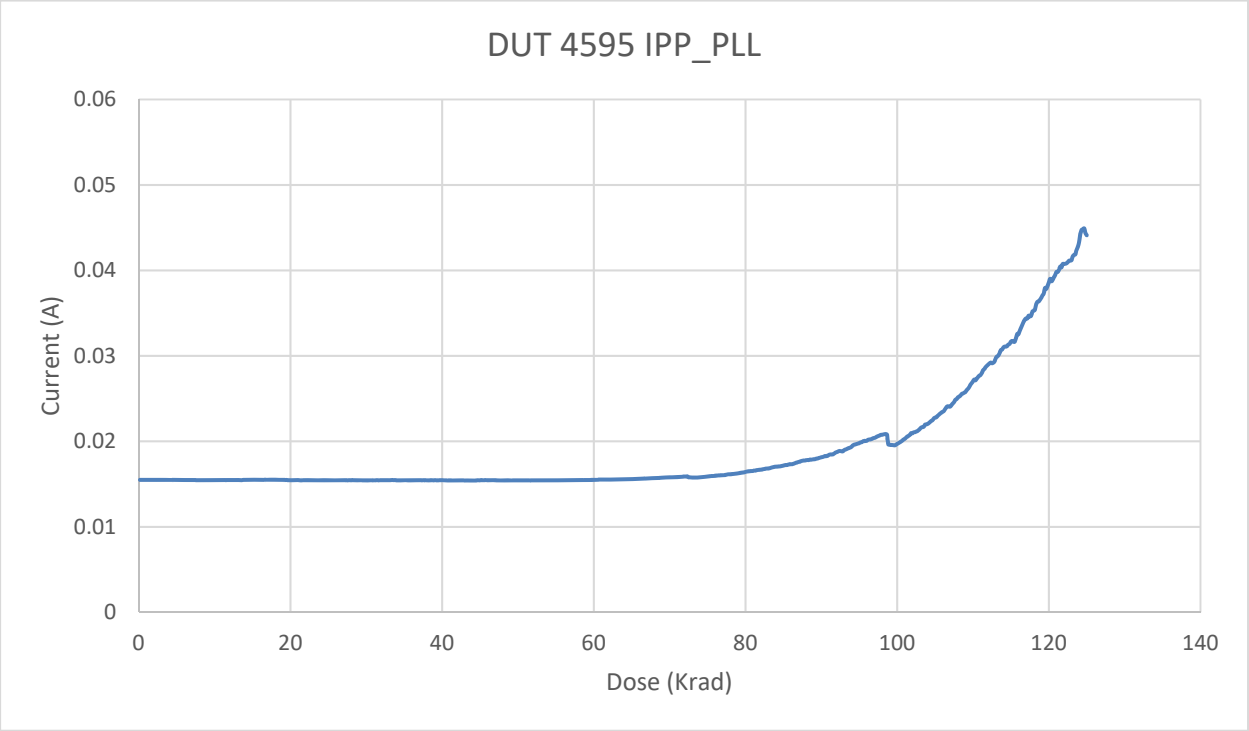

Fig. 20. DUT 4595 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

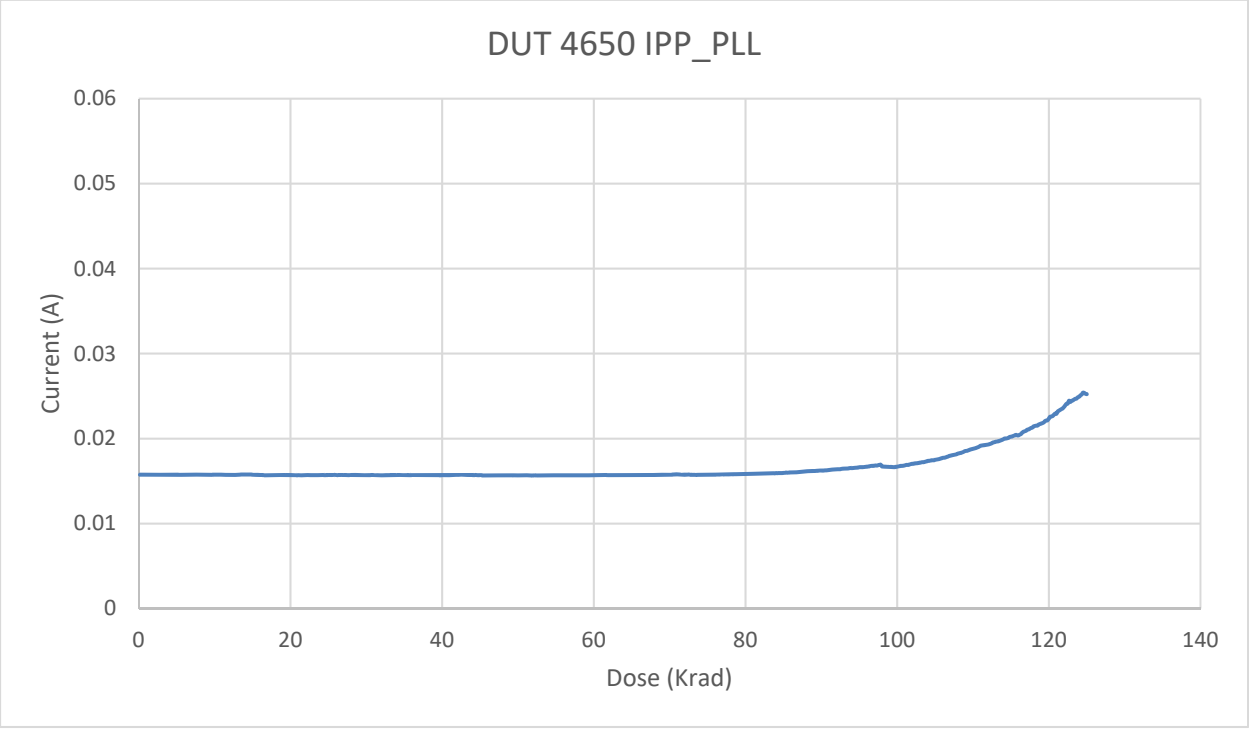

Fig. 21. DUT 4650 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

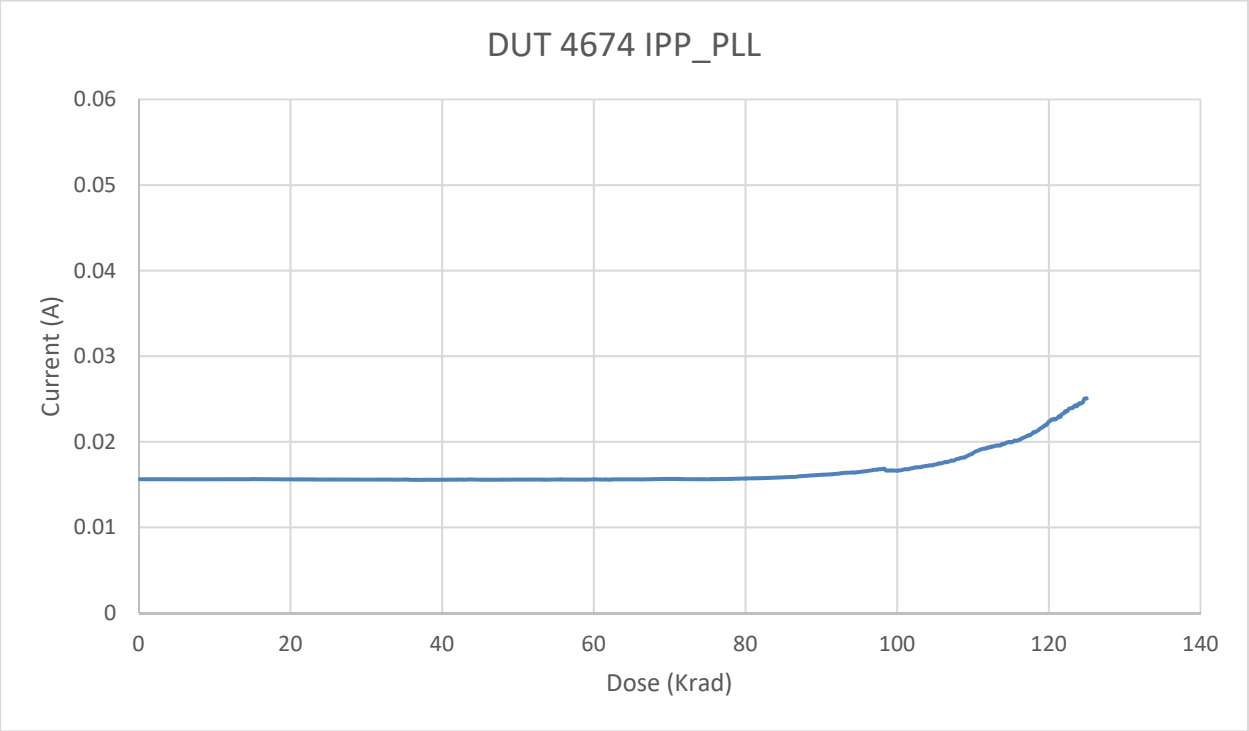

Fig. 22. DUT 4674 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

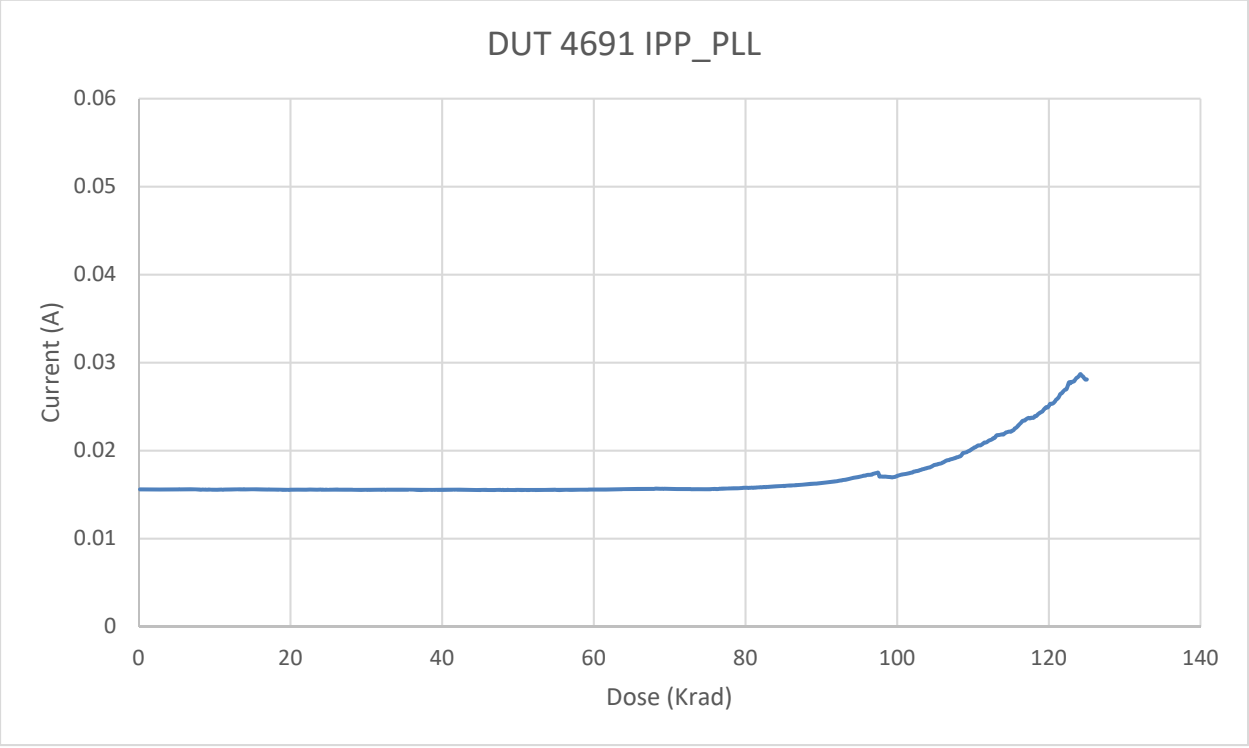

Fig. 23. DUT 4691 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

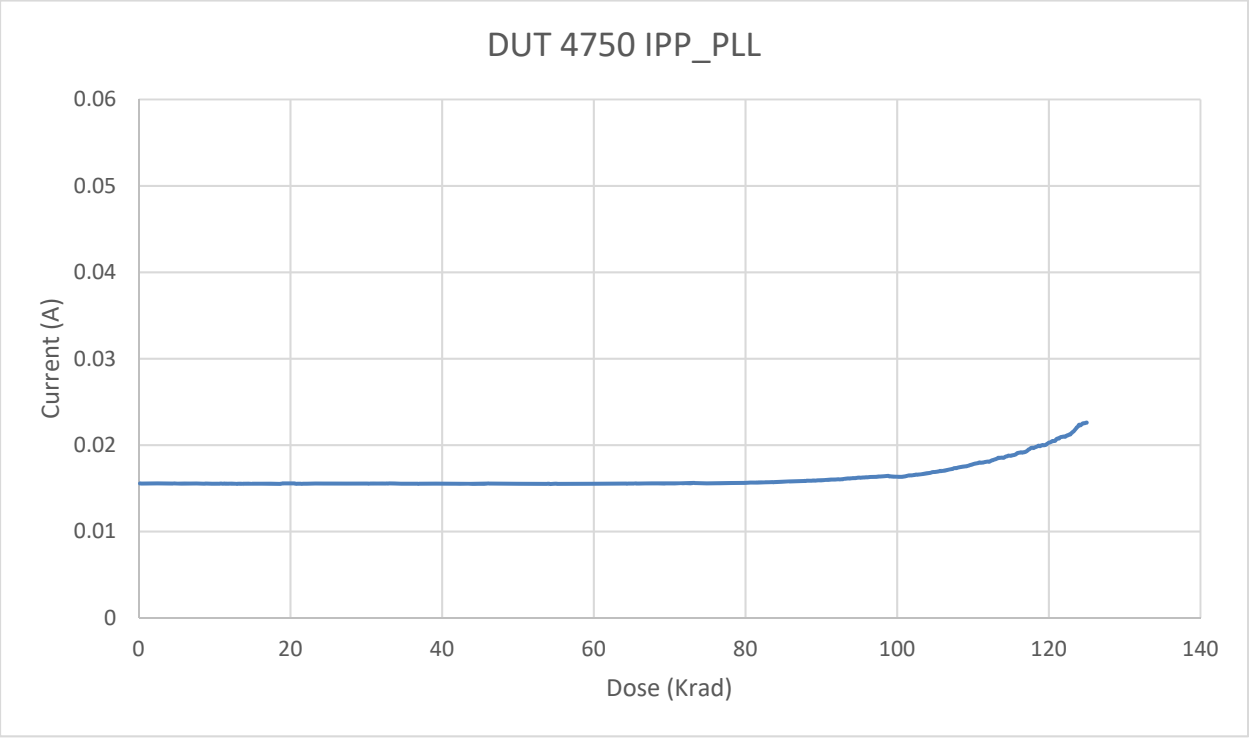

Fig. 24. DUT 4750 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

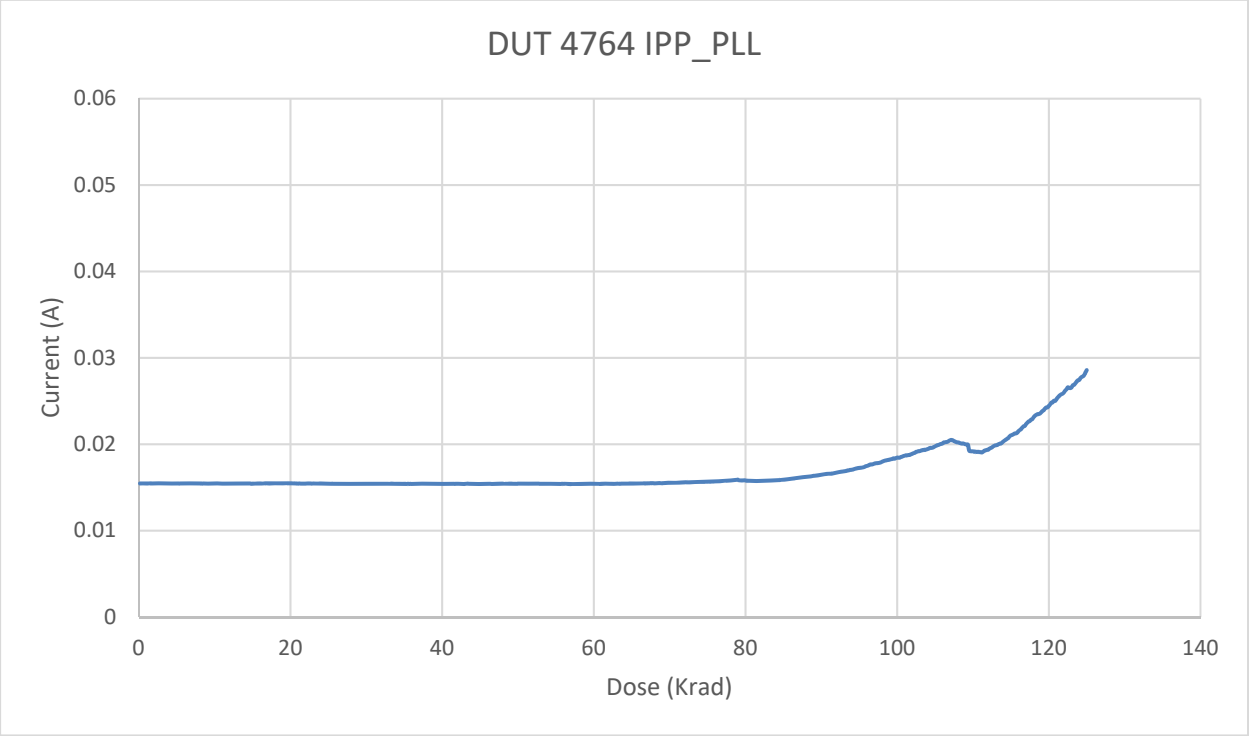

Fig. 25. DUT 4764 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 7. VIH Summary

DUT	Pre-irradiation	Post-irradiation
4595	Passed	Passed
4650	Passed	Passed
4674	Passed	Passed
4691	Passed	Passed
4750	Passed	Passed
4764	Passed	Passed

Table. 8. VIL Summary

DUT	Pre-irradiation	Post-irradiation
4595	Passed	Passed
4650	Passed	Passed
4674	Passed	Passed
4691	Passed	Passed
4750	Passed	Passed
4764	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 9 through 32 are sampled on several pins used in the burn in design.

Table. 9. LVCMOS 25 VOH – DUT 4595

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.131	2.129	2.198	2.194	2.169	2.162	2.149	2.138	2.115	2.097	2.100	2.080
EPCSRST_N_0	B31	2.131	2.130	2.199	2.193	2.169	2.159	2.148	2.134	2.114	2.092	2.098	2.072
EPCSRST_N_1	B32	2.133	2.135	2.201	2.203	2.172	2.174	2.152	2.153	2.119	2.120	2.106	2.106
EPCSRST_N_2	B34	2.130	2.132	2.199	2.201	2.169	2.171	2.148	2.150	2.114	2.116	2.100	2.102
EPCSRST_N_3	B35	2.131	2.133	2.201	2.203	2.172	2.174	2.152	2.153	2.120	2.121	2.106	2.107
EPCSRST_N_4	B36	2.130	2.132	2.198	2.200	2.169	2.170	2.147	2.148	2.113	2.114	2.098	2.099
EPCSRST_N_5	B37	2.131	2.132	2.200	2.199	2.171	2.169	2.150	2.147	2.118	2.111	2.104	2.096
MONITOR	K23	2.135	2.134	2.204	2.203	2.176	2.175	2.156	2.154	2.126	2.123	2.113	2.110
PLL_MON	L20	2.135	2.135	2.208	2.205	2.179	2.178	2.161	2.160	2.137	2.131	2.114	2.119
TOGGLE_MON	L22	2.135	2.135	2.205	2.205	2.178	2.178	2.159	2.158	2.130	2.129	2.117	2.117

Table. 10. LVCMOS 25 VOH – DUT 4650

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.123	2.126	2.189	2.192	2.156	2.159	2.132	2.135	2.091	2.095	2.073	2.077
EPCSRST_N_0	B31	2.126	2.126	2.194	2.190	2.162	2.156	2.140	2.131	2.103	2.088	2.086	2.069
EPCSRST_N_1	B32	2.128	2.131	2.198	2.200	2.169	2.171	2.148	2.150	2.114	2.117	2.100	2.103
EPCSRST_N_2	B34	2.127	2.130	2.197	2.199	2.167	2.170	2.146	2.148	2.113	2.115	2.098	2.100
EPCSRST_N_3	B35	2.127	2.130	2.198	2.201	2.169	2.172	2.149	2.151	2.117	2.119	2.103	2.105
EPCSRST_N_4	B36	2.127	2.129	2.196	2.198	2.165	2.168	2.143	2.147	2.109	2.113	2.094	2.098
EPCSRST_N_5	B37	2.126	2.129	2.194	2.198	2.163	2.167	2.140	2.145	2.104	2.110	2.088	2.095
MONITOR	K23	2.130	2.129	2.201	2.200	2.173	2.171	2.153	2.151	2.123	2.120	2.110	2.107
PLL_MON	L20	2.131	2.130	2.203	2.202	2.176	2.175	2.157	2.156	2.128	2.127	2.116	2.115
TOGGLE_MON	L22	2.130	2.130	2.202	2.201	2.175	2.174	2.155	2.154	2.126	2.125	2.114	2.113

Table. 11. LVCMOS 25 VOH – DUT 4674

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.126	2.128	2.192	2.194	2.159	2.162	2.136	2.139	2.096	2.099	2.079	2.082
EPCSRST_N_0	B31	2.129	2.128	2.196	2.193	2.165	2.159	2.144	2.135	2.108	2.093	2.092	2.074
EPCSRST_N_1	B32	2.131	2.133	2.200	2.203	2.171	2.174	2.151	2.153	2.119	2.121	2.105	2.108
EPCSRST_N_2	B34	2.129	2.132	2.199	2.201	2.170	2.172	2.149	2.151	2.116	2.118	2.102	2.105
EPCSRST_N_3	B35	2.130	2.132	2.200	2.203	2.172	2.174	2.152	2.154	2.120	2.123	2.107	2.110
EPCSRST_N_4	B36	2.129	2.132	2.198	2.201	2.168	2.171	2.146	2.149	2.113	2.116	2.098	2.101
EPCSRST_N_5	B37	2.130	2.131	2.199	2.200	2.170	2.170	2.149	2.147	2.116	2.113	2.102	2.099
MONITOR	K23	2.132	2.131	2.202	2.201	2.175	2.173	2.155	2.153	2.125	2.122	2.112	2.109
PLL_MON	L20	2.133	2.132	2.204	2.204	2.177	2.176	2.158	2.158	2.130	2.129	2.118	2.117
TOGGLE_MON	L22	2.132	2.132	2.204	2.203	2.176	2.176	2.157	2.156	2.128	2.127	2.116	2.116

Table. 12. LVCMOS 25 VOH – DUT 4691

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.127	2.129	2.193	2.195	2.160	2.162	2.137	2.139	2.097	2.099	2.080	2.082
EPCSRST_N_0	B31	2.130	2.129	2.196	2.193	2.166	2.160	2.144	2.135	2.108	2.093	2.092	2.075
EPCSRST_N_1	B32	2.132	2.134	2.200	2.203	2.172	2.175	2.151	2.154	2.119	2.122	2.106	2.108
EPCSRST_N_2	B34	2.130	2.133	2.200	2.203	2.171	2.174	2.150	2.152	2.117	2.120	2.103	2.106
EPCSRST_N_3	B35	2.132	2.135	2.201	2.204	2.173	2.176	2.153	2.156	2.122	2.125	2.109	2.111
EPCSRST_N_4	B36	2.130	2.133	2.198	2.201	2.169	2.171	2.147	2.150	2.113	2.116	2.098	2.101
EPCSRST_N_5	B37	2.131	2.132	2.200	2.200	2.171	2.171	2.150	2.148	2.118	2.114	2.104	2.099
MONITOR	K23	2.132	2.131	2.202	2.201	2.174	2.173	2.155	2.153	2.124	2.122	2.112	2.108
PLL_MON	L20	2.133	2.132	2.204	2.204	2.177	2.176	2.158	2.158	2.130	2.129	2.118	2.117
TOGGLE_MON	L22	2.131	2.133	2.200	2.204	2.171	2.176	2.150	2.157	2.118	2.128	2.104	2.116

Table. 13. LVCMOS 25 VOH – DUT 4750

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.131	2.130	2.199	2.196	2.170	2.164	2.150	2.141	2.117	2.101	2.103	2.084
EPCSRST_N_0	B31	2.131	2.130	2.199	2.194	2.170	2.161	2.150	2.136	2.116	2.094	2.101	2.076
EPCSRST_N_1	B32	2.133	2.136	2.202	2.204	2.173	2.176	2.153	2.155	2.121	2.123	2.108	2.109
EPCSRST_N_2	B34	2.131	2.134	2.200	2.203	2.171	2.174	2.150	2.153	2.118	2.121	2.104	2.107
EPCSRST_N_3	B35	2.132	2.135	2.201	2.205	2.173	2.176	2.153	2.156	2.122	2.125	2.109	2.112
EPCSRST_N_4	B36	2.131	2.134	2.199	2.202	2.170	2.171	2.148	2.149	2.115	2.116	2.100	2.101
EPCSRST_N_5	B37	2.132	2.133	2.200	2.201	2.172	2.171	2.151	2.149	2.119	2.114	2.105	2.099
MONITOR	K23	2.134	2.134	2.203	2.203	2.176	2.175	2.156	2.155	2.126	2.124	2.113	2.111
PLL_MON	L20	2.135	2.134	2.207	2.205	2.181	2.178	2.158	2.159	2.127	2.131	2.128	2.119
TOGGLE_MON	L22	2.134	2.135	2.205	2.205	2.178	2.178	2.158	2.158	2.129	2.130	2.117	2.118

Table. 14. LVCMOS 25 VOH – DUT 4764

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.126	2.128	2.191	2.194	2.159	2.162	2.136	2.138	2.096	2.099	2.078	2.081
EPCSRST_N_0	B31	2.128	2.127	2.195	2.192	2.165	2.159	2.143	2.134	2.107	2.092	2.091	2.073
EPCSRST_N_1	B32	2.130	2.132	2.200	2.202	2.171	2.173	2.150	2.152	2.118	2.120	2.104	2.107
EPCSRST_N_2	B34	2.129	2.131	2.198	2.201	2.169	2.172	2.148	2.150	2.116	2.118	2.102	2.104
EPCSRST_N_3	B35	2.130	2.132	2.200	2.203	2.172	2.174	2.151	2.154	2.120	2.123	2.107	2.109
EPCSRST_N_4	B36	2.129	2.131	2.197	2.200	2.168	2.171	2.146	2.149	2.112	2.115	2.098	2.101
EPCSRST_N_5	B37	2.128	2.130	2.198	2.199	2.169	2.169	2.148	2.147	2.115	2.112	2.102	2.097
MONITOR	K23	2.131	2.130	2.202	2.201	2.174	2.172	2.154	2.152	2.124	2.121	2.111	2.108
PLL_MON	L20	2.132	2.131	2.204	2.203	2.176	2.176	2.158	2.157	2.129	2.128	2.117	2.116
TOGGLE_MON	L22	2.132	2.132	2.203	2.203	2.175	2.175	2.155	2.155	2.126	2.126	2.113	2.115

Table. 15. LVCMOS 25 VOL – DUT 4595

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	234.1	236.7	168.2	174.3	197.1	206.4	220.2	232.6	252.9	271.8	267.2	289.3
EPCSRST_N_0	B31	233.6	237.1	168.3	175.9	197.3	209.0	220.8	236.5	254.3	278.4	269.2	297.1
EPCSRST_N_1	B32	232.4	232.1	166.0	166.3	193.9	194.3	214.8	215.2	246.4	247.4	260.0	261.1
EPCSRST_N_2	B34	234.9	234.7	168.6	168.5	197.2	197.3	218.6	218.3	251.2	251.2	265.3	265.3
EPCSRST_N_3	B35	234.3	233.6	167.0	166.8	195.0	194.8	215.6	215.4	247.0	246.7	260.1	260.2
EPCSRST_N_4	B36	235.6	235.2	169.4	169.5	198.4	198.6	220.2	220.2	253.7	254.1	268.1	268.6
EPCSRST_N_5	B37	234.7	235.6	167.7	170.0	195.8	199.4	216.7	221.5	248.7	256.2	262.1	271.0
MONITOR	K23	231.5	231.2	164.2	164.6	191.2	191.8	210.8	211.8	240.7	242.3	253.0	255.0
PLL_MON	L20	230.3	229.4	160.2	162.0	187.1	188.3	206.3	207.9	235.3	235.9	243.5	247.7
TOGGLE_MON	L22	230.3	229.9	162.7	162.5	189.1	189.0	208.0	207.6	236.8	236.3	248.5	248.3

Table. 16. LVCMOS 25 VOL – DUT 4650

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	242.5	241.6	178.1	177.3	210.7	209.6	237.6	235.9	277.5	275.5	295.2	292.9
EPCSRST_N_0	B31	240.2	242.3	174.2	179.4	205.0	212.9	230.1	240.5	266.3	282.4	282.3	301.0
EPCSRST_N_1	B32	238.0	237.7	169.9	169.6	198.3	198.0	219.6	219.0	251.9	251.3	265.8	265.1
EPCSRST_N_2	B34	239.5	239.3	171.1	171.1	200.1	199.8	221.6	221.1	254.3	254.0	268.4	267.9
EPCSRST_N_3	B35	239.4	239.0	169.9	169.6	198.0	197.7	218.9	218.4	250.3	249.8	263.7	263.1
EPCSRST_N_4	B36	240.5	239.9	172.7	172.1	202.3	201.3	224.1	222.9	258.2	256.3	272.7	270.7
EPCSRST_N_5	B37	241.3	240.1	174.2	172.7	204.6	202.3	227.5	224.4	263.1	258.7	278.6	273.3
MONITOR	K23	237.8	237.6	168.0	168.7	195.2	196.1	215.1	216.6	244.6	246.9	257.0	259.8
PLL_MON	L20	236.8	236.2	166.8	166.4	193.1	193.1	212.6	213.0	240.7	241.1	251.9	252.9
TOGGLE_MON	L22	236.9	236.8	166.9	166.9	193.8	193.7	212.6	212.6	241.3	241.6	253.2	253.5

Table. 17. LVCMOS 25 VOL – DUT 4674

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	241.1	240.2	176.2	175.6	208.1	207.3	234.3	233.1	272.9	271.7	289.9	288.5
EPCSRST_N_0	B31	238.1	240.0	172.2	177.4	202.4	210.3	226.7	237.4	261.9	278.4	277.3	296.5
EPCSRST_N_1	B32	236.1	235.5	168.1	167.8	196.0	195.6	216.8	216.3	248.0	247.6	261.4	261.0
EPCSRST_N_2	B34	237.8	237.2	169.4	169.2	197.7	197.4	218.6	218.0	250.6	250.0	264.3	263.7
EPCSRST_N_3	B35	237.3	236.7	168.4	168.0	196.2	195.7	216.5	215.9	247.2	246.3	260.0	259.1
EPCSRST_N_4	B36	238.0	237.2	170.8	170.2	199.9	199.0	221.4	220.3	254.5	253.3	268.9	267.4
EPCSRST_N_5	B37	238.0	238.3	169.7	171.1	198.0	200.4	219.1	222.0	251.2	255.9	264.8	270.4
MONITOR	K23	236.0	235.6	166.7	167.2	193.9	194.8	213.7	214.8	243.3	245.3	255.6	258.1
PLL_MON	L20	234.7	233.9	165.3	165.1	192.0	191.7	211.7	211.5	239.5	239.6	251.2	251.4
TOGGLE_MON	L22	235.3	234.7	165.6	165.2	192.4	191.8	211.3	210.6	240.0	239.3	251.9	251.2

Table. 18. LVCMOS 25 VOL – DUT 4691

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	238.8	237.7	175.1	174.4	206.9	206.1	233.1	232.0	271.7	270.6	288.8	287.4
EPCSRST_N_0	B31	236.4	238.2	171.4	176.6	201.7	209.4	226.0	236.3	261.2	277.5	276.7	295.7
EPCSRST_N_1	B32	234.8	234.0	167.2	166.8	195.0	194.6	215.9	215.1	247.4	246.6	260.8	260.1
EPCSRST_N_2	B34	236.2	235.4	168.1	167.7	196.4	195.8	217.2	216.4	249.2	248.1	262.7	261.8
EPCSRST_N_3	B35	234.9	234.1	166.9	166.3	194.2	193.8	214.6	213.9	245.2	244.4	258.0	257.1
EPCSRST_N_4	B36	236.7	235.9	170.0	169.4	198.8	198.3	220.5	219.7	253.8	253.0	268.2	267.2
EPCSRST_N_5	B37	236.1	236.4	168.2	169.9	196.4	199.2	217.3	220.9	249.2	255.1	262.7	269.7
MONITOR	K23	235.4	234.7	166.5	166.8	193.6	194.2	213.7	214.5	243.3	244.9	255.8	257.8
PLL_MON	L20	234.2	233.3	165.0	164.7	191.5	191.1	211.0	211.0	239.0	239.0	250.6	250.8
TOGGLE_MON	L22	235.3	232.8	168.2	164.3	196.7	191.0	217.4	209.7	249.7	238.4	263.1	250.1

Table. 19. LVCMOS 25 VOL – DUT 4750

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	235.0	236.6	168.2	173.5	196.7	204.8	219.4	230.5	251.3	268.7	265.1	285.6
EPCSRST_N_0	B31	234.6	237.3	168.2	175.4	196.9	208.1	219.9	235.0	252.4	275.9	266.6	294.1
EPCSRST_N_1	B32	232.8	231.8	166.0	165.7	193.5	193.4	213.9	213.8	244.8	245.2	257.9	258.4
EPCSRST_N_2	B34	235.1	234.0	167.8	167.1	195.9	195.2	216.7	215.8	248.5	247.5	261.9	260.8
EPCSRST_N_3	B35	234.5	233.4	166.6	166.0	194.1	193.3	214.4	213.4	245.2	243.7	257.9	256.5
EPCSRST_N_4	B36	235.8	234.8	169.1	169.1	197.7	197.9	219.2	219.5	252.2	253.1	266.5	267.6
EPCSRST_N_5	B37	235.1	235.1	167.7	169.5	195.7	198.6	216.3	220.4	247.8	254.3	261.1	268.9
MONITOR	K23	233.2	232.1	165.2	165.1	192.3	192.4	212.0	212.4	241.6	242.5	253.9	255.3
PLL_MON	L20	232.0	230.6	163.4	162.7	191.7	189.1	215.6	209.0	239.1	236.9	248.5	248.8
TOGGLE_MON	L22	232.3	230.8	163.8	162.9	190.4	189.2	209.1	207.8	237.9	236.3	249.8	248.1

Table. 20. LVCMOS 25 VOL – DUT 4764

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	240.4	239.5	176.0	175.3	207.8	207.1	233.9	233.1	272.5	271.6	289.8	288.5
EPCSRST_N_0	B31	238.2	240.2	172.3	177.6	202.5	210.6	227.0	237.8	262.4	279.1	277.9	297.4
EPCSRST_N_1	B32	236.5	235.9	168.3	167.8	196.3	195.8	217.0	216.4	248.5	248.1	261.8	261.4
EPCSRST_N_2	B34	237.8	237.3	169.6	169.4	197.9	197.5	219.1	218.2	251.0	250.3	264.6	263.8
EPCSRST_N_3	B35	237.1	236.4	168.2	167.9	195.9	195.6	216.5	215.8	247.0	246.2	260.0	259.2
EPCSRST_N_4	B36	238.5	237.7	170.9	170.3	200.0	199.2	221.5	220.6	254.8	253.6	269.0	267.8
EPCSRST_N_5	B37	238.7	239.0	170.0	171.5	198.4	200.8	219.5	222.6	251.6	256.7	265.3	271.2
MONITOR	K23	236.2	235.7	167.1	167.4	194.3	195.0	214.2	215.3	243.9	245.7	256.3	258.5
PLL_MON	L20	234.9	234.0	165.4	165.1	191.9	191.7	211.5	211.5	239.7	239.7	251.5	251.5
TOGGLE_MON	L22	234.7	233.8	166.2	165.4	193.3	192.1	212.4	211.1	241.7	239.8	253.9	251.8

Table. 21. LVTTL VOH – DUT 4595

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.918	2.917	2.907	2.903	2.887	2.876	2.866	2.849	2.847	2.823
EPCSRST_N_0	B31	2.918	2.916	2.908	2.902	2.887	2.873	2.866	2.843	2.845	2.815
EPCSRST_N_1	B32	2.919	2.921	2.910	2.912	2.891	2.892	2.872	2.873	2.853	2.854
EPCSRST_N_2	B34	2.917	2.919	2.907	2.909	2.887	2.889	2.867	2.869	2.847	2.849
EPCSRST_N_3	B35	2.918	2.920	2.909	2.911	2.891	2.893	2.872	2.874	2.854	2.855
EPCSRST_N_4	B36	2.917	2.919	2.907	2.909	2.886	2.888	2.865	2.867	2.845	2.845
EPCSRST_N_5	B37	2.918	2.919	2.908	2.908	2.889	2.886	2.870	2.864	2.851	2.843
MONITOR	K23	2.922	2.921	2.913	2.912	2.896	2.894	2.879	2.877	2.863	2.859
PLL_MON	L20	2.925	2.922	2.916	2.915	2.901	2.900	2.886	2.884	2.871	2.869
TOGGLE_MON	L22	2.923	2.922	2.915	2.915	2.899	2.899	2.883	2.883	2.868	2.867

Table. 22. LVTTL VOH – DUT 4650

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.910	2.913	2.896	2.900	2.869	2.873	2.841	2.846	2.814	2.821
EPCSRST_N_0	B31	2.913	2.913	2.901	2.898	2.878	2.869	2.854	2.840	2.831	2.812
EPCSRST_N_1	B32	2.915	2.918	2.905	2.908	2.886	2.889	2.867	2.870	2.848	2.850
EPCSRST_N_2	B34	2.914	2.916	2.904	2.907	2.885	2.887	2.865	2.867	2.845	2.847
EPCSRST_N_3	B35	2.915	2.917	2.906	2.908	2.888	2.890	2.869	2.871	2.851	2.853
EPCSRST_N_4	B36	2.914	2.916	2.903	2.906	2.882	2.885	2.861	2.865	2.840	2.845
EPCSRST_N_5	B37	2.913	2.916	2.901	2.905	2.879	2.884	2.856	2.863	2.834	2.841
MONITOR	K23	2.918	2.917	2.909	2.908	2.892	2.890	2.876	2.873	2.859	2.855
PLL_MON	L20	2.918	2.918	2.911	2.910	2.896	2.895	2.881	2.880	2.867	2.865
TOGGLE_MON	L22	2.918	2.917	2.910	2.909	2.895	2.894	2.879	2.878	2.864	2.863

Table. 23. LVTTL VOH – DUT 4674

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.912	2.915	2.900	2.902	2.874	2.877	2.847	2.851	2.822	2.826
EPCSRST_N_0	B31	2.915	2.915	2.904	2.901	2.881	2.872	2.859	2.844	2.837	2.817
EPCSRST_N_1	B32	2.917	2.920	2.908	2.911	2.890	2.892	2.871	2.874	2.853	2.855
EPCSRST_N_2	B34	2.916	2.918	2.906	2.909	2.888	2.890	2.868	2.871	2.849	2.852
EPCSRST_N_3	B35	2.917	2.919	2.908	2.911	2.890	2.893	2.873	2.876	2.855	2.858
EPCSRST_N_4	B36	2.916	2.919	2.906	2.908	2.885	2.888	2.865	2.868	2.845	2.848
EPCSRST_N_5	B37	2.916	2.918	2.906	2.907	2.887	2.887	2.868	2.866	2.849	2.845
MONITOR	K23	2.919	2.918	2.911	2.910	2.894	2.892	2.877	2.875	2.861	2.857
PLL_MON	L20	2.919	2.920	2.912	2.912	2.897	2.896	2.882	2.882	2.868	2.867
TOGGLE_MON	L22	2.919	2.919	2.912	2.912	2.896	2.896	2.881	2.881	2.865	2.865

Table. 24. LVTTL VOH – DUT 4691

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.915	2.917	2.901	2.904	2.875	2.878	2.849	2.852	2.824	2.827
EPCSRST_N_0	B31	2.917	2.916	2.905	2.902	2.882	2.874	2.860	2.845	2.838	2.818
EPCSRST_N_1	B32	2.919	2.921	2.909	2.912	2.891	2.893	2.872	2.875	2.854	2.856
EPCSRST_N_2	B34	2.918	2.920	2.909	2.911	2.890	2.892	2.870	2.873	2.851	2.854
EPCSRST_N_3	B35	2.919	2.922	2.910	2.913	2.893	2.896	2.875	2.878	2.858	2.860
EPCSRST_N_4	B36	2.917	2.920	2.907	2.910	2.887	2.890	2.866	2.869	2.846	2.848
EPCSRST_N_5	B37	2.918	2.920	2.909	2.910	2.890	2.888	2.871	2.867	2.852	2.846
MONITOR	K23	2.919	2.919	2.911	2.910	2.894	2.893	2.877	2.875	2.861	2.858
PLL_MON	L20	2.920	2.920	2.913	2.912	2.898	2.897	2.883	2.882	2.868	2.867
TOGGLE_MON	L22	2.919	2.920	2.909	2.913	2.890	2.897	2.871	2.881	2.852	2.866

Table. 25. LVTTL VOH – DUT 4750

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.918	2.917	2.908	2.904	2.888	2.878	2.869	2.852	2.850	2.827
EPCSRST_N_0	B31	2.918	2.916	2.908	2.903	2.888	2.874	2.868	2.846	2.848	2.819
EPCSRST_N_1	B32	2.919	2.922	2.910	2.913	2.892	2.894	2.874	2.876	2.856	2.857
EPCSRST_N_2	B34	2.918	2.921	2.908	2.911	2.889	2.892	2.870	2.873	2.851	2.855
EPCSRST_N_3	B35	2.919	2.922	2.910	2.913	2.893	2.895	2.875	2.878	2.857	2.860
EPCSRST_N_4	B36	2.917	2.920	2.907	2.910	2.887	2.889	2.867	2.868	2.847	2.847
EPCSRST_N_5	B37	2.918	2.920	2.909	2.909	2.890	2.888	2.871	2.867	2.853	2.846
MONITOR	K23	2.921	2.921	2.912	2.912	2.895	2.894	2.879	2.877	2.862	2.860
PLL_MON	L20	2.922	2.922	2.914	2.914	2.902	2.899	2.884	2.883	2.869	2.868
TOGGLE_MON	L22	2.921	2.922	2.914	2.914	2.898	2.899	2.883	2.883	2.867	2.867

Table. 26. LVTTL VOH – DUT 4764

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	2.913	2.916	2.900	2.903	2.874	2.877	2.848	2.851	2.823	2.826
EPCSRST_N_0	B31	2.915	2.915	2.904	2.901	2.881	2.872	2.858	2.844	2.836	2.816
EPCSRST_N_1	B32	2.917	2.920	2.908	2.910	2.889	2.892	2.871	2.873	2.852	2.855
EPCSRST_N_2	B34	2.916	2.918	2.906	2.909	2.887	2.890	2.868	2.871	2.849	2.852
EPCSRST_N_3	B35	2.917	2.920	2.908	2.911	2.891	2.893	2.873	2.876	2.855	2.858
EPCSRST_N_4	B36	2.916	2.919	2.906	2.908	2.885	2.888	2.865	2.868	2.845	2.848
EPCSRST_N_5	B37	2.915	2.917	2.906	2.907	2.887	2.886	2.868	2.865	2.849	2.844
MONITOR	K23	2.919	2.918	2.910	2.909	2.893	2.892	2.877	2.874	2.860	2.857
PLL_MON	L20	2.920	2.919	2.912	2.912	2.897	2.896	2.882	2.881	2.867	2.866
TOGGLE_MON	L22	2.920	2.920	2.911	2.912	2.895	2.896	2.879	2.880	2.863	2.864

Table. 27. LVTTL VOL – DUT 4595

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	214.7	217.3	228.1	234.3	244.6	256.9	264.8	283.4	286.6	311.9
EPCSRST_N_0	B31	214.3	217.7	227.8	235.6	245.2	260.8	266.2	289.9	288.9	320.9
EPCSRST_N_1	B32	213.1	212.6	222.6	222.2	240.5	241.0	259.2	260.2	278.7	280.1
EPCSRST_N_2	B34	215.4	215.2	225.7	225.5	244.8	244.8	264.6	264.4	284.7	284.7
EPCSRST_N_3	B35	214.8	214.2	224.1	223.3	241.8	241.2	260.2	260.1	278.9	278.9
EPCSRST_N_4	B36	216.1	215.5	226.7	226.1	246.5	246.4	266.9	267.2	287.8	288.6
EPCSRST_N_5	B37	215.3	216.0	225.0	226.8	243.0	247.8	261.9	269.3	281.1	291.2
MONITOR	K23	211.6	211.5	220.7	220.5	236.6	237.3	253.3	254.8	270.7	273.0
PLL_MON	L20	209.8	210.0	211.5	218.7	232.4	232.7	247.7	247.9	260.2	264.5
TOGGLE_MON	L22	211.0	210.4	218.6	217.9	234.0	233.6	249.7	249.5	265.8	265.4

Table. 28. LVTTL VOL – DUT 4650

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	222.5	221.7	239.8	238.2	263.5	260.7	291.1	287.3	320.5	315.3
EPCSRST_N_0	B31	219.9	222.2	235.2	240.1	254.6	265.3	278.3	294.1	303.5	324.8
EPCSRST_N_1	B32	218.1	217.6	227.9	227.0	246.0	245.1	265.1	264.2	284.8	283.7
EPCSRST_N_2	B34	219.1	218.8	229.3	228.6	248.0	247.5	267.5	267.0	287.7	287.1
EPCSRST_N_3	B35	219.3	218.7	227.8	227.1	245.6	244.8	263.6	262.9	282.2	281.7
EPCSRST_N_4	B36	220.4	219.6	230.9	229.8	250.8	249.3	271.5	269.5	292.5	290.3
EPCSRST_N_5	B37	221.1	219.8	232.4	230.0	254.1	250.8	276.5	271.7	299.2	293.2
MONITOR	K23	217.0	217.1	226.0	225.9	241.1	242.4	257.5	259.5	274.6	277.6
PLL_MON	L20	216.0	215.8	224.4	224.9	238.2	238.2	253.1	253.3	268.1	269.5
TOGGLE_MON	L22	216.7	216.4	224.4	223.9	239.4	239.2	254.6	254.6	270.2	270.4

Table. 29. LVTTL VOL – DUT 4674

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	221.3	220.3	237.4	236.3	259.3	257.9	285.3	283.5	313.0	310.7
EPCSRST_N_0	B31	218.5	220.4	233.2	237.9	251.5	262.3	273.7	290.2	298.1	320.1
EPCSRST_N_1	B32	216.7	215.7	225.7	224.5	243.0	242.2	261.3	260.8	280.1	279.6
EPCSRST_N_2	B34	217.9	217.4	227.5	226.6	245.3	244.6	264.0	263.2	283.3	282.6
EPCSRST_N_3	B35	217.5	216.9	226.1	225.2	243.0	242.2	260.4	259.6	278.3	277.4
EPCSRST_N_4	B36	218.2	217.3	228.7	227.4	248.1	246.8	267.9	266.5	288.5	286.9
EPCSRST_N_5	B37	218.3	218.5	227.7	228.3	245.7	248.4	264.8	269.1	284.0	290.1
MONITOR	K23	215.8	215.5	224.6	224.2	239.8	240.9	256.1	258.2	273.3	276.3
PLL_MON	L20	214.7	214.1	223.5	223.3	237.2	236.9	252.2	252.3	268.4	268.4
TOGGLE_MON	L22	215.5	214.6	222.7	222.1	238.0	237.3	253.2	252.7	269.1	268.3

Table. 30. LVTTL VOL – DUT 4691

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	218.3	217.3	235.1	234.0	256.8	256.1	283.1	281.9	310.8	309.2
EPCSRST_N_0	B31	216.2	218.1	231.3	235.9	250.1	260.3	272.6	288.7	296.8	318.6
EPCSRST_N_1	B32	214.7	213.9	224.1	222.8	241.4	240.7	259.9	259.3	278.8	278.1
EPCSRST_N_2	B34	215.6	214.8	224.9	223.9	242.7	241.9	261.8	260.7	280.9	279.9
EPCSRST_N_3	B35	214.4	213.7	223.3	222.5	239.9	239.1	257.5	256.6	275.5	274.6
EPCSRST_N_4	B36	216.3	215.5	226.7	225.7	246.3	245.4	266.4	265.3	287.2	286.2
EPCSRST_N_5	B37	215.7	215.7	225.1	225.8	242.7	246.5	261.8	267.6	280.9	288.8
MONITOR	K23	214.8	214.6	223.6	223.0	239.2	240.0	255.7	257.4	273.0	275.3
PLL_MON	L20	213.6	213.0	222.4	222.3	236.1	235.9	251.3	250.9	267.1	267.3
TOGGLE_MON	L22	215.1	212.7	224.7	220.1	243.6	235.9	262.6	251.3	281.7	266.8

Table. 31. LVTTL VOL – DUT 4750

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	215.1	217.3	228.6	233.5	243.9	255.2	263.0	280.9	284.0	308.1
EPCSRST_N_0	B31	215.0	217.9	228.4	235.2	244.1	259.3	264.2	287.6	285.8	317.4
EPCSRST_N_1	B32	213.4	212.4	222.7	221.7	239.8	239.6	257.7	258.1	276.1	276.9
EPCSRST_N_2	B34	215.5	214.4	224.9	223.7	243.0	241.9	261.6	260.6	280.7	279.7
EPCSRST_N_3	B35	214.9	213.7	223.9	222.6	240.4	239.4	258.1	256.7	276.1	274.6
EPCSRST_N_4	B36	216.1	215.2	226.3	225.7	245.3	245.3	265.3	266.1	285.8	287.4
EPCSRST_N_5	B37	215.5	215.6	224.7	225.9	242.5	246.3	261.0	267.3	279.7	288.6
MONITOR	K23	213.2	212.5	221.5	221.0	237.5	238.0	254.5	255.2	271.4	273.1
PLL_MON	L20	211.0	210.9	224.1	220.3	232.1	233.9	245.6	249.2	264.6	265.5
TOGGLE_MON	L22	212.6	211.2	219.8	218.5	235.7	234.0	251.0	249.6	266.9	265.1

Table. 32. LVTTL VOL – DUT 4764

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad
TID_BUF_OUT	A33	219.9	219.1	236.4	235.6	258.2	257.1	284.0	283.0	311.6	310.3
EPCSRST_N_0	B31	218.0	220.1	232.8	237.5	251.2	262.0	273.7	290.3	298.1	320.4
EPCSRST_N_1	B32	216.3	215.6	225.4	224.4	242.6	242.2	261.2	260.7	280.0	279.6
EPCSRST_N_2	B34	217.5	216.7	226.9	226.3	245.0	244.2	263.7	263.1	283.1	282.3
EPCSRST_N_3	B35	216.4	215.6	225.4	224.4	242.2	241.4	259.7	258.8	277.5	276.7
EPCSRST_N_4	B36	217.9	217.1	228.1	226.8	247.5	246.4	267.4	266.4	288.1	286.7
EPCSRST_N_5	B37	218.2	218.3	227.3	228.2	245.6	248.6	264.7	269.3	283.8	290.7
MONITOR	K23	215.8	215.2	224.5	224.2	239.7	240.8	256.3	258.3	273.6	276.1
PLL_MON	L20	214.2	213.6	223.1	222.8	236.8	236.6	251.6	251.6	268.0	268.1
TOGGLE_MON	L22	214.4	213.7	222.8	221.7	238.8	237.3	254.7	252.9	270.9	268.6

E. Propagation Delay

Table 33 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 33. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
4595	125 krad	0.473	0.477	0.78 %
4650	125 krad	0.523	0.525	0.25 %
4674	125 krad	0.505	0.503	-0.27 %
4691	125 krad	0.505	0.508	0.52 %
4750	125 krad	0.482	0.481	-0.29 %
4764	125 krad	0.512	0.513	0.35 %

F. Transition Time

The figures below show the pre-irradiation and post-annealing transitions edges. In each case the radiation induced transition degradation is not observable.

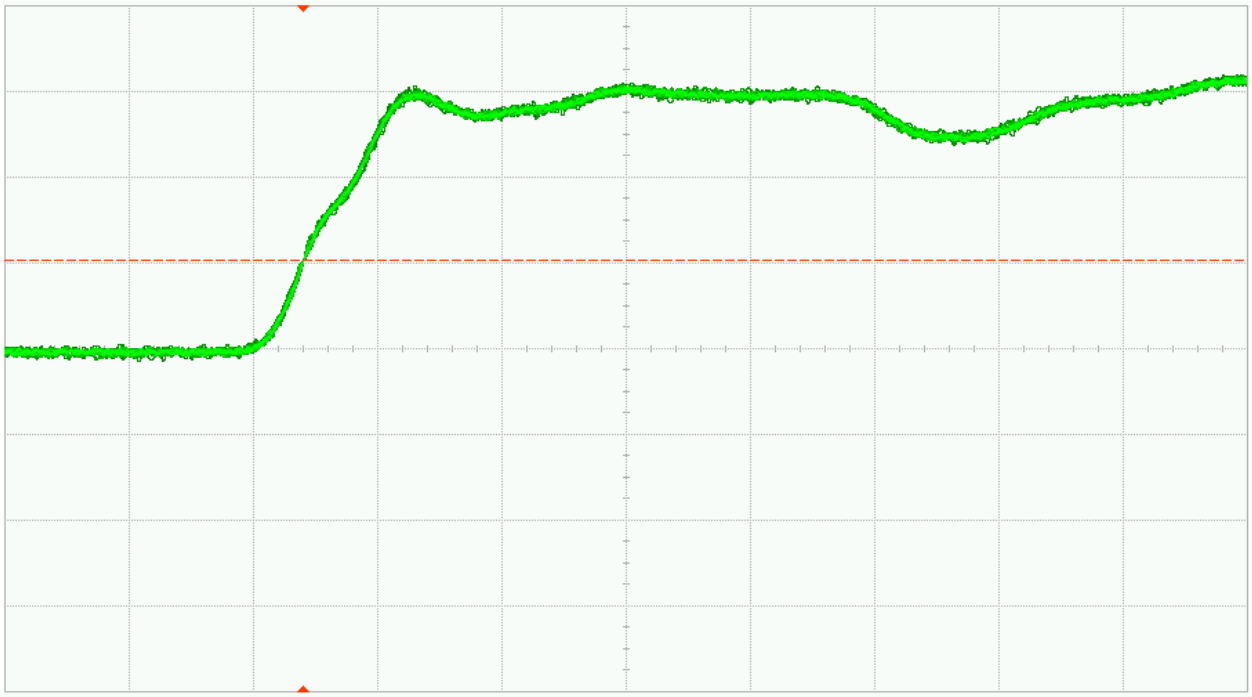

Fig. 26 (a). DUT 4595 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

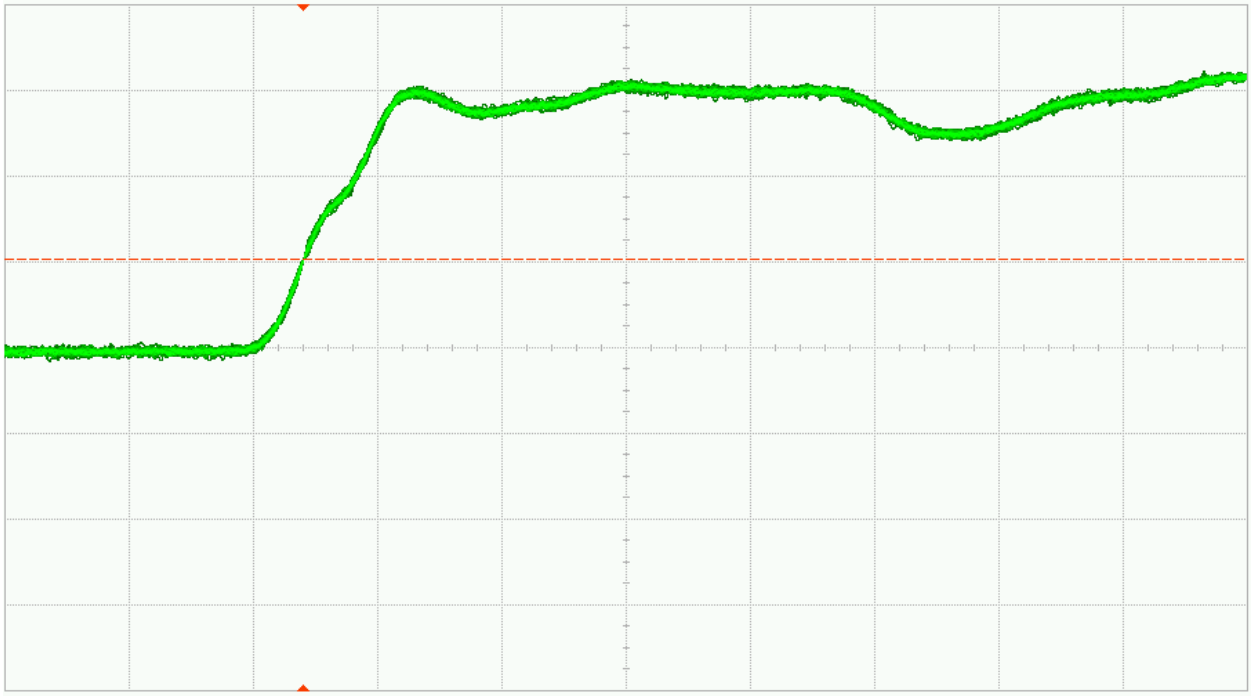

Fig. 26 (b). DUT 4595 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

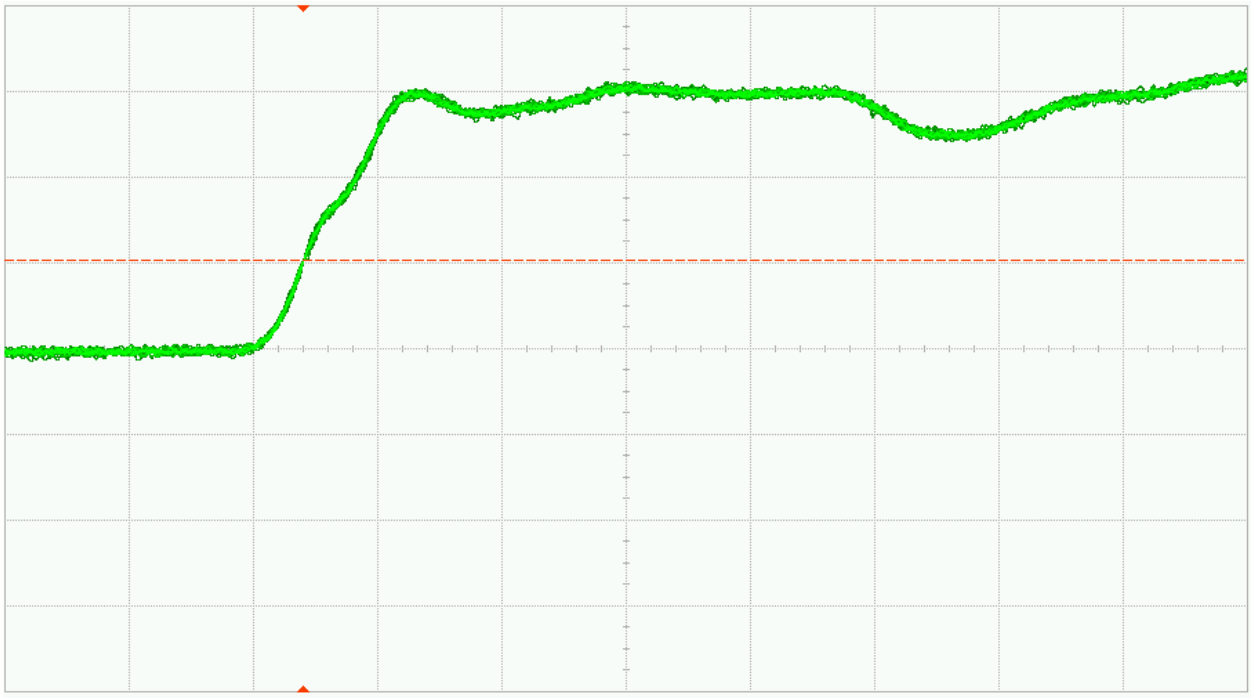

Fig. 27 (a). DUT 4650 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

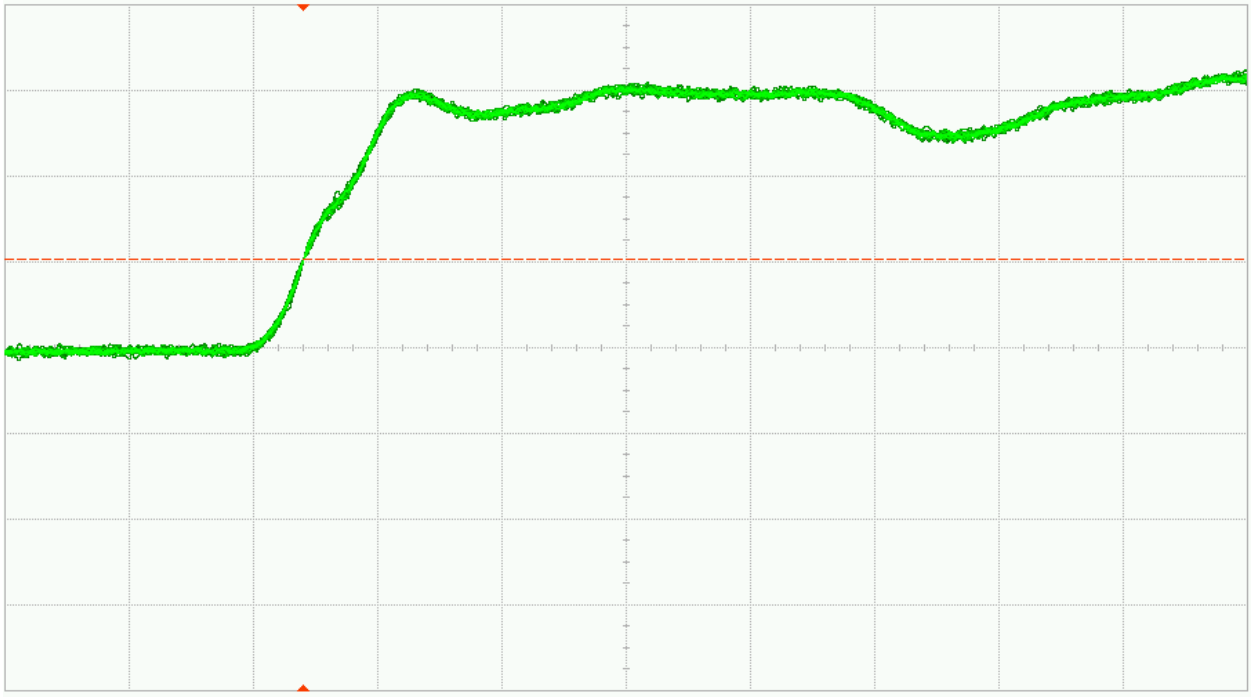

Fig. 27 (b). DUT 4650 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

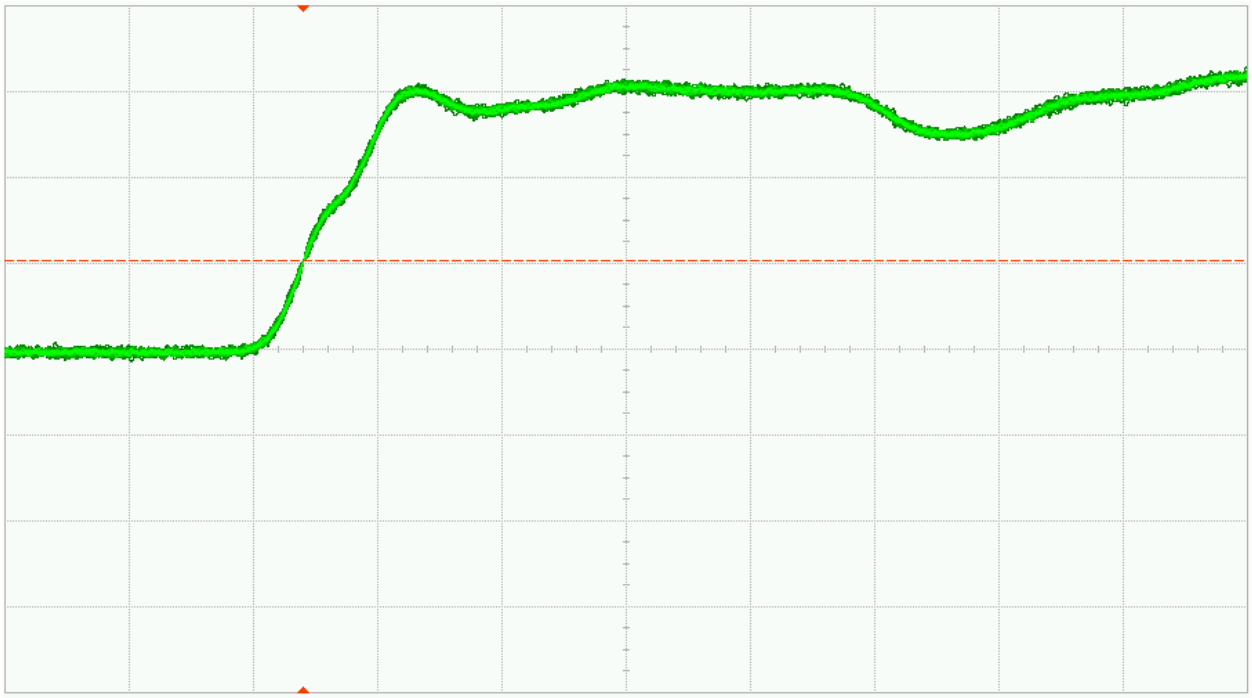

Fig. 28 (a). DUT 4674 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

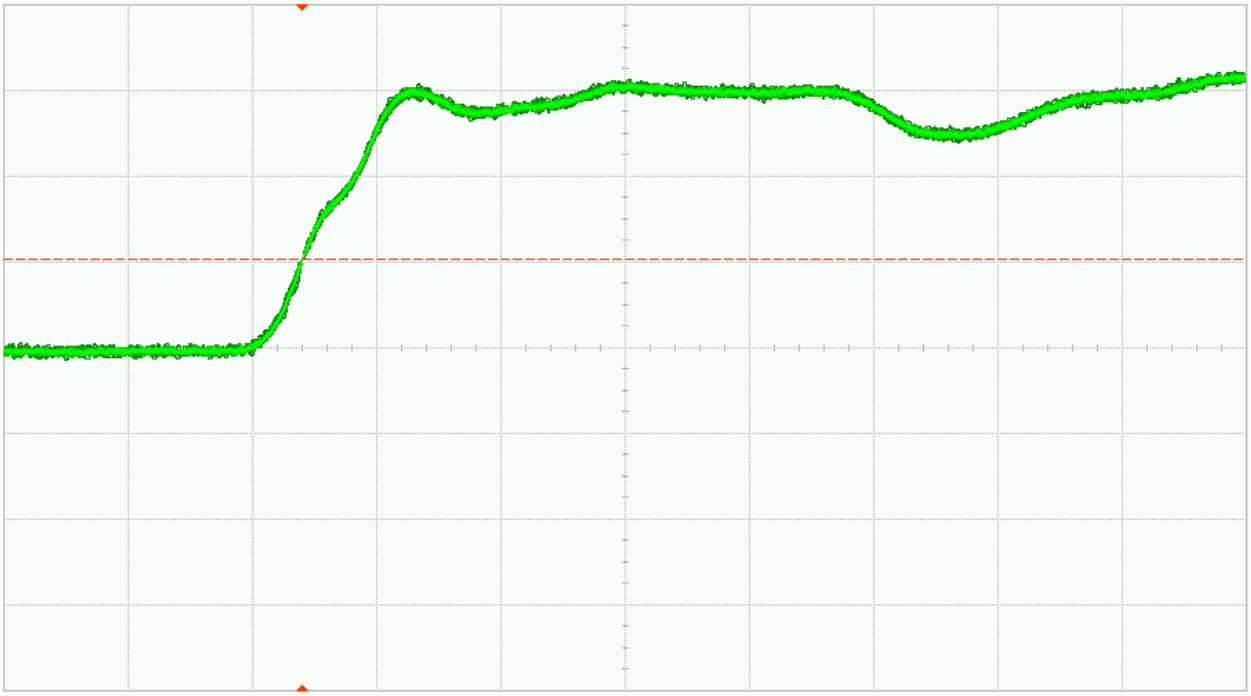

Fig. 28 (b). DUT 4674 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

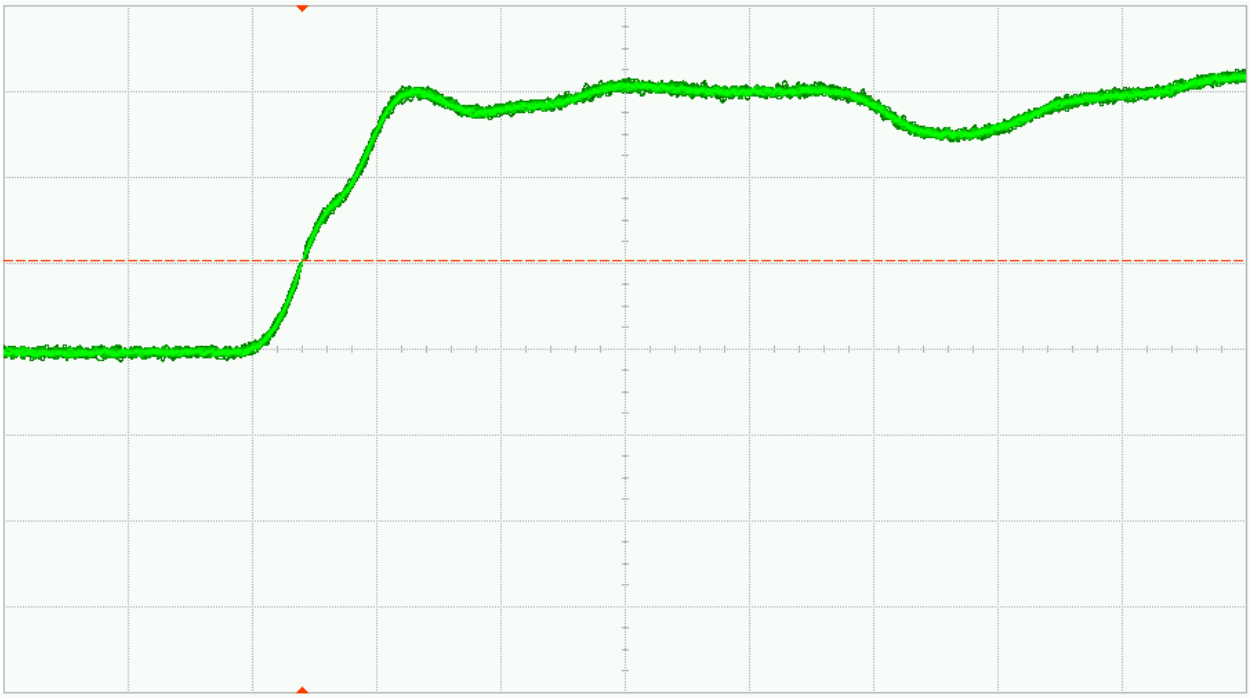

Fig. 29 (a). DUT 4691 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

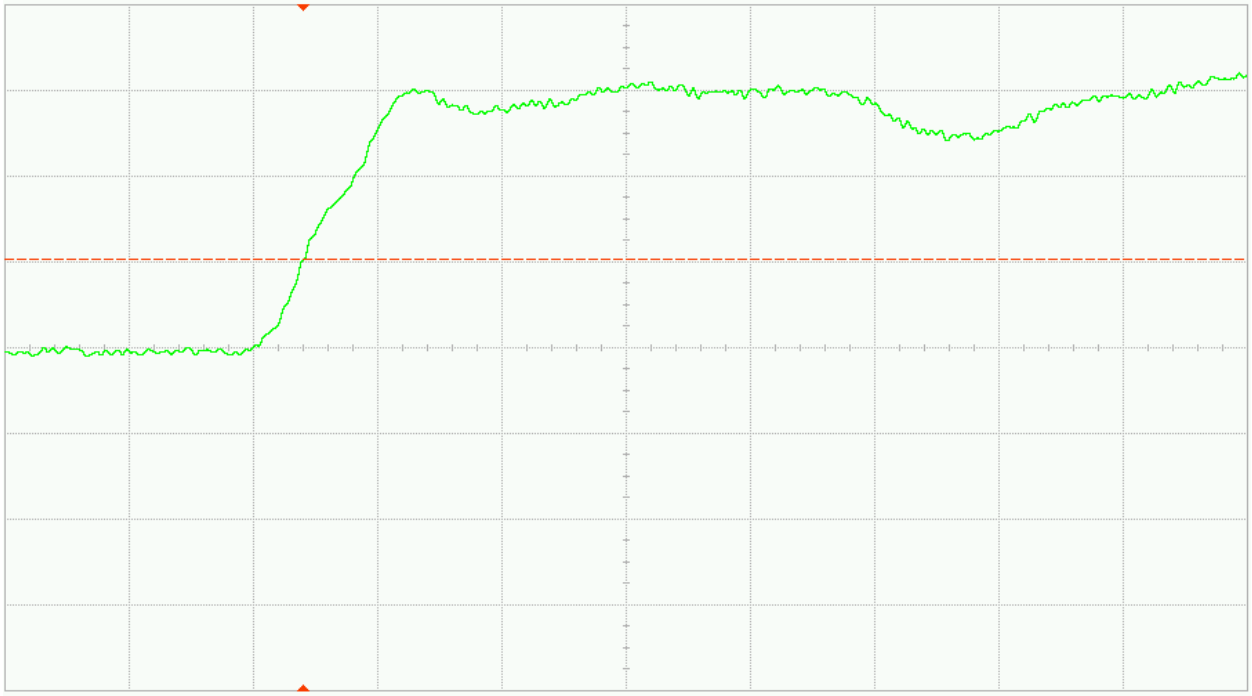

Fig. 29 (b). DUT 4691 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

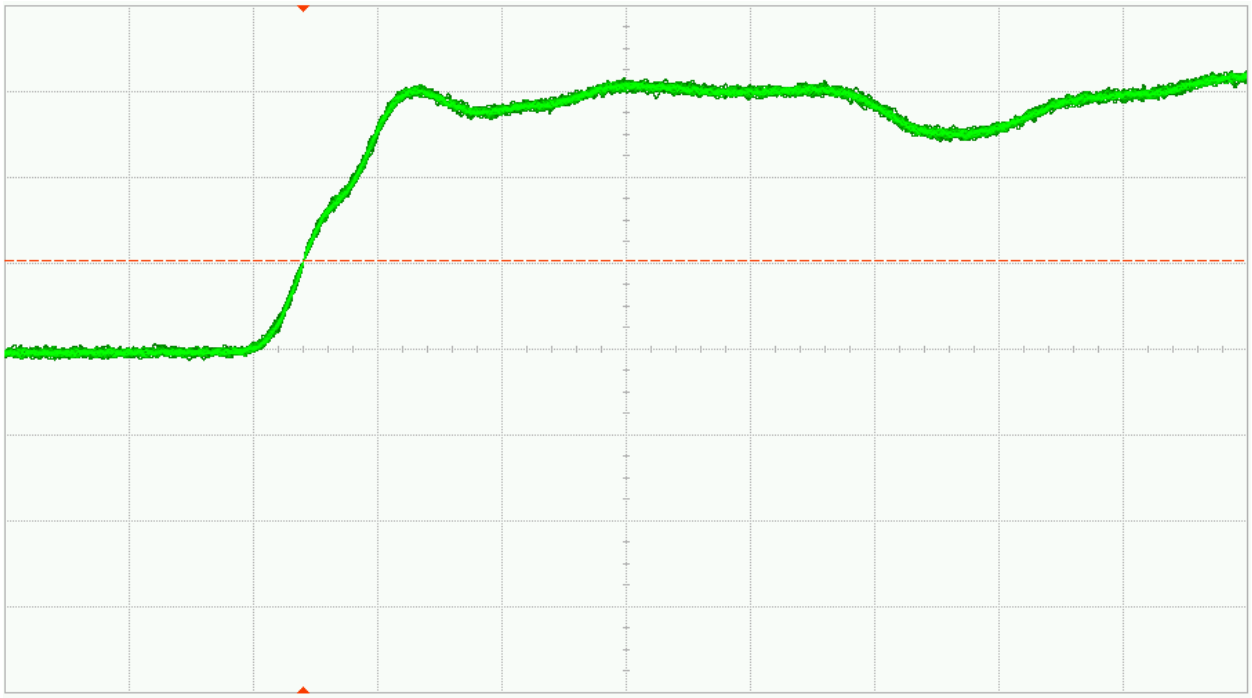

Fig. 30 (a). DUT 4750 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

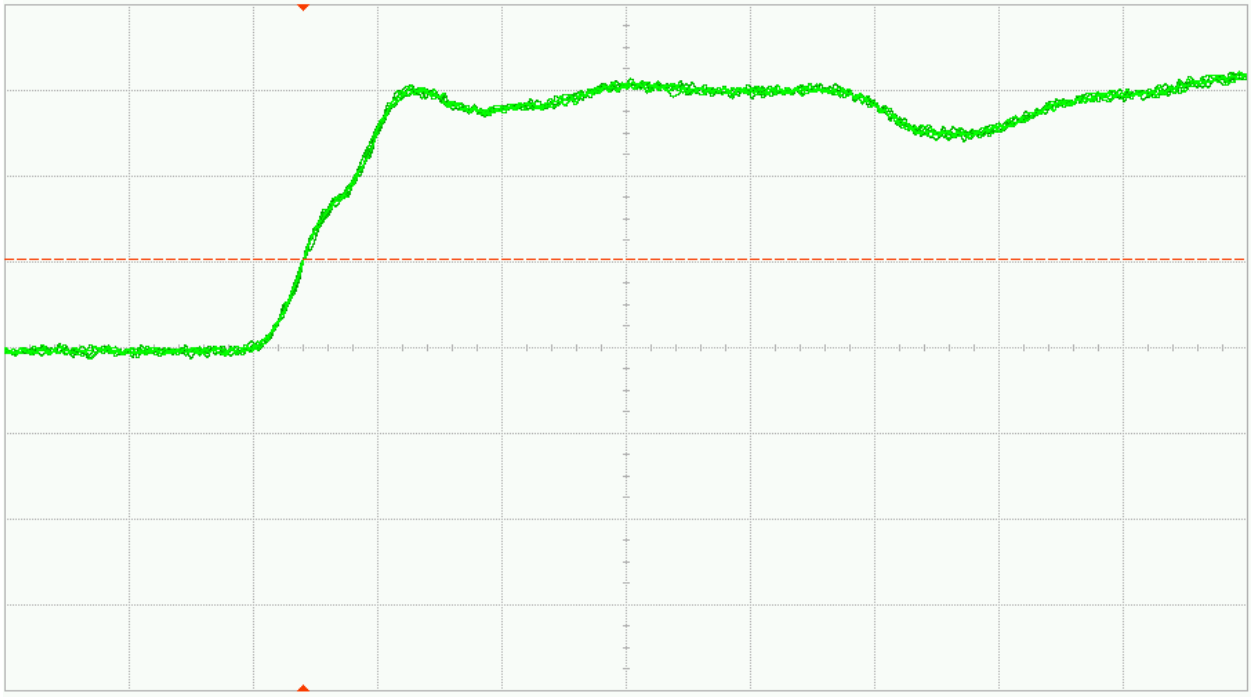

Fig. 30 (b). DUT 4750 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

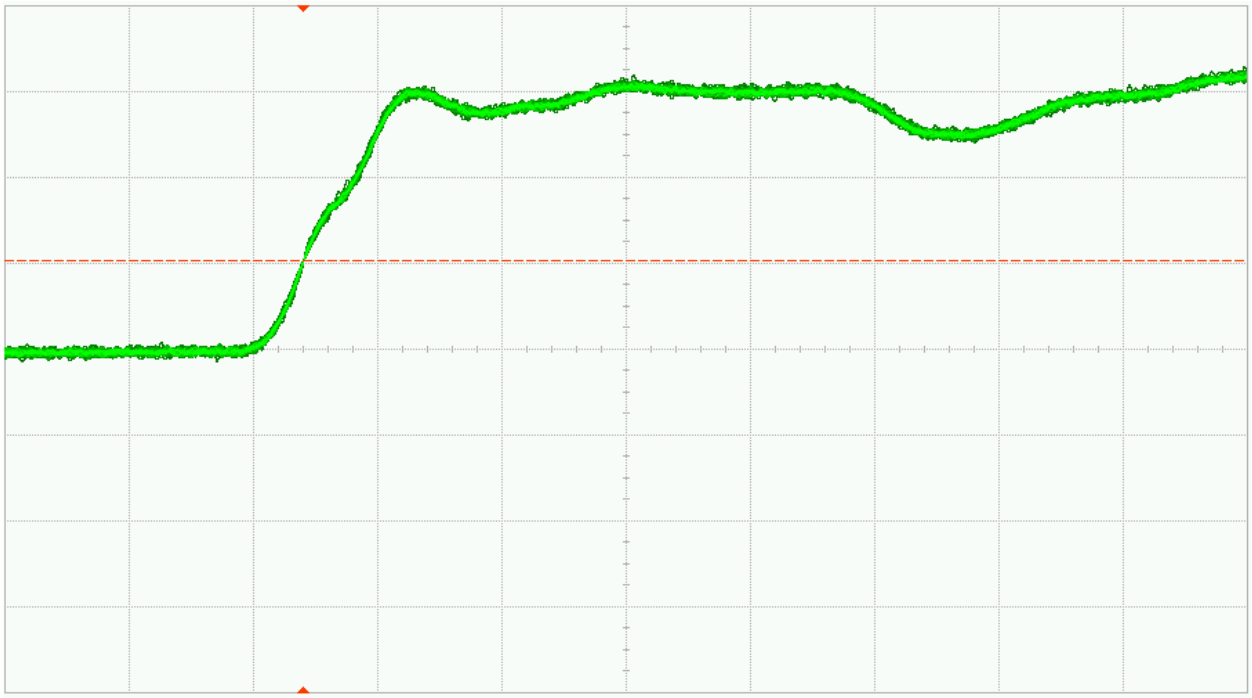

Fig. 31 (a). DUT 4764 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

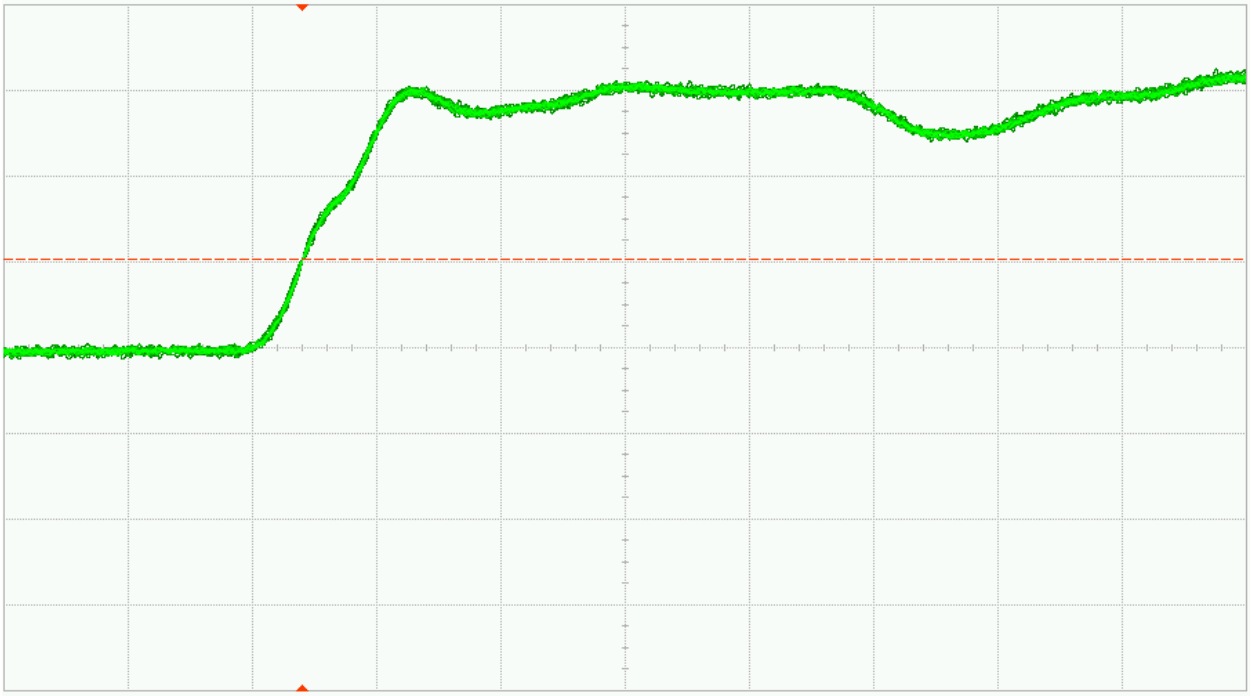

Fig. 31 (b). DUT 4764 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

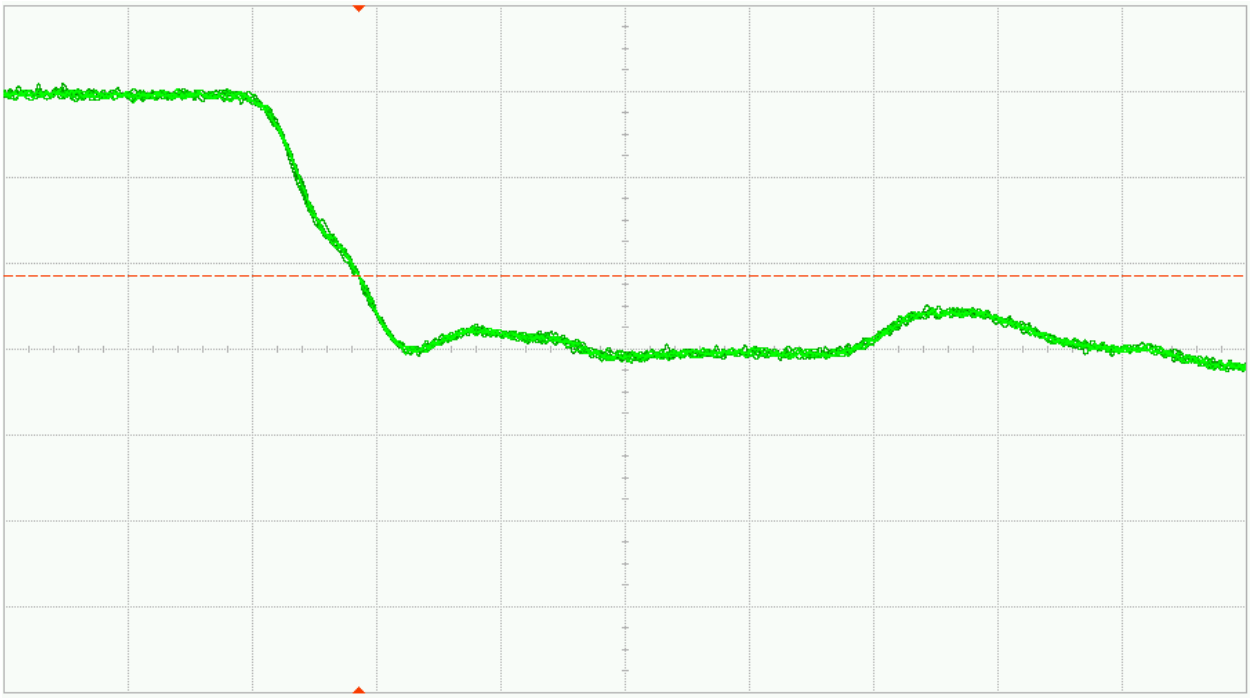

Fig. 32 (a). DUT 4595 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

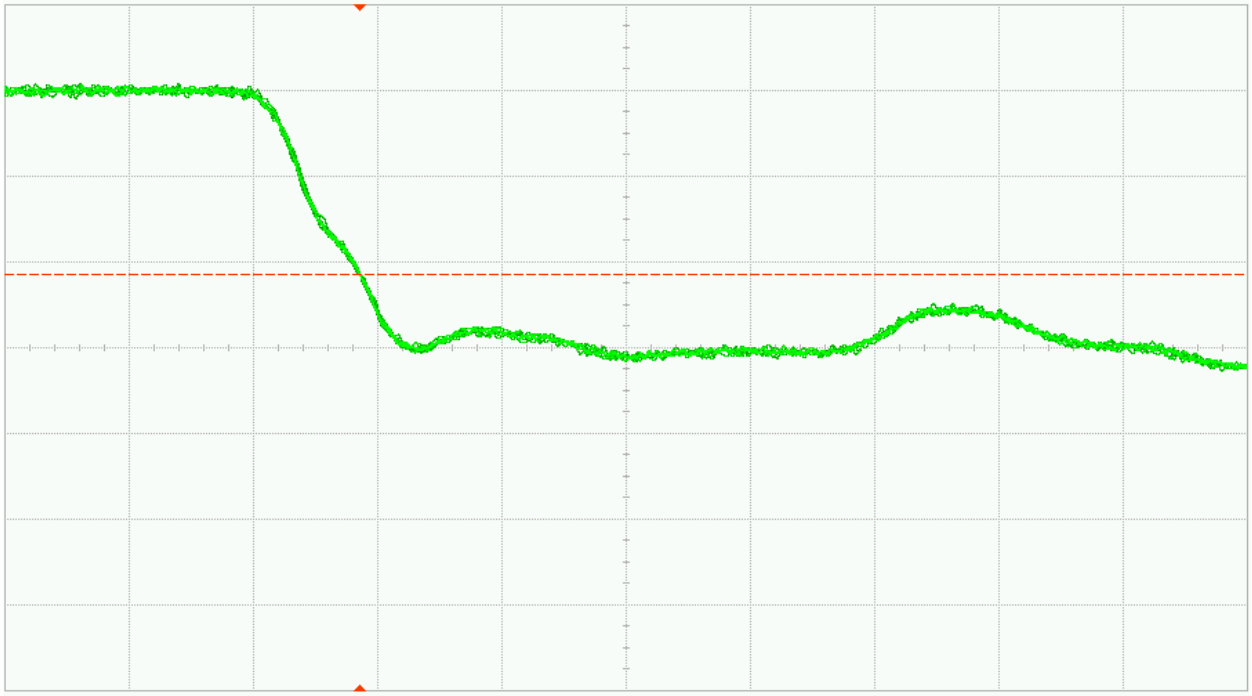

Fig. 32 (b). DUT 4595 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

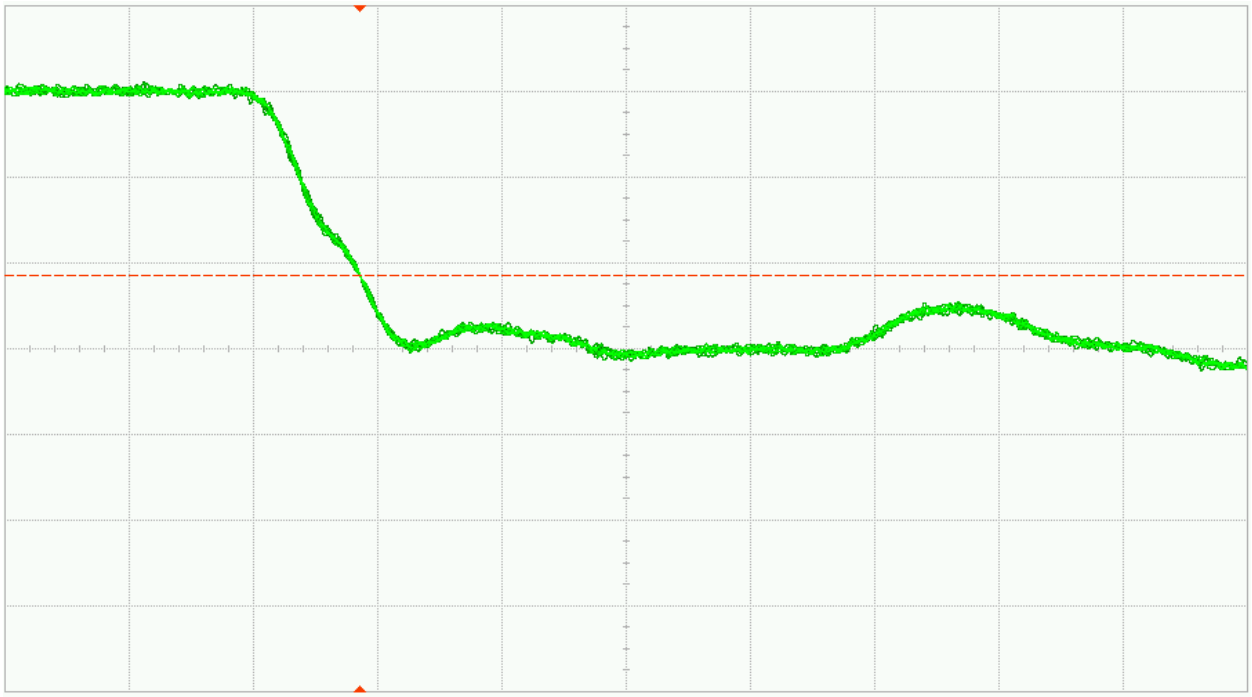

Fig. 33 (a). DUT 4650 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

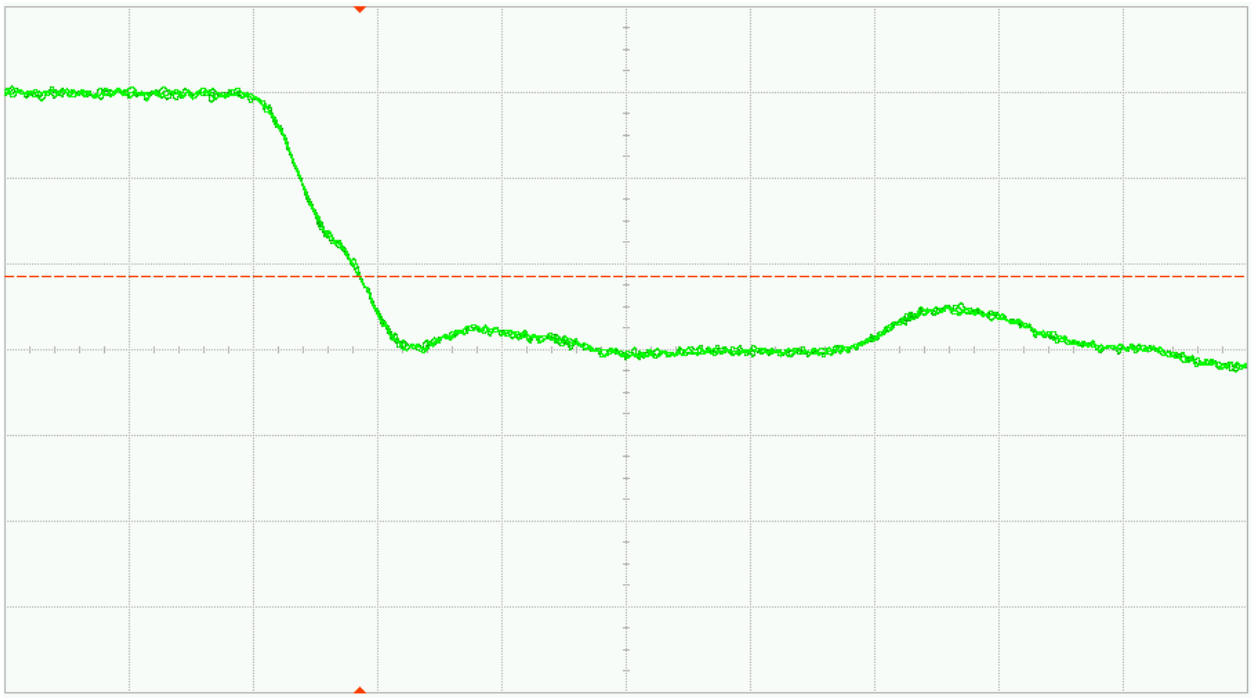

Fig. 33 (b). DUT 4650 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

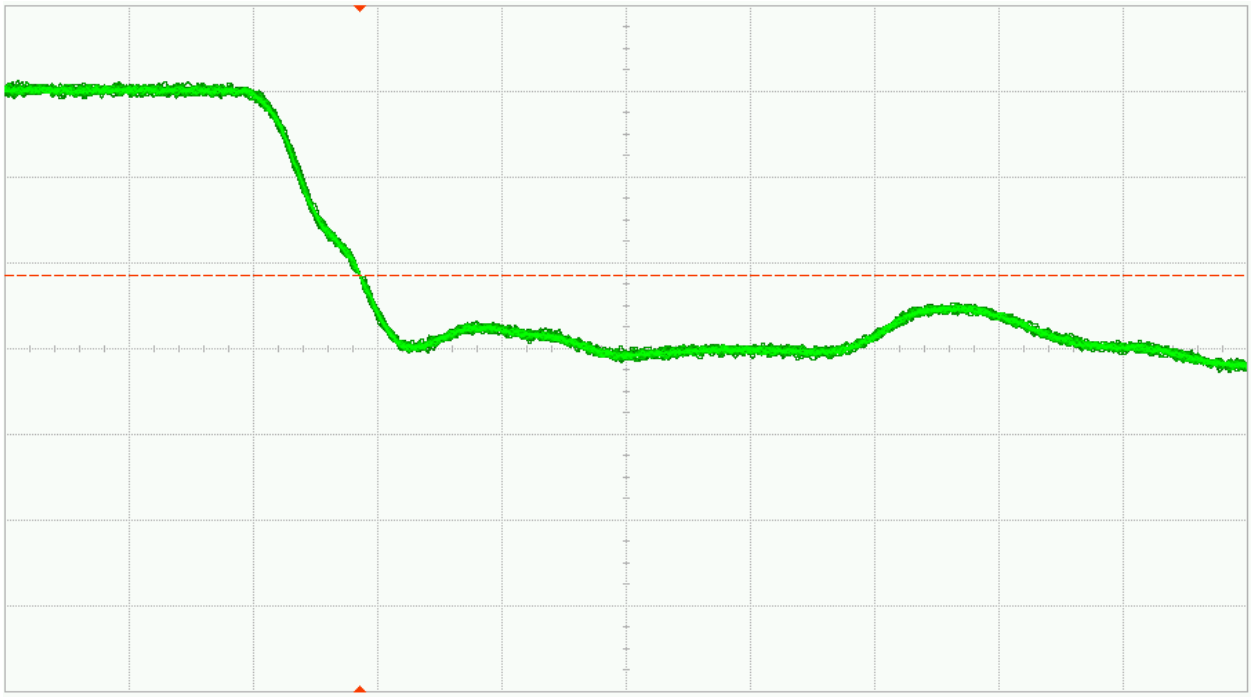

Fig. 34 (a). DUT 4674 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

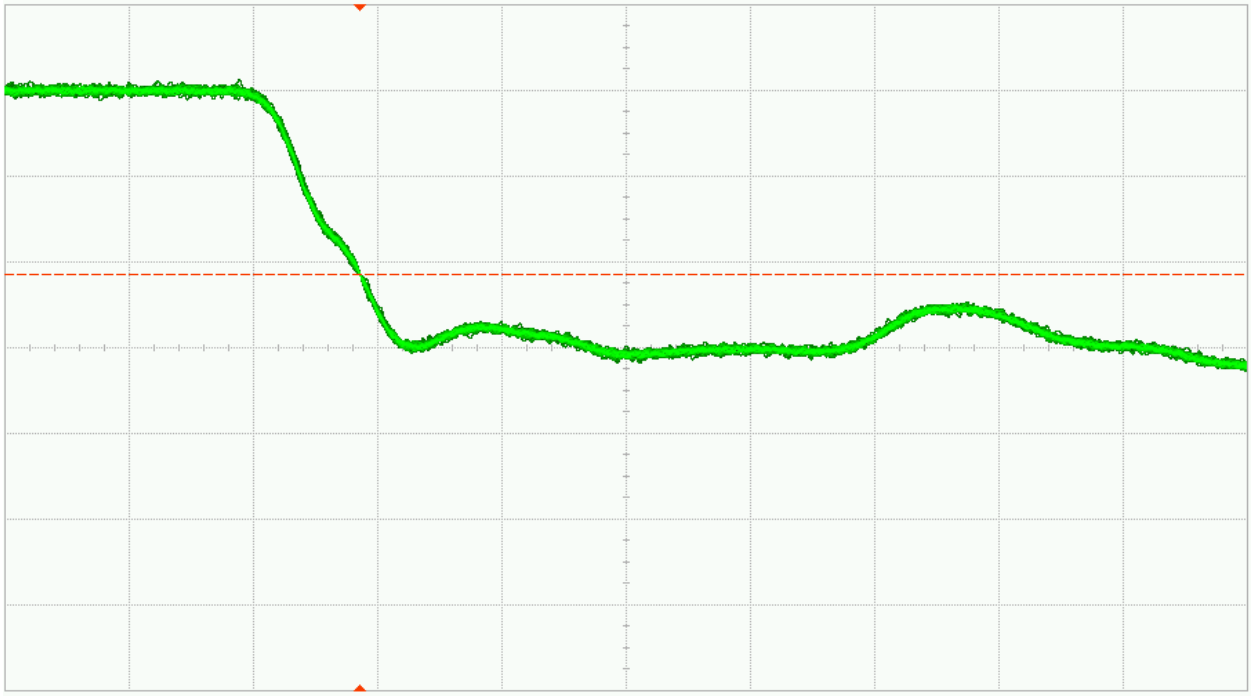

Fig. 34 (b). DUT 4674 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

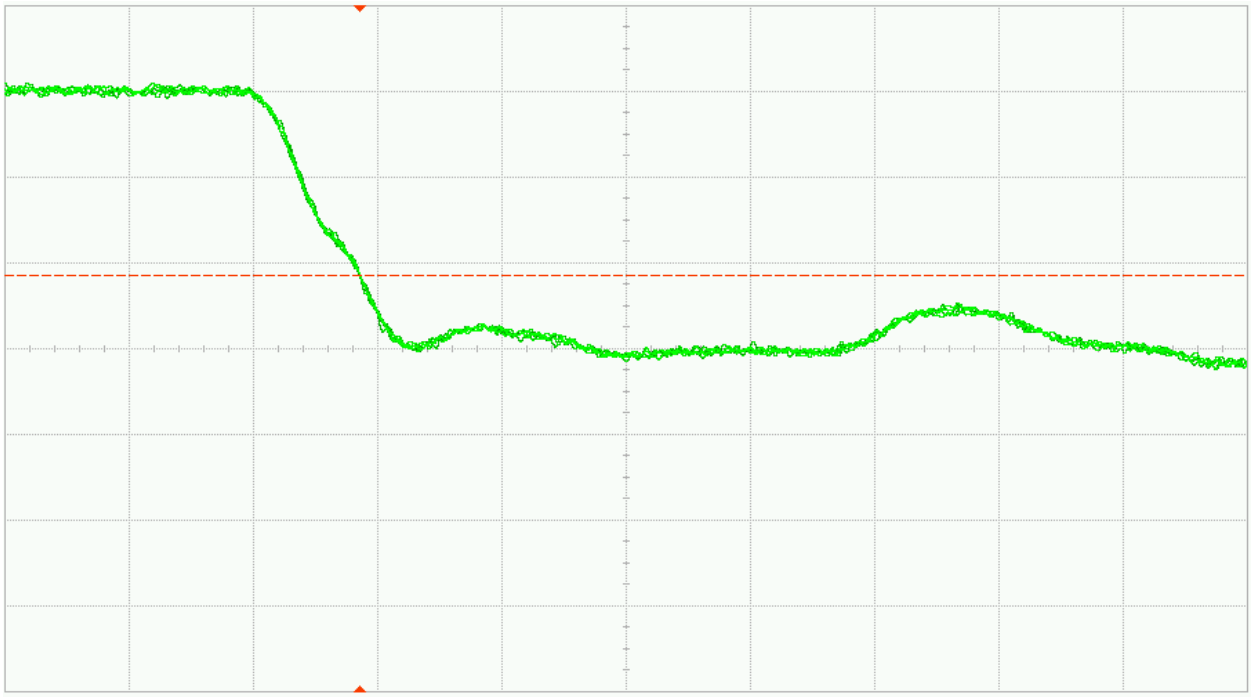

Fig. 35 (a). DUT 4691 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

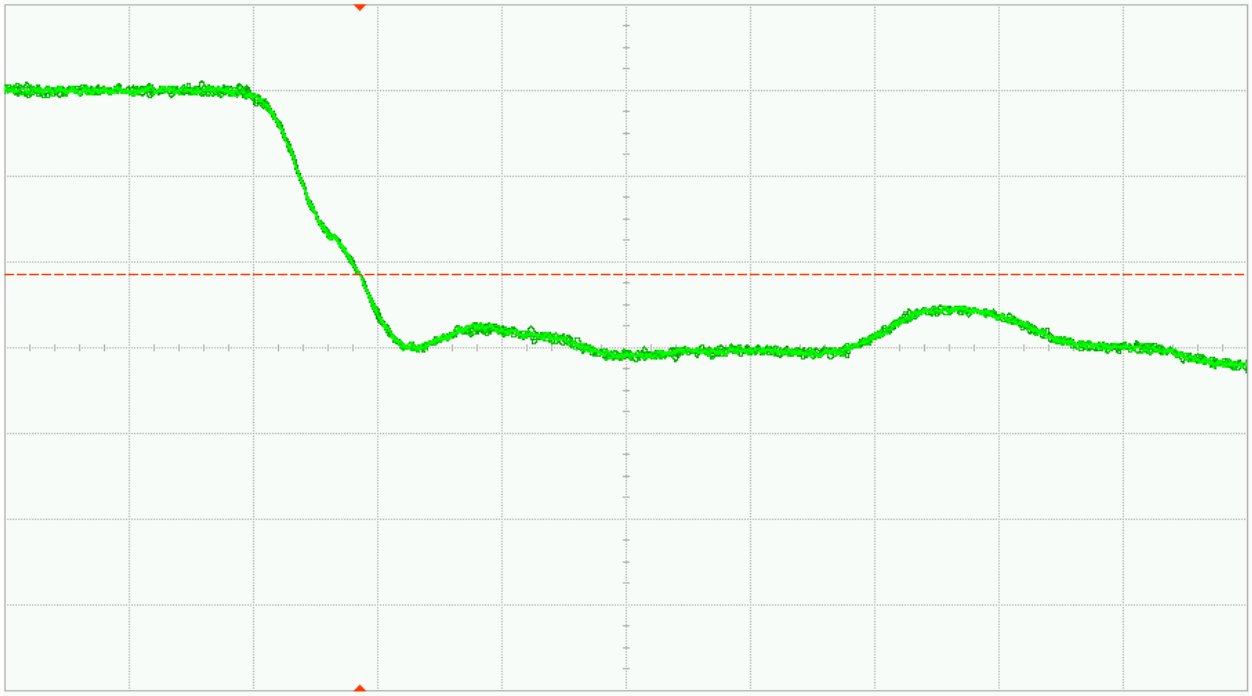

Fig. 35 (b). DUT 4691 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

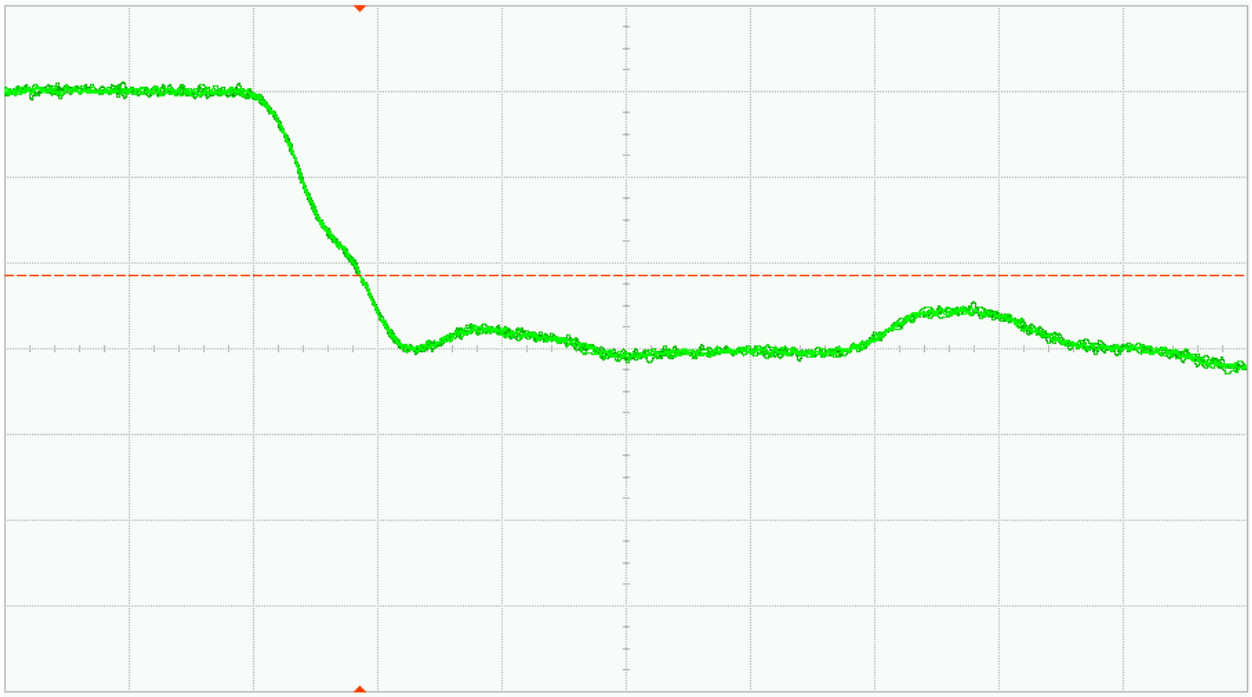

Fig. 36 (a). DUT 4750 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

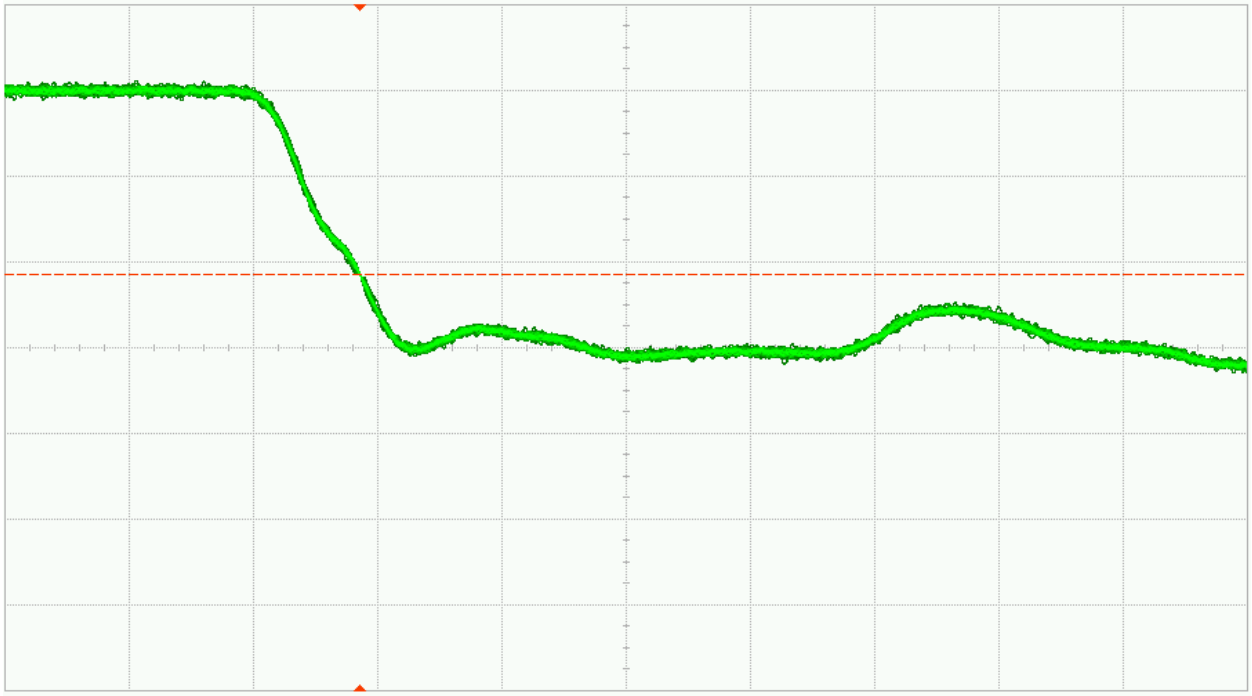

Fig. 36 (b). DUT 4750 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

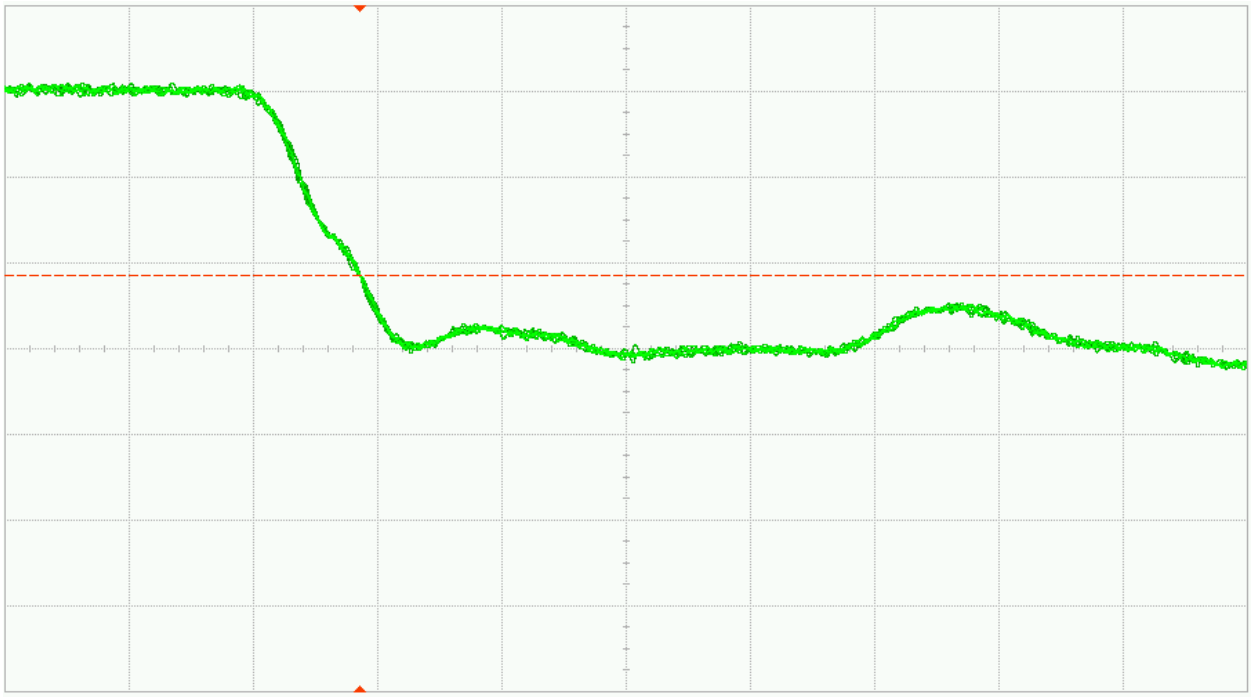

Fig. 37 (a). DUT 4764 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

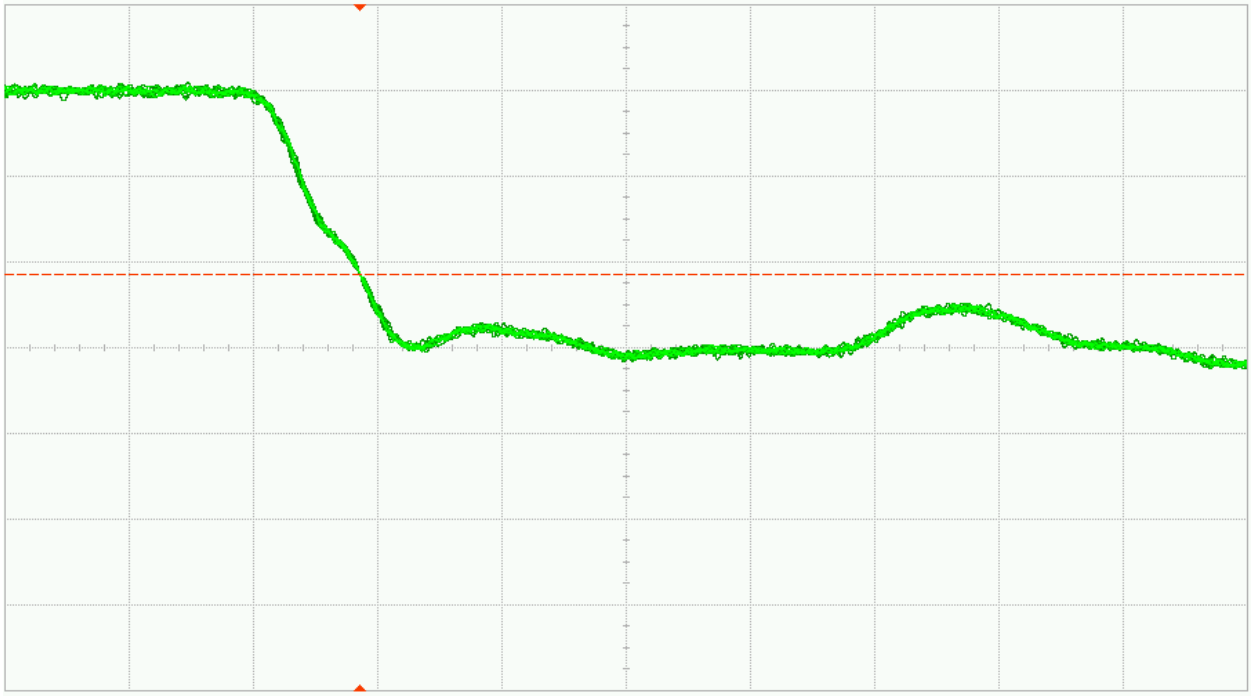

Fig. 37 (b). DUT 4764 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 34. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

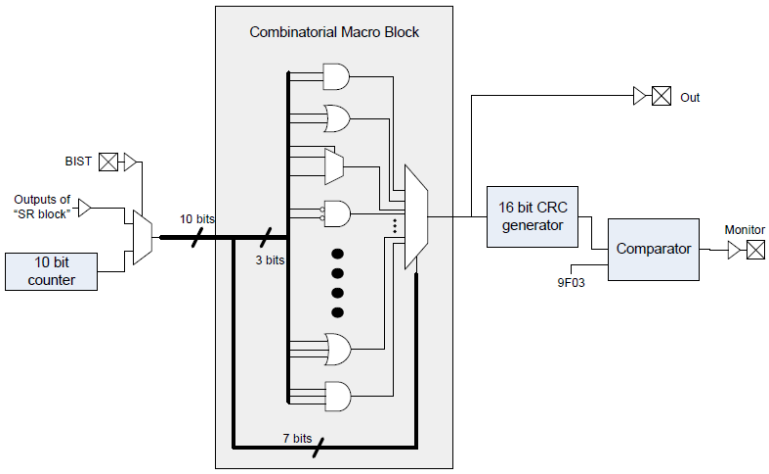

Fig. 38. Combo Block

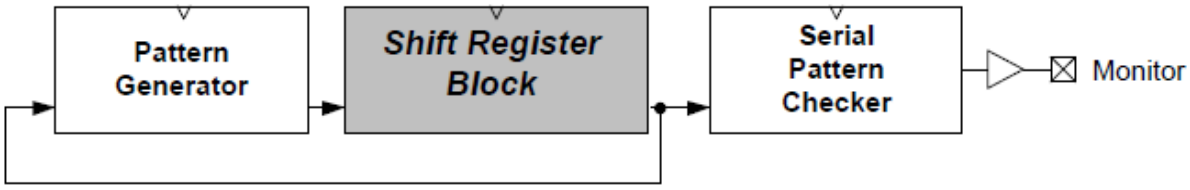

Fig. 39. Shift Register Block

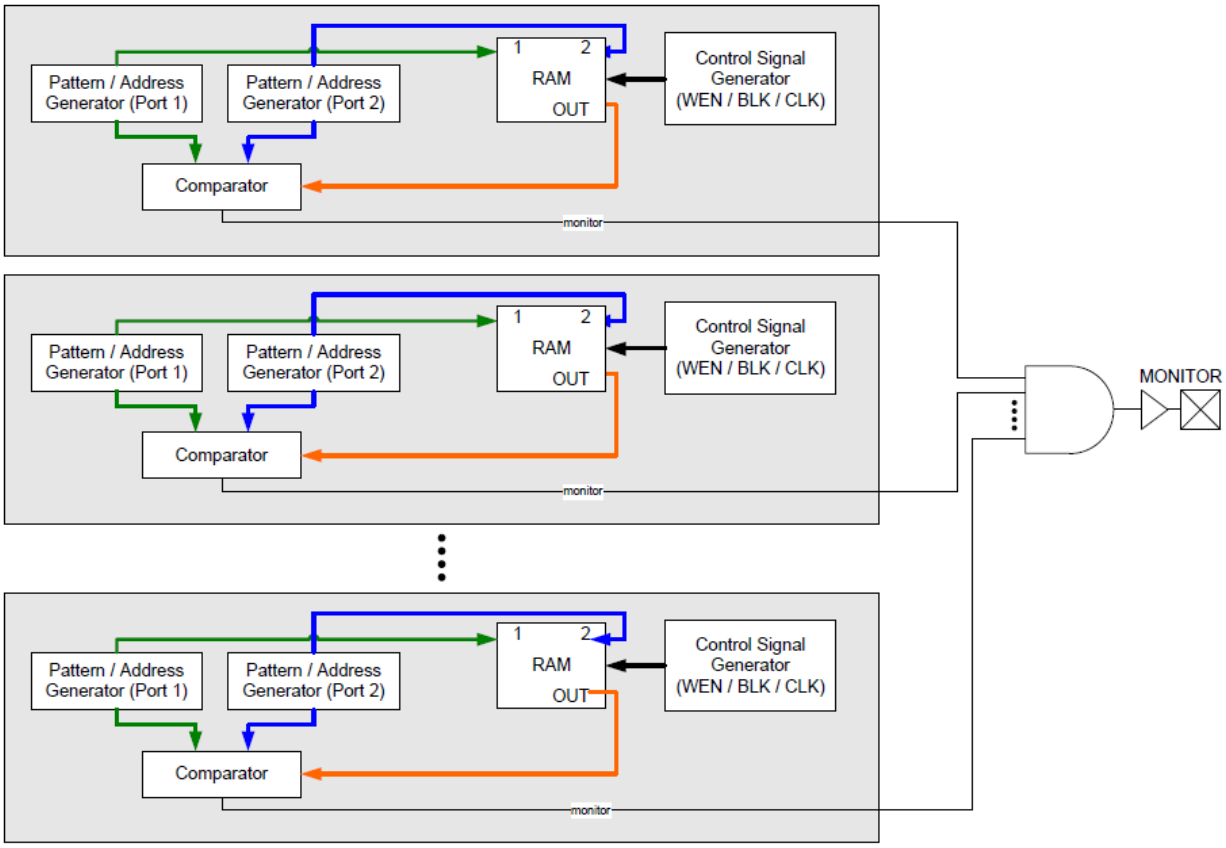

Fig. 40. Embedded Ram Blocks

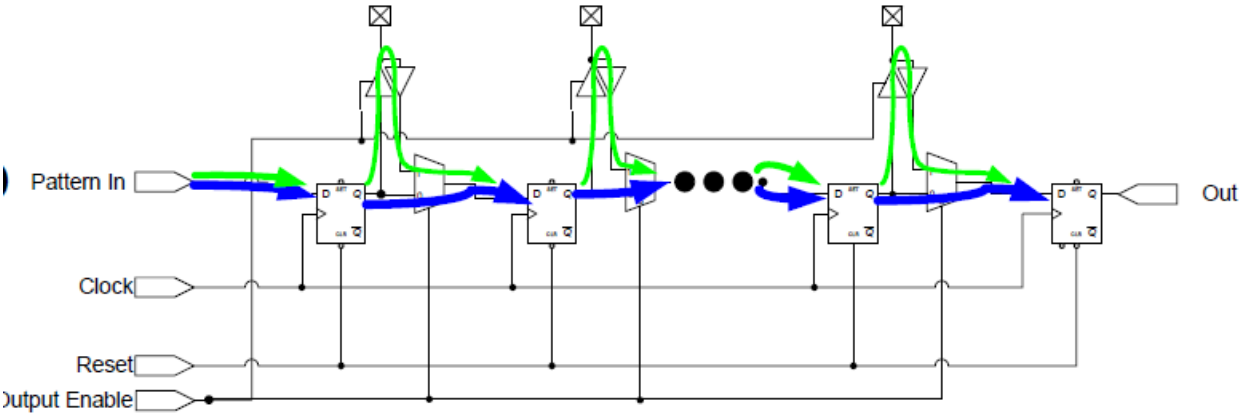

Fig. 41. IO Block

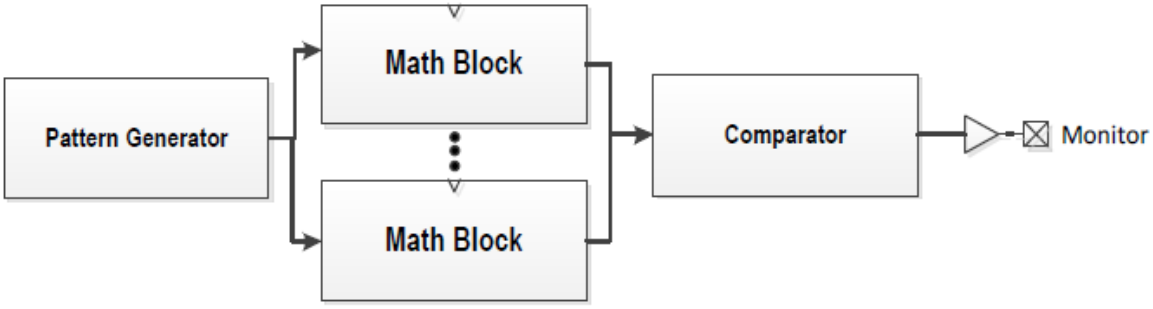

Fig. 42. Math Block

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