Libero SoC PolarFire v2.1

Release Notes

4/2018

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Power Matters.™

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.2

Revision 1.2 includes the following changes:

- Section 1.2.2: Removed Silicon Support references from IOD Receive Interfaces table
- Sections 5.6 and 5.12: Added additional limitations

Revision 1.1

Revision 1.1 includes the following changes:

- Added SmartDebug support for MPF300XT device.
- Removed QDR references, as the QDR cores will be supported at a later date.

Revision 1.0

Revision 1.0 was the first publication of this document.

Reference Documents

PO0137: Product Overview PolarFire FPGA

DS0141: PolarFire FPGA Datasheet

UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide

Pin package Assignment Tables:

- MPF300T/MPF300TS-FCG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCVG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCSG536 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG784 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG1152 Package Pin Assignment Table

UG0752: PolarFire FPGA Power Estimator User Guide

UG0680: PolarFire FPGA Fabric User Guide

UG0684: PolarFire FPGA Clocking Resources User Guide

UG0686: PolarFire FPGA User I/O User Guide

UG0677: PolarFire FPGA Transceiver User Guide

UG0685: PolarFire FPGA PCI Express User Guide

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide

UG0676: PolarFire FPGA DDR Memory Controller User Guide

UG0748: PolarFire FPGA Low Power User Guide

Athena TeraFire Cryptographic Algorithm Library (CAL) Users Guide

UG0743: PolarFire FPGA Debugging User Guide

UG0714: PolarFire FPGA Programming User Guide

UG0725: PolarFire FPGA Device Power-Up and Resets User Guide

UG0726: PolarFire FPGA Board Design User Guide

UG0753: PolarFire FPGA Security User Guide

UG0786: PolarFire FPGA Splash Kit User Guide

DG0755: PolarFire FPGA JESD204B Interface Demo Guide

DG0756: PolarFire FPGA PCIe Endpoint Demo Guide

DG0757: PolarFire FPGA 10GBASE-R Ethernet Loopback Demo Guide

DG0759: PolarFire FPGA Multi-Rate Transceiver Demo Guide

DG0762: PolarFire FPGA DSP FIR Filter Demo Guide

Verilog Simulation Guide

VHDL Simulator Guide

PolarFire FPGA Design Flow User Guide

PolarFire FPGA Macro Library Guide

PolarFire FPGA Design Constraints User Guide

PolarFire FPGA PDC Commands User Guide

PolarFire FPGA Timing Constraints User Guide

PolarFire FPGA Tcl Commands User Guide

PolarFire FPGA I/O Editor User Guide

Chip Planner User Guide

Netlist Viewer Interface User Guide

PolarFire FPGA Netlist Viewer User Guide

SmartPower User Guide

Timing Constraints Editor User Guide

SmartTime Static Timing Analyzer User Guide

PolarFire FPGA SmartDebug User Guide

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1 Libero SoC PolarFire™ v2.1 Software Release Notes

The Libero® system on chip (SoC) PolarFire™ v2.1 release is software for designing with Microsemi PolarFire FPGAs. PolarFire FPGAs are the fifth generation nonvolatile FPGA devices from Microsemi, built on 28-nm flash technology. The PolarFire cost-optimized FPGAs deliver lowest power at mid-range densities.

For more information about PolarFire devices, see the Microsemi website.

1.1 What's New in Libero SoC PolarFire v2.1

The Libero SoC PolarFire v2.1 release includes the following new features and enhancements.

1.1.1 MPF300XT Production Device Support

With Libero SoC PolarFire v2.1, support is added for the MPF300XT device, the first production device in the PolarFire FPGA family. This release includes the following support for this device:

- Full Libero flow
- Production Timing Data
- Programming support
- SmartDebug support

1.1.2 Synthesis

The following Synthesis enhancements are included in this release:

- An improved net delay model, potentially enhancing QoR and correlation with post-layout timing
- MATH block inference: Coefficient ROM in DOTP mode
- ROM Inference: For inferred ROMs, an option has been added in Libero -> Synthesis -> Configure Options to map ROM constructs to Logic or RAM. If SynplifyPro is invoked through Libero, by default, inferred ROM constructs will be mapped to FPGA Logic. Set the above new option to "RAM" to map ROM constructs to RAM instead.

1.1.3 Timing

- Production timing support has been implemented for the MPF300XT device.
- MPF300T/TS_ES devices' timing data has been updated to be the same at the MPF300XT device.
- The default corner for max delay worst case timing analysis has been changed to match silicon.

1.1.4 I/O Editor

Libero SoC PolarFire v2.1 supports two types of pinouts for DDR3, DDR4, and LPDDR3 memory interfaces: "migratable" and "device-optimized". If you use a migratable pinout, you can move your design to another device (with the same package) in the PolarFire family without needing to change your memory placement. Device-optimized pinouts are not migratable across multiple devices, but are more compact and offer higher performance.

1.1.5 Programming

Important note for Block Flow users: In this release, the Block Flow must not be used for designs intended to be programmed onto silicon, for any PolarFire device.

- Programming is supported for the MPF300XT device.
- SPI Flash programming times have been improved by a factor of approximately 2x. TCK can be configured at up to 15MHz; it was limited to 4MHz in Libero SoC PolarFire v2.0. Increasing TCK will improve programming time for the SPI Flash.

- Configuration and programming of Data Storage clients is supported for the SPI Flash.
- BSDL files generated using Libero SoC PolarFire v2.1 are now compliant with IEEE standard 1149.6 as well as 1149.1.

1.2 Silicon Features

1.2.1 Memories

A number of enhancements are included in Libero SoC PolarFire v2.1 to enhance support for Memory Interfaces:

- LPDDR3 memory is now supported.
- DDR3 and DDR4 improvements for reliability.
- For the PolarFire SRAM (AHBLite and AXI) core, an additional Native interface is now supported.
- Note: QDR is supported in Libero SoC PolarFire v2.1 software; however, the PolarFire QDR core will be made available at a later date in the Catalog.

1.2.2 IOD Receive Interfaces

- Clock topologies around the perimeter of the IO ring updated for implementation of IOD Rx interfaces
- New centered interface support for ratio 2/3.5/4/5

The following table lists the IOD Receive interfaces available with this release.

Interface	Design Creation/ Simulation/Place and Route
RX_DDR_G_A	Yes
RX_DDR_L_A	Yes
RX_DDR_G_C	Yes
RX_DDR_L_C	Yes
RX_DDRX_B_A	Yes
RX_DDRX_BL_A	Yes
RX_DDRX_B_C	Yes
RX_DDRX_BL_C	Yes
RX_DDRX_B_DYN	Yes
RX_DDRX_BL_DYN	Yes
RX_DDRX_BL_A_MIPI	Yes
RX_DDRX_BL_DYN_MIPI	Yes
* I/O delay tap must be adjusted using the dynamic delay control ("Advanced->Debug->Expose dynamic delay control")	

1.2.3 Transceiver

- The Transceiver HDL simulation model has been updated for faster runtime.
- MPF300XT: The default Transceiver signal integrity parameters have been updated based on device characterization.

2 Device Support

Libero SoC PolarFire v2.1 Device Support (Devices and packages in **bold** are new in v2.1)

Device	Package	Speed Grade	Core Voltage	Range	License Required
MPF100T	**FCSG325**	**-1, STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Silver/Gold/Platinum**
	FCVG484	**-1, STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Silver/Gold/Platinum**
	FCG484	**-1, STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Silver/Gold/Platinum**
MPF100TS	**FCSG325**	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCVG484	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCG484	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
MPF200T	**FCSG325**	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
	FCSG536	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
	FCVG484	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
	FCG484	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
	FCG784	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Gold/Platinum**
MPF200TS	**FCSG325**	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCSG536	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCVG484	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCG484	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
	FCG784	**-1, STD**	**1.0/1.05V**	**IND**	**Eval/Platinum**
MPF300T_ES	FCG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG1152	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCSG536	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCVG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG784	-1, STD	1.0/1.05V	EXT/IND	Eval/Platinum
MPF300TS_ES	FCG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
	FCG1152	STD	1.0 /1.05V	EXT/IND	Eval/Platinum
		-1	1.0 /1.05V	EXT/IND	Eval/Gold/Platinum
	FCSG536	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCVG484	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
	FCG784	-1, STD	1.0 /1.05V	EXT/IND	Eval/Platinum
MPF300XT	**FCG1152**	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCG484	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCG784	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
MPF300T	**FCG484**	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCG1152	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCSG536	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCVG484	**-1, STD**	**1.0 /1.05V**	**EXT/IND**	**Eval/Platinum**
	FCG784	**-1, STD**	**1.0/1.05V**	**EXT/IND**	**Eval/Platinum**

MPF300TS	FCG484	-1, STD	1.0/1.05V	IND	Eval/Gold/Platinum
	FCG1152	STD	1.0 /1.05V	IND	Eval/Platinum
		-1	1.0 /1.05V	IND	Eval/Gold/Platinum
	FCSG536	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCVG484	-1, STD	1.0/1.05V	IND	Eval/Platinum
	FCG784	-1, STD	1.0/1.05V	IND	Eval/Platinum
MPF500T	FCG784	-1, STD	1.0/1.05V	EXT/IND	Eval/Platinum
	FCG1152	-1, STD	1.0/1.05V	EXT/IND	Eval/Platinum
MPF500TS	FCG784	-1, STD	1.0 /1.05V	IND	Eval/Platinum
	FCG1152	-1, STD	1.0 /1.05V	IND	Eval/Platinum

See the Licensing web page for licensing details.

3 Design Migration

3.1 General Notes on Design Migration

3.1.1 Device and Package Name Changes

The following devices were renamed in Libero SoC PolarFire v2.1:

- MPF100T/TS_ES renamed to MPF100T/TS
- MPF200T/TS_ES renamed to MPF200T/TS
- MPF500T/TS_ES renamed to MPF500T/TS

Libero SoC PolarFire v2.0 projects opened with v2.1 will be automatically converted to use the new device names.

EVAL packages (packages with the "_EVAL" suffix) are no longer supported in v2.1. When you open a v2.0 project containing an EVAL package, it will be automatically converted to the production version; the production packages are equivalent to the EVAL packages.

Fully Bonded Packages for MPF100T/TS and MPF200T/TS devices are no longer supported in Libero SoC PolarFire v2.1. Use Libero SoC PolarFire v2.0 to convert any designs using the Fully Bonded Packages to use other supported packages before opening those designs in Libero SoC PolarFire v2.1.

3.1.2 Design Invalidation

Libero SoC PolarFire v2.1 is a major release milestone in the Microsemi® PolarFire FPGA program. The timing numbers and worst-case timing analysis have changed, and require that older PolarFire projects be invalidated in this release.

1. Upon opening a Libero SoC PolarFire v2.0 project, Verify Timing and Verify Power will be invalidated. You must rerun these steps to regenerate the timing and power reports.
2. You must upgrade to the latest version, or regenerate cores that have been invalidated and re-generate existing designs through full implementation and timing verification flow.
    a. You must also rerun the Derive Constraints step before running Synthesis or Place-and-Route to get the most up-to-date configured core-related timing constraints.

The following is the list of cores that have been invalidated in Libero SoC PolarFire v2.1:

Core	User Action
DDR3	Upgrade to latest version in Catalog
DDR4	Upgrade to latest version in Catalog
PolarFire SRAM (AHBLite and AXI)	Upgrade to latest version in Catalog
PCI Express	Upgrade to latest version in Catalog
Transceiver Interface	Regenerate Core
PolarFire IOD Generic Receive Interfaces	Upgrade to latest version in Catalog
PolarFire IOD Generic Transmit Interfaces	Upgrade to latest version in Catalog
PolarFire IOD CDR	Regenerate Core
PolarFire RGMII TO GMII	Upgrade to latest version in Catalog
CoreSmartBERT	Upgrade to latest version in Catalog

PF Micro SRAM	Regenerate Core
PF Dual-Port Large SRAM	Regenerate Core
PF Two-Port Large SRAM	Regenerate Core

3.2 Cores Supported in Libero SoC PolarFire v2.1

Display Name	Libero SoC PolarFire v2.1	Changes from Libero SoC PolarFire v2.0
Clock Conditioning Circuitry (CCC)	1.0.112	None
Clock divider	1.0.102	Fixed derived constraint for x5/x3.5 ratio
CoreSmartBERT	2.0.106	None
Crypto	1.0.101	None
DDR3	2.2.109	Production solution with MPF300XT
DDR4	2.2.109	Production solution with MPF300XT
Glitchless clock mux	1.0.101	None
LPDDR3	2.1.111	New for 2.1, production solution with MPF300XT
PCI Express	1.0.234	See details below
PF Dual-Port Large SRAM	1.1.110	Bug Fixes to support future enhancements
PF Micro SRAM	1.1.107	Bug Fixes to support future enhancements
PF Two-Port Large SRAM	1.1.108	Bug Fixes to support future enhancements
PF uPROM	1.0.108	None
PolarFire 7:1 LVDS Receive Interface	1.0.104	None
PolarFire 7:1 LVDS Transmit Interface	1.0.104	None
PolarFire Dynamic Reconfiguration Interface	1.0.101	None
PolarFire IOD CDR	1.0.210	None
PolarFire IOD Generic Receive Interfaces	1.0.238	Functional Bug Fixes
PolarFire IOD Generic Transmit Interfaces	1.0.234	Minor UI Enhancements
PolarFire Initialization Monitor	2.0.101	None
PolarFire RC Oscillators	1.0.102	None

PolarFire RGMII TO GMII	1.0.207	None
PolarFire SRAM (AHBLite and AXI)	1.1.123	Added support for a Dual-Port Native Interface
Tamper	1.0.102	None
Transceiver Interface	1.0.223	Functional Bug fixes
Transceiver Reference Clock	1.0.103	None
Transmit PLL	1.0.109	None

3.2.1 Changes to PCI Express Core in Libero SoC PolarFire v2.1

In Libero SoC PolarFire v2.1, the following enhancements have been made to the PCI Express core:

- All devices: The AXI Translation address in the Master Settings window and the AXI Source address in the Slave Settings window are now limited to 32 bits (including the [11:0] reserved bits). Users can enter translation addresses in the range 0x0000_0 - 0xFFFF_F (equivalent to a 32-bit range of 0x0000_0000 - 0xFFFF_F000).
- The fundamental reset port (PERST_N) is now available for MPF100/200/300/500 T/TS devices.

4 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC PolarFire v2.1. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

4.1 List of Resolved Issues

Case Number	Description
493642-2417096507	Placer unable to find valid placement for ICB_CLKINT
493642-2417773203	CoreFIFO Generation Error
493642-2397475099	PCIe BAR Simulation hangs
493642-2416349115	Eye Monitor takes longer to plot the Eye the first time
493642-2268812377	DDR constraints coverage report indicates missing ddr constraints and violations
493642-2410129119	Libero crashes when handling VHD: Packages with Array of Records
493642-2370609002	SmartDebug always shows the Transceiver data width as 40 even though it is configured for a different value
493642-2363102341	Enhancement request to support dual port RAMs and native interface for PF_AHB_AXI_SRAM
	BAR2 in the PCI configuration space is enabled despite being disabled in the PCIe configurator
	PF_XCVR: Additional Drive Settings needed to set Lane in EQ-NEAREND mode in SmartDebug
	PF_XCVR: Incorrect Cumulative Error Count Output for internal prbs patterns in SmartBERT tests, SmartDebug
	Fixed configuration to support Firewire (S800) protocol
	PCIe MSI interrupts are not set correctly

5 Known Issues and Limitations

5.1 SPI Flash Programming

This release includes the following limitations:

- Only the Micron SPI Flash is currently supported with the Evaluation Kit.
- This tool erases the SPI Flash prior to programming. It is recommended to program the SPI Flash with Libero SoC PolarFire v2.1 prior to programming other data on the SPI Flash using non-Libero programming solutions.
- Partial update of the SPI Flash is currently not supported.
- It is not recommended to have huge gaps between clients in the SPI Flash, since gaps are currently programmed with 1's and will increase programming times.

  The following table lists the ERASE, PROGRAM, and VERIFY/READ times for different client sizes. All times are in hh:mm:ss.

  Note: Depending on the SPI-Flash memory silicon version, you may observe a shorter erase time.

SPI Size	ERASE	PROGRAM	VERIFY/READ	TCK	Programmer
1 MB	00:03:55	00:00:45	00:10:46	4MHz	FP5
1 MB	00:03:55	00:00:28	00:10:05	15MHz	FP5
9 MB	00:03:55	00:06:38	01:19:15	4MHz	FP5
9 MB	00:03:55	00:04:26	01:08:49	10MHz	FP5
18 MB	00:03:55	00:09:04	02:32:43	10MHz	FP5
128 MB	00:03:55	00:58:38	22:07:55	15MHz	FP5

5.2 SPI-Slave Programming

Programming Libero SoC PolarFire v2.1 via SPI instead of JTAG is currently not supported. Support for this use model will be added in a future release.

5.3 PolarFire and FlashPro Express - MPF300T_ES or MPF300TS_ES Programming File Fails to Program a MPF300XT Device

In Libero SoC PolarFire v2.1 and FlashPro Express, the MPF300T_ES or MPF300TS_ES programming file cannot program a MPF300XT device, and vice versa.

Workarounds:

1. Change the device in Libero to match the target device.
2. Export DAT file format to use for DirectC.
3. Export a STAPL file from Libero and use standalone FlashPro on Windows in single mode to program.

5.4 SmartDebug

This release includes the following limitations:

- General Limitations
  - Standalone SmartDebug: Non Microsemi Devices in chain: Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug. **Workaround**: Users should use SmartDebug through the Libero flow to debug Microsemi Devices.
  - Standalone SmartDebug: ID Code of Microsemi device cannot be read when non-Microsemi device is connected in chain when using standalone SmartDebug.

    Workaround: Users should use SmartDebug through the Libero flow to perform this operation.
  - Logical View: The logical view cannot be reconstructed for:
    - LSRAM/uSRAM for port widths of x1 inferred through RTL.
    - LSRAM/uSRAM configurations when a single net of output bus is used i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using physical view.
    - LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
    - HDL modules inferring RAM blocks are instantiated in SmartDesign.
- Transceiver Limitations
  - CDR-Far End loopback mode does not successfully loopback the data from Rx to Tx. This will be fixed in an upcoming PolarFire release.
  - Plot eye introduces a burst of errors in data traffic on XCVR lanes when started. This will be fixed in an upcoming PolarFire release.
  - The Custom DFE solution (using the Optimize DFE option in the Eye Monitor tab) does not work when the transceiver is configured in 8B10B PCS-PMA mode and the receiver is DFE.

    Workaround: Perform the following steps to obtain the expected eye output with PLOT_EYE.

    1. Assert PCS RX RESET
    2. Optimize DFE
    3. Plot Eye
    4. De-Assert PCS RX RESET
  - SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- Linux Limitations
  - Demo Mode does not work on Linux platforms. SmartDebug crashes when Debug XCVR is invoked in demo mode without connecting a programmer to the machine.
  - Optimize DFE does not work on Linux platforms. This will be fixed in the next PolarFire release.
  - Signal Integrity parameters modification through SmartDebug does not work on Linux platforms. This will be fixed in the next PolarFire release.

5.5 Block Flow

In this release, the Block Flow must not be used for designs intended to be programmed onto silicon. The Block Flow will be fully supported in Libero SoC PolarFire v2.2.

5.6 DDR3 and DDR4 and LPDDR3 Memories

- The Constraints Coverage report indicates some missing constraints; this can be ignored.
- Dual rank is not supported for DDR3/DDR4.
- Data Bus Inversion is not supported for DDR4.
- The Lookahead Activate and Precharge option is selectable but not functional. Selecting this option will have no effect in simulation, or on silicon.

5.7 DLL

- **Secondary Phase Restrictions Missing:** Although the user can specify values for Primary and Secondary phase with no restrictions, the Secondary Phase value cannot be lower than the Primary Phase value.
  Workaround: Do not set the Secondary Phase value lower than the Primary Phase value.
- In DLL Phase Generation Mode, the secondary output clocks are not producing the correct phase in pre-synth HDL simulations.

5.8 PLL

- Only the post-VCO feedback mode is available in this release.
- Bypass option on output clocks is not available in this release.

5.9 PCIe

- The AXI interface minimum clock frequency is 125 MHz. If the user would like the AXI4 to run slower, the CoreAXI4Interconnect uses a clock per interface to allow the PCIe to run at 125MHz while the rest of the design can run slower.
- For BFM simulation of AXI master or slave, the simulator may print out a warning message about AHB signals, such as “HRESP”. The warning message can be ignored.
- Simulation support for fundamental reset (PERST_N) and SECDED is not available in Libero SoC PolarFire v2.1 and will be added in a future release for the MPF100/200/300/500 T/TS devices.

5.10 Transceiver

- When XCVR is configured in 8b10b mode and the PCS-Fabric width is 16, the following Interface Clock options are not supported for both TX and RX Clocks:
  - Use as PLL reference clock option
  - Global and Global (Shared) options
- When the PCS-Fabric width is configured to be 64 or 80, the Interface clock option “Use as PLL reference clock” is not supported.

5.11 IOD Receive Interfaces

The External PLL option is not supported while using a Regional Clock for the IOD RX Interface. This option should not be used, and will be removed from the UI in a future release.

5.12 External Hold Repair

When the Repair Minimum Delay Violations option is enabled in Place and Route and the design contains negative minimum delay slacks on an input I/O, the repair will fail. As a workaround, insert a sufficient number of BUFD cells on the I/O path based on the magnitude of the negative slack.

5.13 Synthesis

Synplify Pro is intended to be used only with PolarFire devices in this release.

Inferred MathBlocks: Libero SoC PolarFire v2.1 does not support the B2 pin of the MACC_PA_BC_ROM. The B2 pin going to fabric will not be routed. If this pin has been used in a SynplifyPro-inferred MACC_PA_BC_ROM or in HDL, Compile will error out with the message: “Using 'B2' pins is not supported in this release of software on instance”

5.14 Standalone Synthesis Flow

Libero SoC PolarFire v2.1 users may synthesize their design outside the PolarFire tool by using Synopsys SynplifyPro directly. When using this flow, the following additional steps are necessary to successfully synthesize and implement a design:

- Ensure that the <install location>/Designer/data/aPA5M/polarfire_syn_comps.v is passed to SynplifyPro. This file contains module declarations with timing information for PolarFire primitives not known to Synopsys.
- Many configured cores generate timing constraints. You must ensure that these constraint files are passed to synthesis for optimal results. These constraint files must also be imported into PolarFire along with the synthesis gate level netlist to get optimal place and route results and have correct timing analysis done by PolarFire. Core generate constraint files must be modified so that constraints are expressed using the proper hierarchical name of the configured cores in the top-level design.

5.15 PolarFire Core Generation Language

With Libero SoC PolarFire v2.1, some PolarFire cores generate only Verilog files, regardless of the preferred HDL language selected. Affected cores include:

- Cores in the PolarFire Features list
- Clocking: CCC, RC Oscillators, No-Glitch Mux
- Memories: DDR3, DDR4, LPDDR3, Large SRAM, Micro SRAM

VHDL users desiring to simulate designs containing affected cores must use mixed-language simulation (available with ModelSim ME Pro).

5.16 Other Limitations

This release has the following additional limitations:

- Post-synthesis and post-layout simulations are not supported.

- IBIS generation is not supported.

  Note: Generic IBIS models are available on the Microsemi website and can be used; however, they will not include design specific data such as package parasitics or IO options such as termination. These will require manual adaption to the generic IBIS models.

5.17 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

5.18 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click Yes and the software is installed successfully.

5.19 Installation on Windows 7

During Libero SoC PolarFire v2.1 installation on Windows 7 machines, you may see pop-up warning messages about shortcuts toward the end of installation process.

These messages can be safely ignored. Click OK to close the pop-up windows and the installation will proceed and complete as expected. All Windows shortcuts will appear correctly.

5.20 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running PolarFire successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC PolarFire v2.1, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

6 System Requirements

The Libero SoC PolarFire v2.1 release has the following system requirements:

- 64-bit OS
  - Windows 7, Windows 8.1, or Windows 10 OS
  - RHEL 5, RHEL 6, RHEL 7, CentOS 5, CentOS 6, or CentOS 7
    - Programming is not supported on RHEL 5, CentOS 5
- A minimum of 32 GB RAM

Note: Setup instructions for using Libero SoC PolarFire v2.1 on Red Hat Enterprise Linux OS or CentOS are available here. As noted in that document, installation step 2 now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

Note: Support for the following operating systems will cease after December 2017. Libero SoC PolarFire v2.2 (the next major planned PolarFire release) will not support the below OS versions. For more information, refer to PCN17031.

- RedHat Enterprise Linux 5.x through 6.5
- CentOS 5.x through 6.5

7 Download Libero SoC PolarFire v2.1 Software

The following are available for download:

- Libero SoC PolarFire v2.1 for Linux
- Libero SoC PolarFire v2.1 for Windows
- Libero SoC PolarFire v2.1 MegaVault

Note: Installation requires administrative privileges.

After successful installation, clicking **Help-> About Libero** will show Version: 12.100.10.13