LX8247

Datasheet

Dual eFuse with Current Monitor

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in February 2018. It was the first publication of this document.

2 Product Overview

The LX8247 consists of dual 5 V and 12 V eFuse over-voltage protection switches.

The 5 V and 12 V eFuse switches are designed for hot swap and limit inrush current limiting. In addition, they provide fast-acting protection of voltage surges, output over-current, and crow bar events. Under an input voltage surge condition, the eFuse devices clamp the output voltage to protect downstream circuitry and maximize run time. In addition to surge protection, the 5 V eFuse switch provides bidirectional voltage blocking to block current in the reverse direction under input voltage crowbar conditions. Both eFuses have thermal protection to protect all circuitry in the event of sustained surge or short conditions.

The LX8247 has dual current monitoring outputs to allow monitoring of the input power under all conditions. Both the 5 V and 12 V inputs are monitored.

Flexible SATA and SAS disable modes are supported and can be tailored to a particular system.

2.1 Features

- 12 V eFuse
  - Current limiting (hot swap inrush, over-load, short-circuit)
  - Output voltage clamping and soft start
  - Output current monitoring
  - Thermal latch off
- 5 V eFuse
  - Current limiting (hot swap inrush, over-load, short-circuit)
  - Output voltage clamping and soft start
  - Current monitoring
  - Reverse current protection
  - Thermal latch off
- High-speed (3.4 MHz) I^2C serial bus
- PowerDisable support

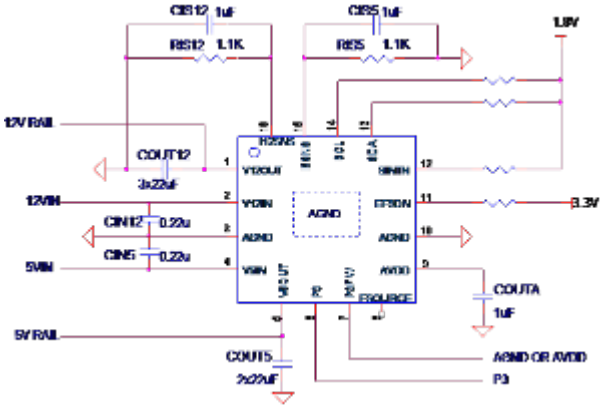
2.2 Applications

- Gen 2 enterprise HDD

2.3 Typical Application

The following illustration shows a typical application of the LX8247 device.

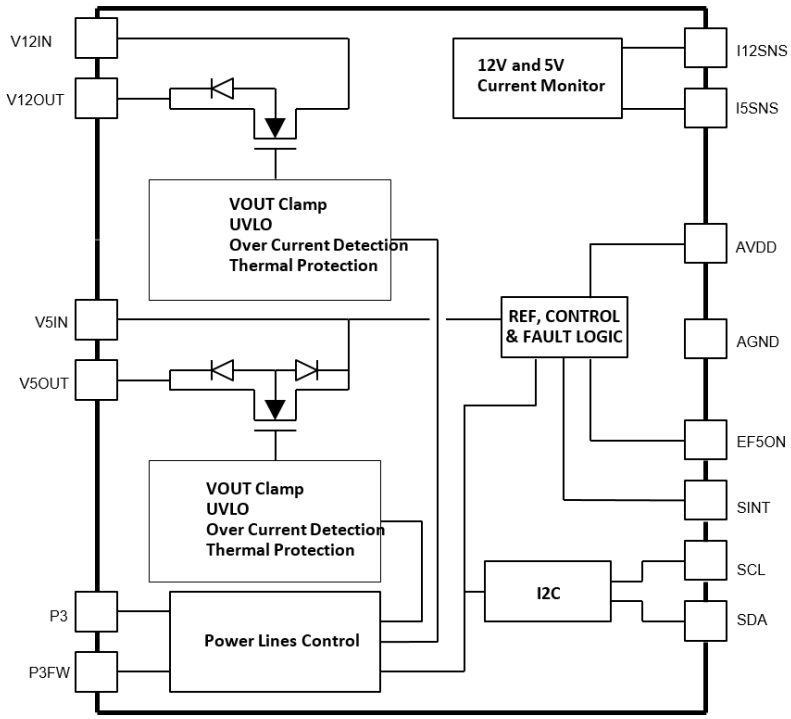
Figure 1 • Typical Application of LX8247



2.4 Block Diagram

The following illustration shows a simplified block diagram of the LX8247 device.

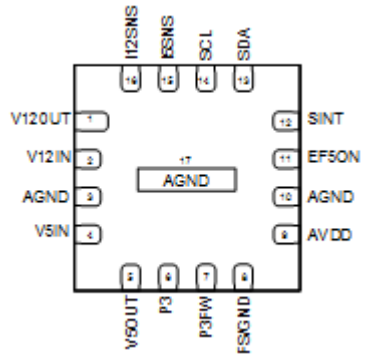
Figure 2 • Block Diagram



3 Pin Descriptions

The following illustration shows the top view of the pinout of the LX8247 device.

Figure 3 • Pinout QFN 16L 3.0 mm × 3.0 mm



The following four lines indicate the top marking on the device.

- Pin 1 Indicator

MSC

8247

YYWWL = Year/Week/Lot identifier

The following table describes the pins of the LX8247 device.

Table 1 • Pin Description

Pin Number	Pin Name	Pin Type	Description
1	V12OUT	Power output	12 V eFuse output. Clamped at 15 V when V12IN goes beyond 15 V. The initial slew rate at this pin is controlled to limit turn-on surge currents.
2	V12IN	Power input	12 V Input.
3	AGND	Power input	Ground. Connect to the board GND plane at a single point.
4	V5IN	Power input	5 V input.
5	V5OUT	Power output	Bidirectionally protected 5 V output. Clamped at 6 V. The initial slew rate at this pin is controlled to limit turn-on surge currents.
6	P3	Digital input	SAS P3 PowerDisable. 3.3 V CMOS input. Force high to initiate PowerDisable sequence. Force low to enter active mode.
7	P3FW	Digital input	Allow firmware to control P3 function when P3FW is connected to AVDD
8	GND (FSOURCE)	Power input	Ground. Internally reserved for programming eFuse. 6 V power source pin for programming OTP. After programming, this pin needs to be grounded.

Pin Number	Pin Name	Pin Type	Description
9	AVDD	Power output	Output of the internal pre-regulator. This housekeeping voltage will be used to generate internal bias currents and voltages. It also represents the voltage that is used for internal IC communication. This pin is not to be used by external circuitry. A 1 uF bypass cap should be placed between AVDD and AGND.
10	AGND	Power input	Ground. Connect to the board GND plane at a single point.
11	EF5ON	Digital output	Open drain ouput. External pull up resistor is required. Logic 1 indicates 5 V eFuse FET is closed.
12	SINTN	Digital output	General purpose interrupt output. External pull-up resistor is required. Logic 0 to indicate interrupt.
13	SDA	Digital in/out	I^2C data port. External pull-up resistor is required. 1.8 V CMOS logic levels. The power supply for the external pull-up resistors is assumed to be at 1.8 V, but the sequencing of this supply can occur at any time before, during, or after powering of the LX8247 5 V or 12 V input. If this power supply drops below 1.8 V logic level threshold's tolerance value (±10%), then I^2C communication can be interrupted. The default register value loading of all I^2C registers (customer and test) should be independent on the SDA state.
14	SCL	Digital input	I^2C clock port. External pull-up resistor is required. 1.8 V CMOS logic levels. The power supply for the external pull up resistors is assumed to be at 1.8 V, but the sequencing of this supply can occur at any time before, during, or after powering of the LX8247 5 V or 12 V input. If this power supply drops below 1.8 V logic level thresholds tolerance value (±10%), then I^2C communication can be interrupted. The default register value loading of all I^2C registers (customer and test) should be independent on the SCL state.
15	I5SNS	Analog output	5 V eFuse output current monitor. Connect to an external parallel R-C filter network. These component values will be adjusted when the final gain of the current monitor is determined.
16	I12SNS	Analog output	12 V eFuse output current monitor. Connect to an external parallel R-C filter network. These component values will be adjusted when the final gain of the current monitor is determined.
17	AGND	Power input	Ground. Connected to back side thermal pad.

4 Electrical Specifications

The following section describes the electrical specifications of the LX8247 device.

4.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings of the LX8247 device.

Table 2 • Absolute Maximum Ratings

Parameter	Min	Max	Units
V12IN	–0.3	25	V
V5IN, V12OUT	–0.3	15	V
V12OUT current		3.5	A
V5OUT current		3.5	A
P3, P3FW, V5OUT, SINTN, SDA, SCL, I5SNS, I12SNS, AVDD, EF5ON	–0.3	6.5	V
Junction temperature	–10	150	°C
Storage temperature	–65	150	°C
Peak solder reflow temperature (40 seconds)		260+0,–5	°C
ESD (human body model)		2000	V
ESD (charged device model)		500	V

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

4.2 Operating Ratings

The following table describes the operating ratings of the LX8247 device.

Table 3 • Operating Ratings

Parameter	Min	Typ	Max	Min
V12IN voltage	10.8		13.2	V
V12OUT continuous current			2.5	A
V5IN voltage	4.3		5.5	V
V5OUT voltage	2.5		5.5	V
V5OUT continuous current			2.5	A
Serial I/F voltage	1.7	1.8	1.95	V
P3 input voltage	–0.3	3.3	3.6	V
P3FW input voltage	–0.3		1.1*AVDD	V
Junction temperature	–10		125	°C
Ambient temperature	–10		85	°C

4.3 Thermal Properties

The following table describes the thermal properties of the LX8247 device.

Table 4 • Thermal Properties

Thermal Resistance (wDFN)	Typ	Units
θ_{JA}	50	°C/W

Note: The θ_{JX} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

4.4 Electrical Characteristics

Unless otherwise specified, the following specifications apply over the operating ambient temperature of –40 °C ≤ T_A ≤ 85 °C. Except where otherwise noted, the following test conditions apply: V12IN= 12 V, V5IN= 5 V, Cin12= 0.22 uF, Cin5= 0.22 uF, Cout12= 3*22 uF, Cout5= 2*22 uF. Typical parameters refers to T_A= 25 °C.

Table 5 • Device

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Biasing current		V5IN current, P3 low at V12IN= 12 V, V5IN= 5 V		0.4	1	mA
		V5IN current, P3 high at V12IN= 12 V, V5IN= 5 V		0.4	1	mA
		V12IN current, P3 low at V12IN= 12 V, V5IN= 5 V		0.4	1	mA
		V12IN current, P3 high at V12IN= 12 V, V5IN= 5 V		0.4	1	mA

Table 6 • 12 V eFuse FET

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Inrush current	I_inrush	Inrush current during the hot-swap condition. Measure the input current into V12IN in the transient of VCC from 0 V to 12 V at the slew rate of 12 V/20 ns.			1.5	A
On resistance	Rdson	T_j= 25 °C, 200 mA through V12IN to V12OUT		62		mΩ
		T_j= 125 °C, 200 mA through V12IN to V12OUT		95		mΩ
Off state leakage current					11	uA
Continuous current	I_{DC}	T_A= 25° C; Note 1		2.5		A
Vout ramp time	T_{RISE}	Measure 10% to 90% rise time at V12OUT. Initiate the ramp by setting P3 low.		10		ms
Turn on delay	T_{DLY}	Measure delay from the falling edge of P3 to the 10% point at V12OUT.		1.3		ms
Output clamping voltage	V_{CLAMP}	V12IN= 18 V, DC test, no load. Measure V12OUT.	13.8		15	V
Maximum overshoot in the transient		Increase V12IN from 12 V to 24 V in 12 V/100 ns. Monitor the maximum excursion at V12OUT with no load.			15	V

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
UVLO falling threshold		Decrease V12IN. Observe when V12OUT with some load falls below V12IN by 100 mV.	8.8	9	9.24	V
UVLO rising hysteresis		Increase V12IN. Observe when V12OUT turns on. Calculate hysteresis as the difference between the rising and falling thresholds.	0.6	0.7	0.8	V
Short circuit current limit	Isc_lim	V12OUT < 1.5 V. Force V12OUT to 0 V, measure I (V12OUT).		1	1.5	A
Overloading current limit	Iavg_lim	Rdson change of the 12 V eFuse FET should be <10% before current reaches.	3	4	5	A
Limit transient peak	Ilim-Peak	Apply a 1.3 Ω load with a switch at Vin = 12 V.		8		A
Limit transient settle time	Tsetl	Time the transient settles within ±5% of the steady state value.		30		µs
Current monitor output current gain		Imon/IeFuse, ImonG= 0. Test at 200 mA and 300 mA.	285	294	303	uA/A
		Imon/IeFuse, ImonG= 1. Test at 200 mA and 300 mA.	570	588	606	uA/A
Current monitor error		I(eFuse12)= 200 mA, Imon/IeFuse. ImonG= 1. Calculate error vs. ideal value.		2	3	%

Table 7 • 5 V eFuse FET

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Inrush current	I_inrush	Inrush current during the hot-swap condition. Measure the input current into V5IN in the transient of VCC from 0 V to 5 V at the slew rate of 5 V/10 ns.			1.5	A
Operating output voltage range		Note 1	2.5		5.5	V
On resistance	Rdson	T_j= 25 °C, 200 mA through V5IN to V5OUT. Use Kelvin sensing and your 200 uV meter.		50		mΩ
		T_j= 125 °C, 200 mA through V5IN to V5OUT		95		mΩ
Off state leakage current					11	uA
Continuous current	I_{DC}	T_A= 25° C; Note 1		2.5		A
Vout ramp time	T_{RISE}	Measure 10% to 90% rise time at V5OUT. Initiate the ramp by setting P3 low.		10		ms
Turn on delay	T_{DLY}	Measure delay from the falling edge of P3 to the 10% point at V5OUT.		2.5		ms
Output clamping voltage	V_{CLAMP}	V5IN= 10 V, DC test, no load. Measure V5OUT.	5.7	6	6.3	V
Maximum overshoot in the transient		Increase V5IN from 5 V to 12 V in 70 ns (5 V/µs). Monitor the maximum excursion at V5OUT with no load.			6.5	V
UVLO falling threshold	UVLO_OFF_V5IN	Decrease V5IN. Observe when V5OUT with some load begins to fall.	4.0	4.1	4.2	V

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
UVLO rising threshold	UVLO_ON_V5IN	Decrease V5IN. Observe when V5OUT shuts down somehow. Calculate hysteresis as the difference between the rising and falling thresholds.	4.25	4.35	4.45	V
Short circuit current limit	Isc_lim	V5OUT < 1.5 V. Force 0 V at V5OUT measure I (V5OUT).		1	1.5	A
Overloading current limit	Iavg_lim	Rdson change of the 5 V eFuse FET should be <5% before current reaches 3 A.	3	4	5	A
Limit transient peak	Ilim-Peak	Apply a 620 mΩ load with a switch at Vin = 5 V.		7		A
Limit transient settle time	Tsetl	Time the transient settles within ±5% of the steady state value.		30		µs
Current monitor output current gain		Imon/IeFuse, ImonG= 0. Measure at 100 mA and 200 mA.		300		uA/A
		Imon/IeFuse, ImonG= 1. Measure at 100 mA and 200 mA.		600		uA/A
Current monitor error		I(eFuse12)= 100 mA, Imon/IeFuse.		2	3	%
Reverse current voltage threshold		For HGST requirement. Force V5OUT above V5IN. Monitor the eFuse status change. Determine the rising and falling thresholds.		–35		mV
Reverse current voltage hysteresis		See test above.		8		mV
Reverse current trigger level			0.2		1.27	A
EF5ON comparator deglitch filter		Note 1		500		ns

Table 8 • Temperature Monitor

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
EOTW	Early over temperature warning	Output disabled.	140	155	170	°C
OTth	EOTW	Sweep temperature. Thermal fault, output disabled.	160	175	190	°C
OThy	Over temperature hysteresis	Thermal fault, output disabled.		50		°C
Tdelta	Temperature difference from EOTW to OTth	Output enabled.	15	20	25	°C

Table 9 • P3 and P3FW

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
P3 logic rising threshold	VP3th	V(P3) < VP3th: Power enabled V(P3) > VP3th: Power disabled Digital XOR test mode output	1.2	1.6	2.0	V
P3 logic falling threshold hysteresis			200	300	400	mV
P3 pull-down resistor		Rpulldown	60	100	140	KΩ
P3FW logic rising threshold	VP3FWth	V(P3FW) < VP3FWth: P3EN register bit control through I²C is disabled. V(P3FW) > VP3FWth: P3EN register bit control through I²C is enabled. Digital XOR test mode output.	1.2	1.6	2.0	V
P3FW logic threshold hysteresis			200	300	400	mV

Table 10 • SINTN

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Output low voltage		ISINK(SINTN)= 1 mA			0.4	V
Output high leakage current		Set SINTN off, force 1.8 V at SINTN, measure the leakage current			2	uA

Table 11 • EF5ON

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Output low voltage		ISINK(EF5ON)= 1 mA			0.4	V
Output high leakage current		Set EF5ON off, force 1.8 V at SINTN, measure the leakage current			2	uA
EF5ON comparator deglitch				500		ns

Table 12 • I2C

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Vol-SDA		I=4 mA; Note 1			0.4	V
VDD for I²C interface		Input condition; Note 1	1.7	1.8	1.95	V
Vil		Logic0 input voltage; Note 1	-0.5		0.3 *VDD	V
Vih		Logic1 input voltage; Note 1	0.7 *VDD		VDD+0.5	V
Vihyst		Input hysteresis; Note 1	0.1 *VDD			V
Iin		Input current, Vi=0.1*VDD to 0.9*VDD; Note 1	–10		10	uA
Vol		Logic0 output voltage, Isink= 2 mA; Note 1	0		0.2 *VDD	V
Iol		Vol= 0.4 V; Note 1	3			mA

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Input voltage deglitch		Note 1	0		10	ns
SCL clock frequency		Note 1	0		3.4	MHz
T_{SU}, start/stop		Setup time; Note 1	160			ns
T_{HOLD}, start/stop		Hold time; Note 1	160			ns
T_{LOW}, SCL		Low pulse time; Note 1	160			ns
T_{HI}, SCL		High pulse time; Note 1	60			ns
T_{SU}, SDA		Data setup time; Note 1	10			ns
T_{HOLD}, SDA		Data hold time; Note 1	0		70	ns
T_{RISE}, tfall, SCL		Clock rise/fall time; Note 1	10		40	ns
T_{RISE}, tfall, SDA		Data rise/fall time; Note 1	10		80	ns

Note 1: Guaranteed by design.

5 Theory of Operation/Application Information

The following section describes the theory of operation and application information for the LX8247 device.

5.1 12 V eFuse Block Functions

The 12 V eFuse is initially on its off state. The ON/OFF control of the eFuse is based on the input pins Vin12, P3, P3FW, P3En bit and fault conditions. After the eFuse is allowed to turn on, it then ramps the output voltage to its final value while limiting the max current to the current limit value. If the input continues to rise above the OV12 threshold, the eFuse will limit the output to the OV12 limit and set the OV12 bit in the serial port. The 12 V eFuse will operate in this state until it hits its OT limit and shuts down. The eFuse will restart after temperature is below the OT hysteresis value. The 12 V eFuse block also has an output current monitor. The current monitor output current is proportional to the current of the 12 V eFuse from input to output.

5.2 5 V eFuse Block Functions

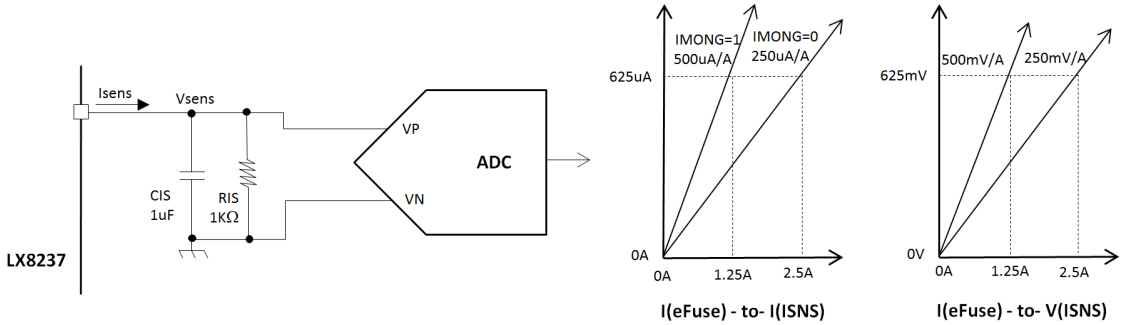
The 5 V eFuse is initially on its off state. The ON/OFF control of the eFuse is based on the input pins Vin5, P3, P3FW, P3En bit and fault conditions. After the eFuse is allowed to turn on, it then ramps the output voltage to its final value while limiting the max current to the current limit value. If the input continues to rise above the OV5 threshold, the chip will limit the output to the OV5 limit and set the OV5 bit in the serial port. The 5 V eFuse will operate in this state until it hits its OT limit and shuts down. The eFuse will restart after temperature is below the OT hysteresis value. When the current goes in the reverse direction above the threshold, the eFuse will open and isolate the output from the input. The eFuse will restart with current limit once the reverse current goes to zero and the input has satisfied the normal startup criteria. The 5 V eFuse block has an output current monitor. The current monitor output current is proportional to the current of the 5 V eFuse from input to output. The 5 V eFuse block has a logic output at EF5 on open drain pin to indicate when the eFuse is in its open protective state.

5.3 eFuse Current Monitor Function

The average current being supplied by each eFuse output can be monitored at I5SNS and I12SNS. A current proportional to the average eFuse output current will be sourced out of the sense pins. This current will be converted to a voltage and filtered by a parallel R-C network connected at I5SNS and I12SNS pins.

By default, the current monitors are disabled. They are enabled through the serial port. Any fault that turns off either the eFuses or the regulators will turn off the current monitor by reseting IMON bits as well. The current monitors have two different gain selections to allow for better resolution at different current ranges.

Figure 4 • Current Monitor Function



5.4 I2C Serial Interface

The chips supports a high speed (3.4 MHz) serial interface with the I²C serial protocol. This interface is bidirectional, allowing the microprocessor to set functions and read status. Status0/1 register bits are latched once the first fault happens. In this case, the following fault cannot write the register anymore. Only a write action to status0 register can clear both status0 and status1 registers.

Table 13 • Serial Bus Register Map

Address E6h			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Dec	Hex									
0	00H	ID1	DEV[1]	DEV[0]	MID[2]	MID[1]	MID[0]	NID[2]	NID[1]	NID[0]
		Read-only	1	1	0	0	1	0	1	0
1	01H	ID2	VID[3]	VID[2]	VID[1]	VID[0]	FAB[1]	FAB[0]	SID[1]	SID[0]
		Read-only	0	0	1	1	0	0	0	0
2	02H	TBD	NA	NA	TBD	TBD	TBD	TBD	TBD	TBD
		Read/Write	0	0	0	0	0	0	0	0
3	03H	TBD	NA	NA	TBD	TBD	TBD	TBD	TBD	TBD
		Read/Write	0	0	0	0	0	0	0	0
4	04H	CONTROL0	P3EN	IMONG	TBD	TBD	TBD	IMONEN	TBD	TBD
		Read/Write	0	0	0	0	0	0	0	0
5	05H	STATUS0	UV12	UV5	TBD	TBD	OT12	OT5	EOTW12	EOTW5
		Read/Write	0	0	0	0	0	0	0	0
6	06H	STATUS1	OC12	OC5	TBD	TBD	P3STATE	NA	OV12	OV5
		Read/Write	0	0	0	0	0	0	0	0

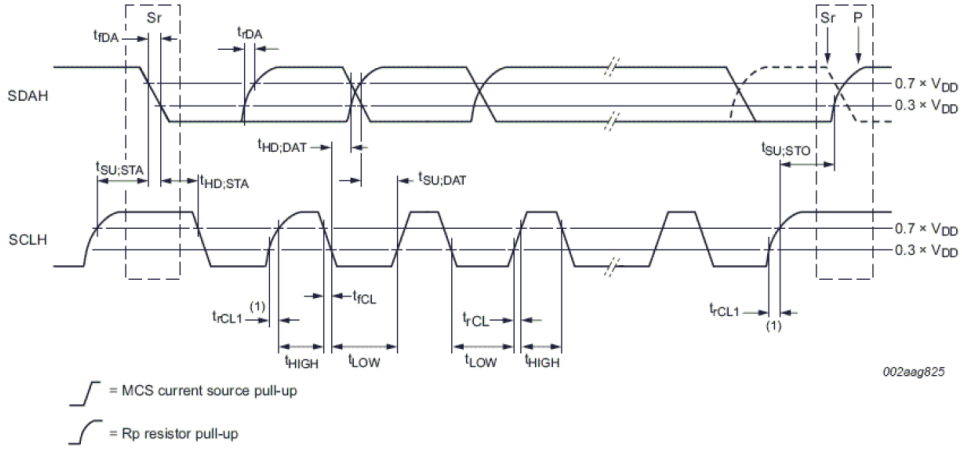
The abbreviations for the Serial Bus Register Map (see page 13) are listed, as follows:

ID1 and ID2:
DEV= Device [11]
MID= Major ID [001]: Mask revisions (includes pizza versions)
NID= Minor ID [010]
VID= Device [0000]: Device pizza version (ver 1= 0000, ver 2= 0001, ver 3= 0010, and so on)
FAB= Fab [00]
SID= Vendor ID [00]

IMONEN= eFuse current monitor enable
IMONG= Current monitor gain
P3EN= P3 PowerDisable feature enable
UV12= 12 V input voltage under voltage
UV5= 5 V input voltage under voltage
OT12= eFuse12 over temperature
OT5= eFuse5 over temperature
EOTW12= eFuse12 early temperature warning
EOTW5= eFuse5 early temperature warning
OC12= eFuse12 over current
OC5= 3Fuse5 over current
P3State= P3 pin state
OV12= eFuse12 input over voltage
OV5= eFuse5 input over voltage

The following illustration shows the I²C timing diagram.

Figure 5 • I2C Timing Diagram



(1) First rising edge of the SCLH signal after Sr and after each acknowledge bit.

5.5 Reverse Current Control of 5 V eFuse

The simplest protection against the reverse current is a diode in-series connection to the load. However, the power loss is significant at the forward current mode. At the worst, the supply rail of the load is not regulated. In order to solve this problem, the body gating technique is implemented for the LX8247. The basic concept of this method is to detect the polarity and amplitude of voltage drop through the pass N-type FET. Once the negative voltage drop is detected up to the specified threshold, an active switch connects the body of the pass FET from the source to drain. It generates the opposite polarity of body diode to block the reverse current.

Microsemi's approach to protect the discharging from the output capacitor is to utilize the combination of two protection methods. One method is to detect the voltage drop over the Rdson of the eFuse FET. The othere is to use the accurate input UVLO circuit.

The Rdson sensing is responsible for the high dv/dt input drop like crawbar response (max –5 V/µs). A 35 mV threshold is assigned to detect the reverse voltage from V5IN to V5OUT through the eFuse Rdson. If any reverse current generates a negative voltage drop ≥–35 mV across the eFuse by the high dv /dt, the eFuse will be shut off by the reverse protection circuit.

When V5IN is lower than the UVLO threshold, the UVLO circuit will also open the eFuse.

5.6 SINTn Control

The SINTn pin will set to logic 0 whenever any fault is set in the fault registers. This includes the change of state for the P3 pin. Whenever a fault status bit is set, the SINTn output is logic 0 until all the faults are cleared by FW by writing to the status0 register.

5.7 Temperature Monitoring

The chip has an on-die temperature sensor for thermal protection as well as system warning of impending over-temperature. Upon hitting the EOTW threshold, the chip will set the EOTW bit and pull the SINTn pin low to alert the processor. If the temperature continues to rise above the OT threshold, the chip will shut off the block that causes the OT to allow for cool down. Other blocks will remain in their previous state.

5.8 Thermal Protection

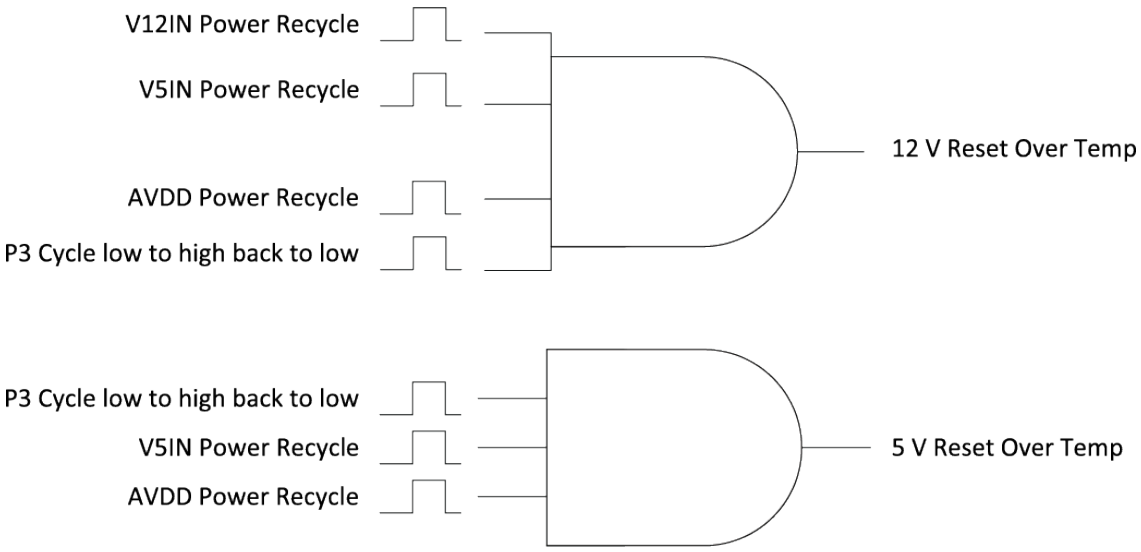
If the temperature of 12 V eFuse hits 175 °C, the eFuse will be latched off. It will remain latched off until one of the following conditions occurs:

- V12IN is cycled high to low and back
- P3 is cycled low to high and back
- V5IN is cycled high to low and back
- AVDD cycles high to low and back

If the temperature of 5 V eFuse hits 175 °C, that eFuse will be latched off. It will remain latched off until until one of the following conditions occurs:

- V5IN is cycled high to low and back
- P3 is cycled low to high and back
- AVDD cycles high to low and back

Figure 6 • Thermal Protection Reset Logic



5.9 EF5ON Control

The EF5ON signal may be used to turn on an external linear regulator when the system is in power backup mode to sustain the voltage of V5OUT rail, and turn off the external regulator when V5IN is above the UVLO threshold and soft start has completed, or when V5IN is above the UVLO threshold and internal reference becomes higher than V5OUT. At input power up, because the external regulator is not active and V5OUT is essentially 0 V, EF5ON is asserted high when V5IN reaches rising UVLO threshold and the internal reference starts ramp up. EF5ON has 1 ms deglitch one-shot delay filter to prevent fast transient from toggling the EF5ON.

5.10 P3 PowerDisable Control

The PowerDisable feature is a hardware-configurable option to be allow firmware to enable or disable the P3 pin function. If the P3FW pin is high, then the P3 pin function can be enabled or disabled from firmware with the P3EN bit.

Table 14 • P3 PowerDisable Control

P3FW	P3EN	P3	12 V 5 V eFuses
0	0	0	Close
0	0	1	Open
0	1	0	Close
0	1	1	Open
1	0	0	Close
1	0	1	Close
1	1	0	Close
1	1	1	Open

5.11 Fault Condition Management

Table 15 • Fault Condition Management

Signals (latched)	Condition/Comment	SIN Tn Pin	5 V eFuse	12 V eFuse	Status Bit Set
V12IN under voltage	This fault asserts when the falling V12IN crosses the falling threshold of UVLO of V12IN.	H => L	Closed	Open	UV12
V5IN under voltage	This fault asserts when the falling V5IN crosses the falling threshold of UVLO of V5IN.	H => L	Open	Closed	UV5
V12IN over voltage	This fault asserts when V12OUT clamping occurs.	H => L	Closed	Closed (V12OUT clamp)	OV12
V5IN over voltage	This fault asserts when V5OUT clamping occurs.	H => L	Closed (V5OUT clamp)	Closed	OV5
V12OUT over current (delay filter ~1.024 ms)	This fault asserts when current limit occurs at 12 V eFuse FET.	H => L	Closed	Enable (I12OUT limit)	OC12
V5OUT over current (delay filter ~1.024 ms)	This fault asserts when current limit occurs at 5 V eFuse FET.	H => L	Enable (I5OUT limit)	Closed	OC5
5 V early over-temperature warning (delay ~32 µs)	This fault asserts when 5 V eFuse temperature crosses the EOTW threshold.	H => L	Closed	Closed	EOTW 5
12 V early over-temperature warning (delay ~32 µs)	This fault asserts when 12 V eFuse temperature crosses the EOTW threshold.	H => L	Closed	Closed	EOTW 12
5 V over temperature	This fault asserts when temperature crosses the OT threshold.	H => L	Open	Closed	OT5
12 V over temperature	This fault asserts when temperature crosses the OT threshold.	H => L	Closed	Open	OT12

Signals (latched)	Condition/Comment	SIN Tn Pin	5 V eFuse	12 V eFuse	Status Bit Set
P3 pin logic 1 (feature enabled)		H => L	Open	Open	P3STATE

5.12 Power Sequence of the 12 V and 5 V eFuse

The eFuse12 and eFuse5 are powered independently from the V12IN and V5in inputs, respectively. The eFuse12 will close and open with V12IN input above or below its eFuse 12 close/open threshold. Similarly, the eFuse 5 will close and open with V5IN input above or below its close/open threshold.

The on states of the 12 V and 5 V e-Fuse in the following table are established when the 12 V input or 5 V input rises above their UVLO threshold, respectively, and AVDD has risen above its UVLO threshold, and P3FW is not active (low state). When P3FW is high and the P3EN bit is low (default value), the P3 power disable function is disabled and the power-up status is not dependent on P3.

Table 16 • eFuse Status when P3FW Is Inactive

V12IN	V5IN	P3	EF12-State	EF5-State
On	On	Low	On	On
Off	On	Low	Off	On
On	Off	Low	Off	Off
Off	Off	Low	Off	Off
On	On	High	Off	Off
Off	On	High	Off	Off
On	Off	High	Off	Off
Off	Off	High	Off	Off

5.13 I2C SCL and SDA Pin Requirements

The power supply for the external pull up resistors attached to the SCL and SDA pins is assumed to be at 1.8 V, but the sequencing relative to the internal digital block power supply can occur at any time before or during startup or power down or any time in between. If the power supply drops below 1.8 V logic level thresholds tolerance value (–10%), then I^2C communication can be interrupted. The default register value loading of all I^2C registers must be be independent on the SCL/SDA state since this is not known.

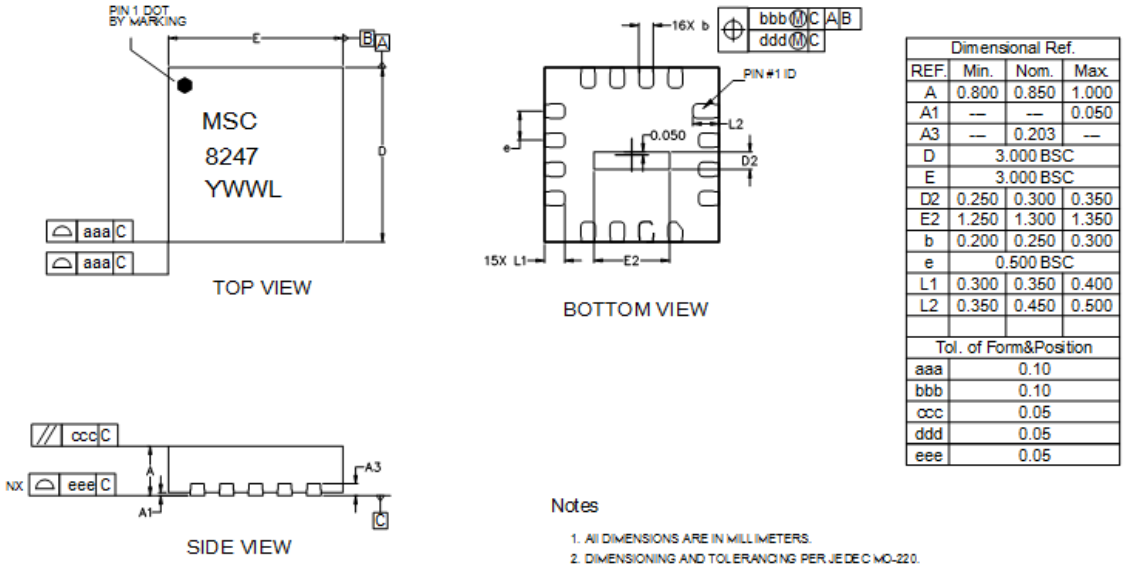
6 Package Specification

The following information describes the package specification of the LX8247 device.

6.1 Package Outline Dimensions

The following illustration shows the package outline dimensions.

Figure 7 • Package Outline Dimensions



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	1.000
A1	---	---	0.050
A3	---	0.203	---
D	3.000 BSC		
E	3.000 BSC		
D2	0.250	0.300	0.350
E2	1.250	1.300	1.350
b	0.200	0.250	0.300
e	0.500 BSC		
L1	0.300	0.350	0.400
L2	0.350	0.450	0.500
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		
eee	0.05		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

7 Ordering Information

The following table lists ordering information for the LX8247 device.

Table 17 • Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
–40 °C to 85 °C	Smart E-Fuse PMIC, 12 V E-Fuse, 5 V E-Fuse	QFN 16L 3.0 mm × 3.0 mm	LX8247ILQ-TR	Tape and reel

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