LX8233
Evaluation Board User Guide

Microsemi
Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in March 2018. It was the first publication of this document.

2 Overview

The LX8233 is a fast-acting, bidirectional eFuse switch designed both to protect circuitry connected to its output (VOUT) from transient input voltage surges on its input (VCC), and to protect VCC from overload current events coming from the load on VOUT. It will also block the reverse discharge current from flowing from VOUT to VCC if the input supply collapses.

Voltage protection features include under-voltage lockout (UVLO) and over-voltage clamping. This clamp limits VOUT voltage allowing continued circuit operation during an input over-voltage transient condition, while UVLO ensures that VOUT remains off until VCC reaches its minimum operating threshold. On the current side, the LX8233 protects the input from a output short circuit and/or over current condition with a 2.5 A current limit circuit.

Another protection feature is latching thermal shutdown of VOUT, with a fault flag output on the combined EN/FAULT pin. Once thermal shutdown threshold is reached and the eFuse switch opens, the tristate EN/FAULT pin will be pulled to about 1.6 V signaling to the system and potentially other connected eFuse switches that a fault has occurred. The LX8233 latches at this level until reset by the Enable pin, DEVSLP pin, or there is a VCC power recycle.

At device power-up the user can initialize the DevSleep pin functionality and VOUT slew rate in one of two modes depending on the state of the FET_ON pin. In DevSleep Disabled mode, the slew rate is set to 13 ms, and VOUT shutdown is engaged when the DEVSLP pin is toggled high regardless of the state of the FET_ON pin. In DevSleep Enabled mode, the slew rate is reduced to 1.4 ms, and shutdown is engaged when the DEVSLP pin is toggled high and the FET_ON pin is low.

2.1 Features

- 50 mΩ (typical) Rdson Internal eFuse FET protected from 15 V
- Bi-directional current blocking switch
- SATA DevSleep support
- SAS-DISABLE support
- Up to 15 V transient input range
- 6 V output voltage clamp
- Continuous operation during VCC surge
- Current limit at overload and short-circuit protection
- Over-temperature protection
- Selectable soft-start 13 ms or 1.4 ms rise time
- UVLO detection
- VQFN 2 mm x 3 mm 13L package

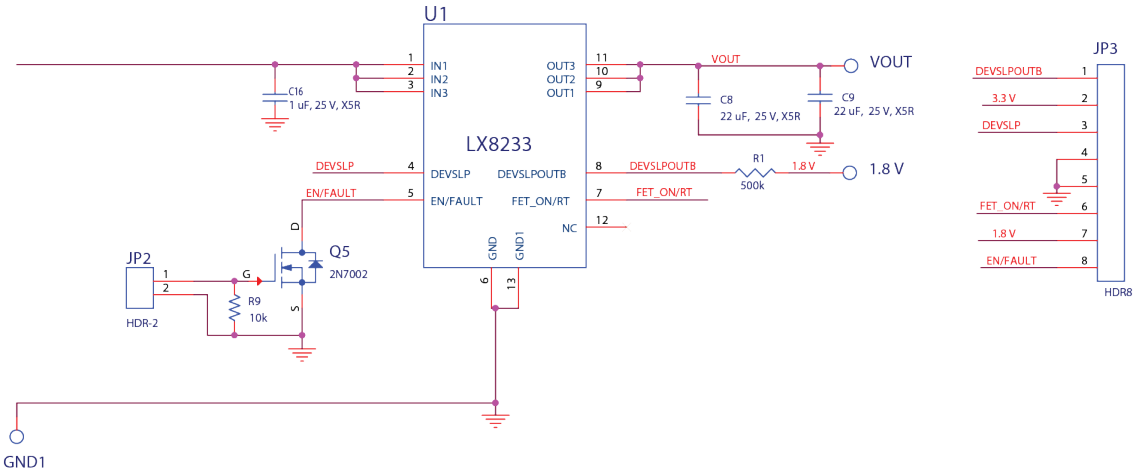
2.2 Applications

- Hard-disk drive
- Solid-state drive
- Hot swap
- PC cards

2.3 Evaluation Board Schematic

The following schematic shows the LX8233 evaluation board.

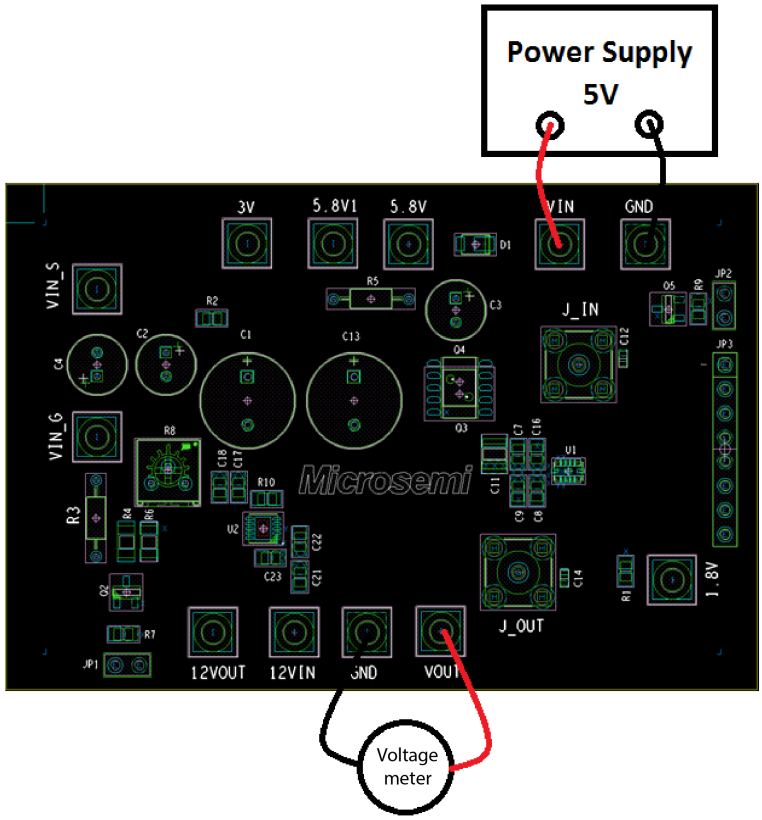
Figure 1 • Evaluation Board Schematic



2.4 Basic Power Supply Connection

The following illustration shows the basic power supply connection instructions for the LX8233 evaluation board.

Figure 2 • Basic Power Supply Connection



2.5 Recommended Operating Conditions

The following table lists the recommended operating conditions for the LX8233 evaluation board.

Table 1 • Recommended Operating Conditions

Description	Symbol	Min	Max	Unit
Input voltage	VCC	4.2	5.75	V
Input current	I_{VCC}		2.5	A
Junction temperature	T_J	–40	125	°C

3 PCB Layout of Evaluation Board

The following images show the PCB layout of the LX8233 evaluation board.

Figure 3 • Top Silkscreen

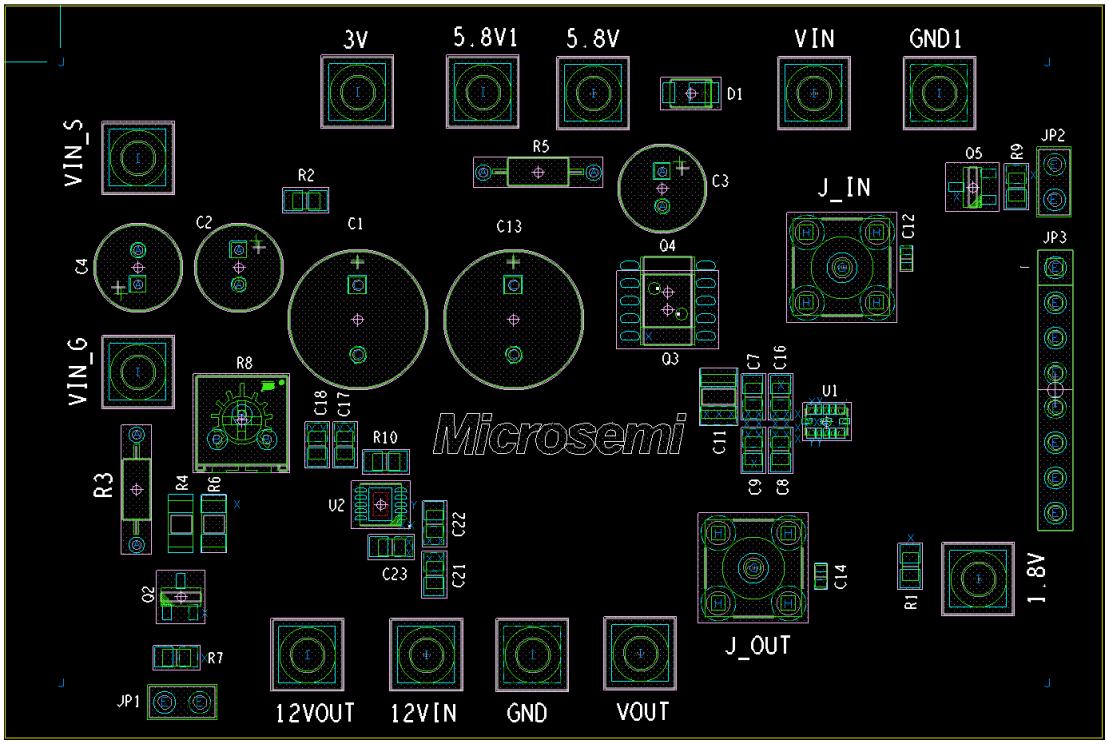


Figure 4 • Top Layer

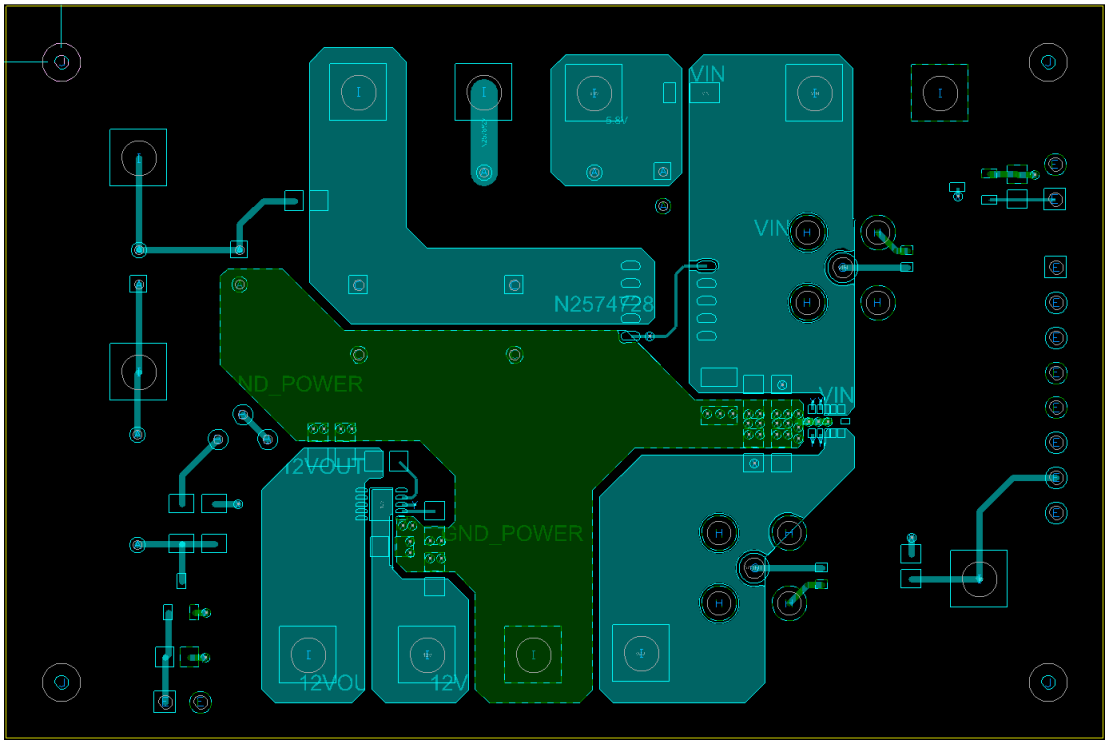


Figure 5 • Ground Layer

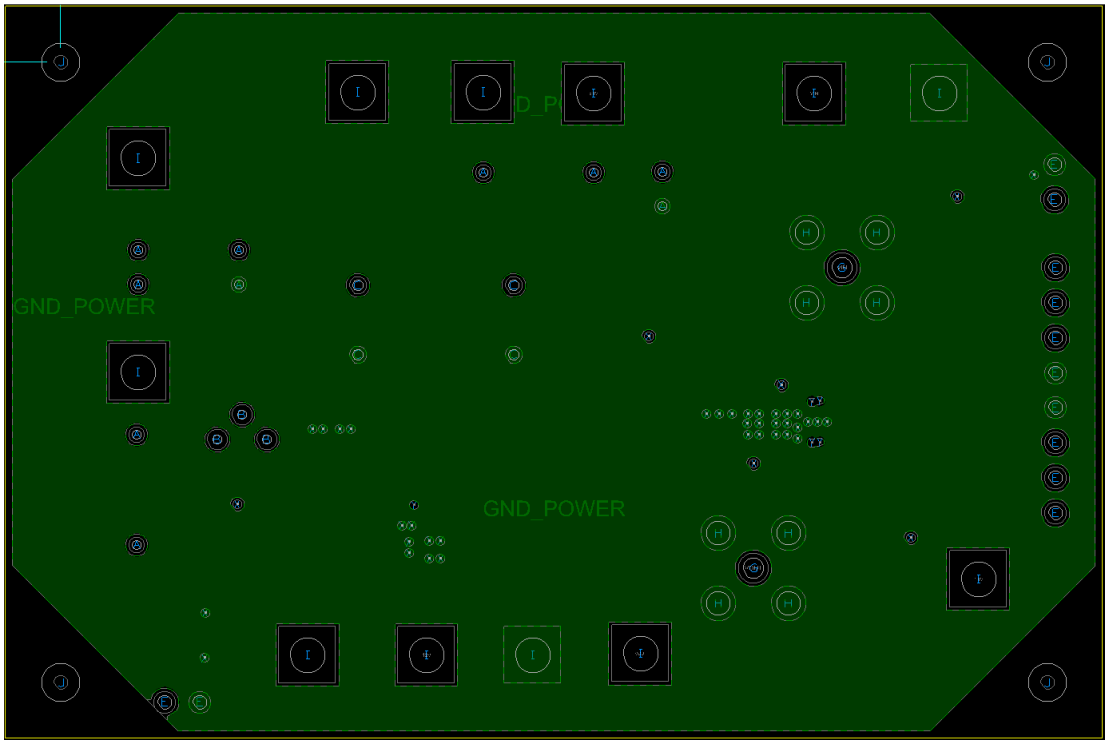


Figure 6 • Power Layer

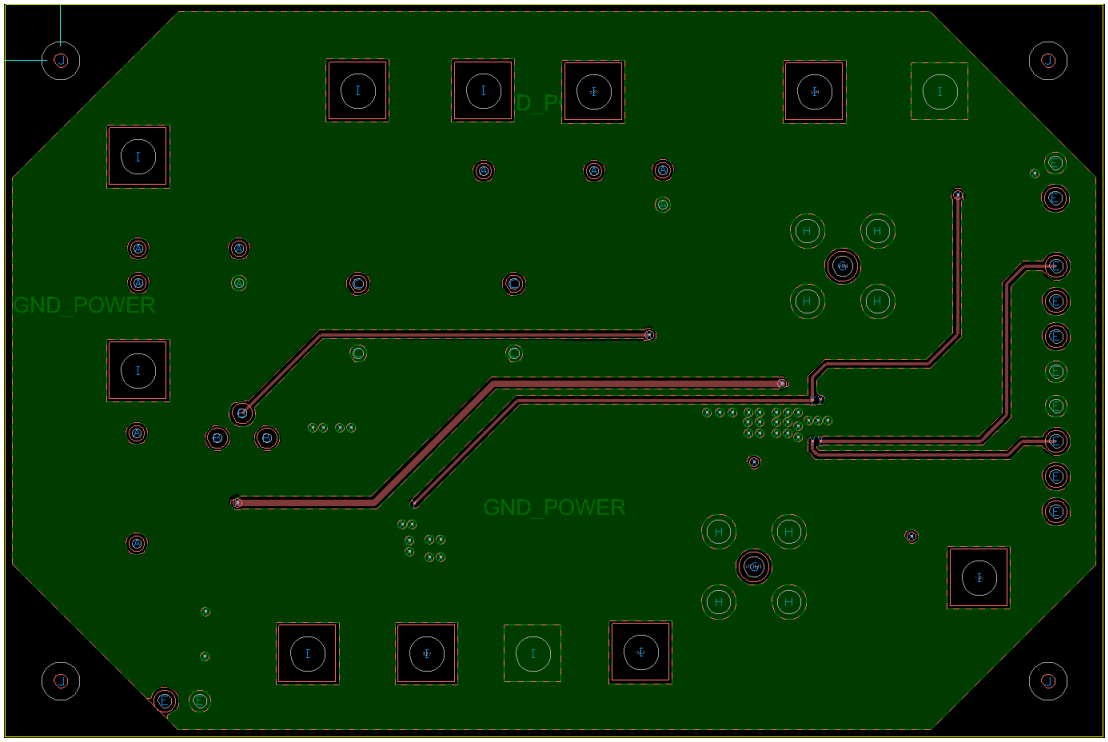
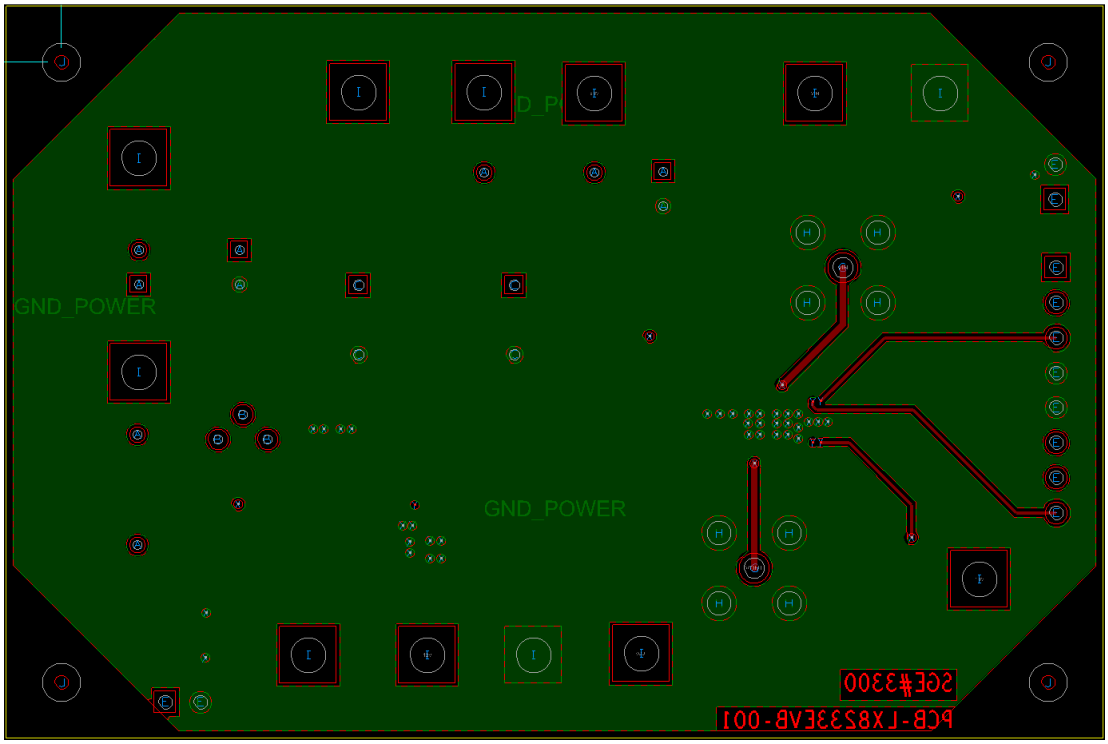


Figure 7 • Bottom Layer



4 Bill of Materials

The following tables describe the bill of materials for the LX8233 device.

Table 2 • Miscellaneous Components

Part Number	Reference	Quantity
Microsemi IC—LX8233ILQ	U1	1

Table 3 • Capacitors

Part Number	Reference	Quantity
22 µF/25 V/X5R	C8, C9	2
1 µF/25 V/X5R	C16	1
22 µF/6.3 V/X5R	C9	1

Table 4 • Resistors

Part Number	Reference	Quantity
500 kΩ	R1	1
10 kΩ	R9	1

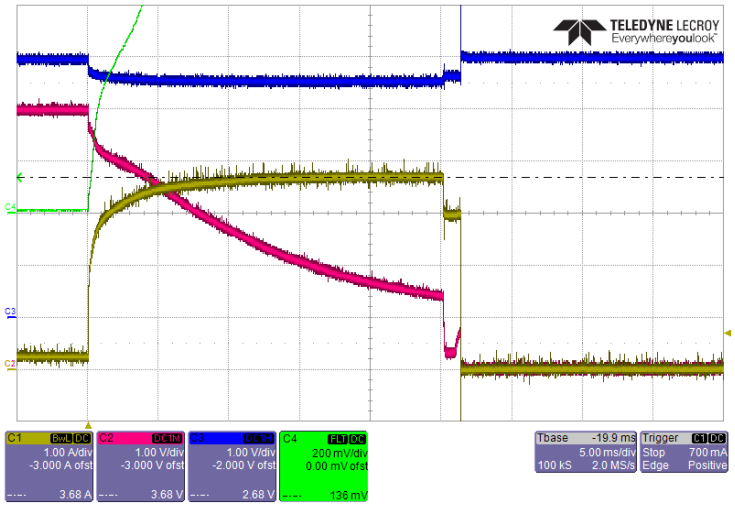
Table 5 • Miscellaneous Components

Part Number	Reference	Quantity
2N7002	Q5	1

5 Scope Images

The following image shows ILIM and SC LIM.

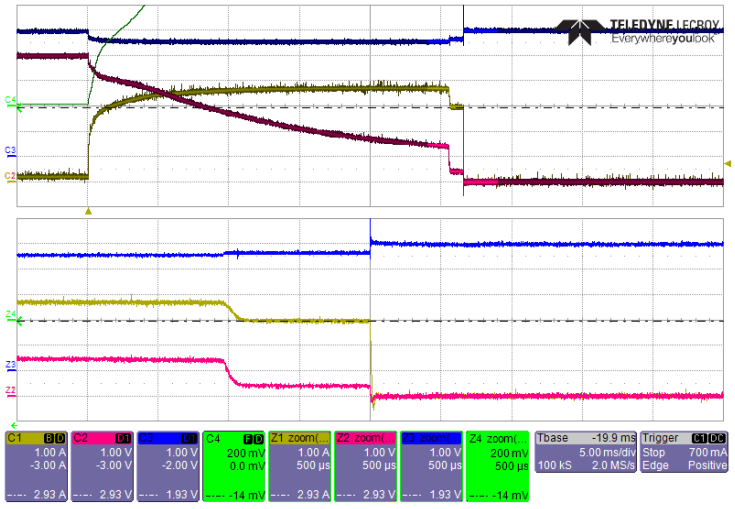
Figure 8 • OC/SC Limit



CH3 (BLU): VIN
CH2 (RED): VOUT
CH1 (YEL): Output current
CH4 (GRN): VIN - VOUT

The following image shows SC LIM before thermal shutdown.

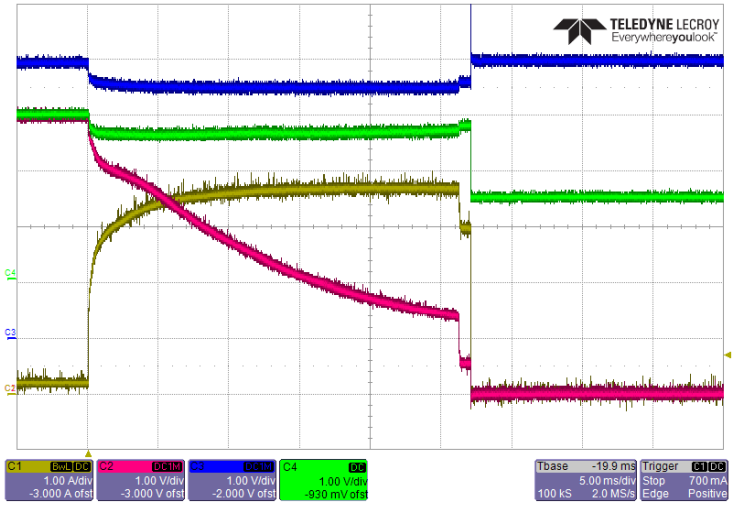
Figure 9 • SC LIM Before Thermal Shutdown



CH3 (BLU): VIN
CH2 (RED): VOUT
CH1 (YEL): Output current
CH4 (GRN): VIN - VOUT

The following image shows SC LIM and EN/Fault pin at thermal shutdown.

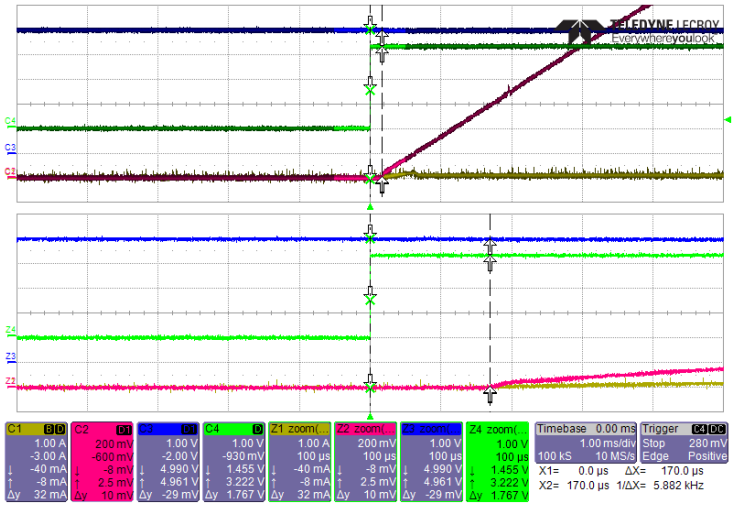
Figure 10 • SC LIM and EN/Fault Pin at Thermal Shutdown



CH3 (BLU): VIN
CH2 (RED): VOUT
CH1 (YEL): Output current
CH4 (GRN): EN/Fault

The following image shows turn on from Fault/Enable.

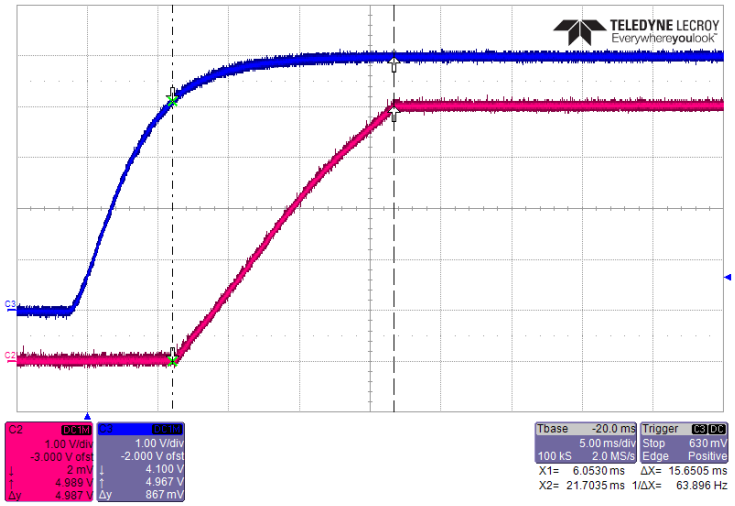
Figure 11 • Turn-on Delay



CH2 (RED): VOUT
CH3 (BLU): VIN
CH4 (GRN): Enable

The following image shows the soft start rise rate with FETON/RT floating at start.

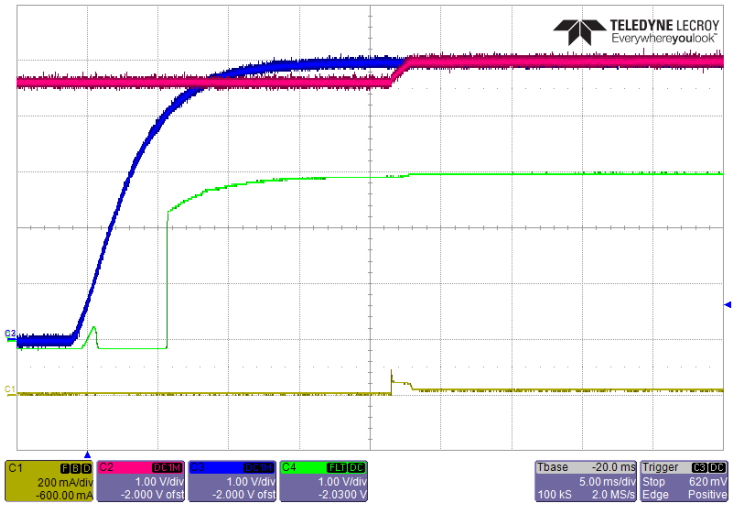
Figure 12 • Soft Start Rise



CH3 (BLU): VIN
CH2 (RED): VOUT

The following images shows the pre-bias start, VIN > VOUT.

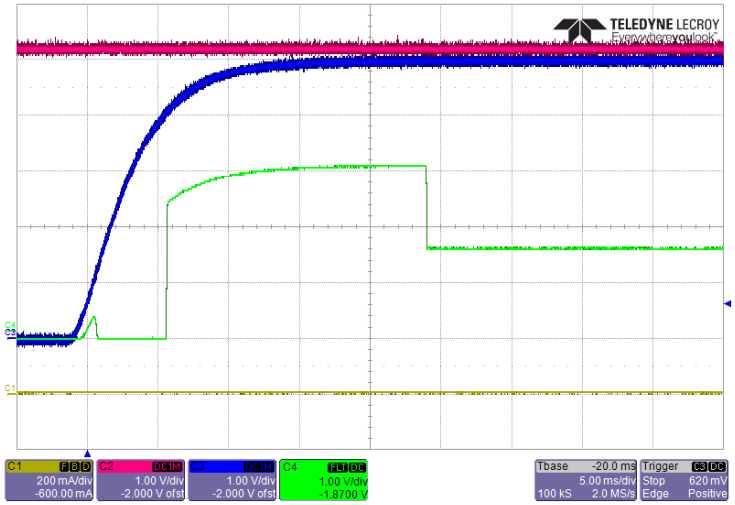
Figure 13 • Start Fault Logic



CH3 (BLU): VIN
CH2 (RED): VOUT
CH4 (GRN): Fault/Enable
CH1 (YEL): VIN current

The following image shows the pre-bias start, Vin < VOUT.

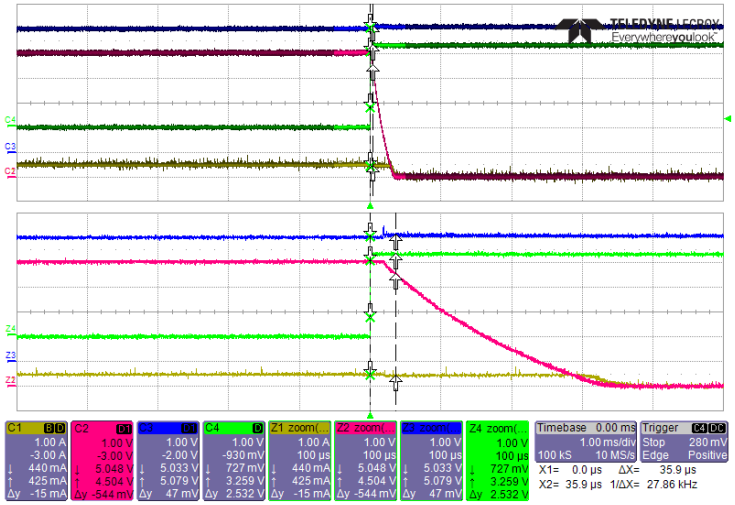
Figure 14 • VIN < VOUT



CH3 (BLU): VIN
CH2 (RED): VOUT
CH4 (GRN): Fault/Enable
CH1 (YEL): VIN current

The following image shows DEVSLP delay to turn off.

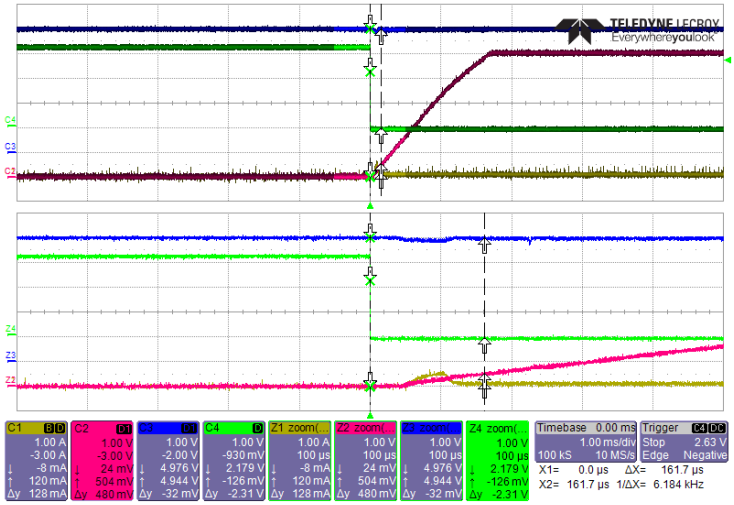
Figure 15 • DEVSLP Delay to Turn Off



CH4 (GRN): DEVSLP signal
CH2 (RED): VOUT
CH3 (BLU): VIN

The following image shows DEVSLP delay to turn on.

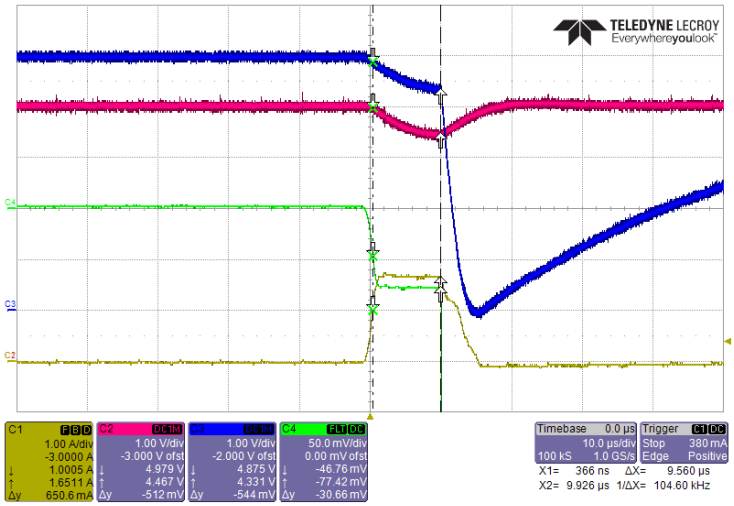
Figure 16 • DEVSLP Delay to Turn On



CH4 (GRN): DEVSLP signal
CH2 (RED): VOUT
CH3 (BLU): VIN

The following image shows a 1.7 A reverse current pulse.

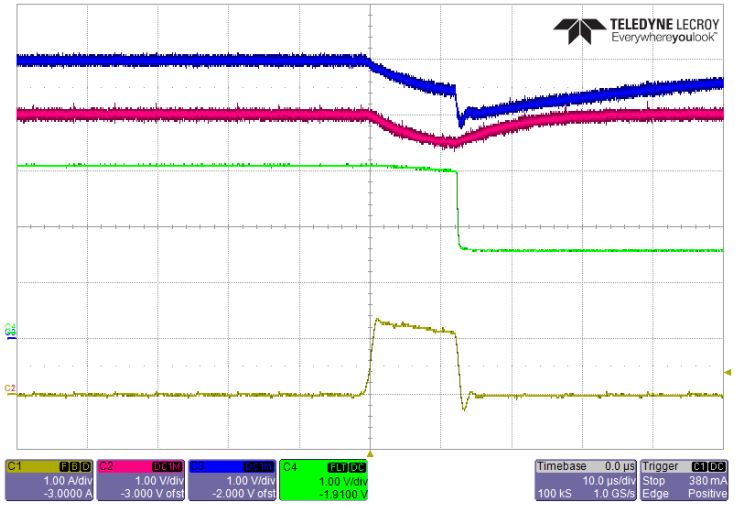
Figure 17 • Reverse Current Detection



CH1 (YEL): Reverse current
CH3 (BLU): VIN
CH2 (RED): VOUT
CH4 (GRN): VIN - VOUT

The following image shows the reverse current pulse and EN/Fault pin.

Figure 18 • Reverse Current Pulse and EN/Fault Pin



CH1 (YEL): Reverse current
CH3 (BLU): VIN
CH2 (RED): VOUT
CH4 (GRN): EN/Fault

6 Ordering Information

The following table lists the ordering information for the LX8233 device.

Table 6 • Ordering Information

Part Number	Description
LX8233ILQ	VQFN 2 mm x 3 mm 13L
LX8233 Evaluation Board	Evaluation PCB for LX8233ILQ

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

MSCC-0236-UG-01001-1.0-0318