LX8233

Datasheet

2.5 A 5 V eFuse with Bidirectional Protection Switch and DevSleep/Disable Mode

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in February 2018. It was the first publication of this document.

2 Product Overview

The LX8233 is a fast-acting, bidirectional eFuse switch designed to protect circuitry connected to its output (VOUT) from transient input voltage surges on its input (VCC) and to protect VCC from overload current events coming from the load on VOUT. It will also block the reverse discharge current from flowing from VOUT to VCC if the input supply collapses.

Voltage protection features include under-voltage lockout (UVLO) and over-voltage clamping. This clamp limits VOUT voltage, allowing continued circuit operation during an input over-voltage transient condition, while UVLO ensures that VOUT remains off until VCC reaches its minimum operating threshold. On the current side, the LX8233 protects the input from a output short circuit and/or over-current condition with a 2.5 A current limit circuit.

Another protection feature is latching thermal shutdown of VOUT, with a fault flag output on the combined EN/FAULT pin. Once the thermal shutdown threshold is reached and the eFuse switch opens, the tristate EN/FAULT pin will be pulled to about 1.6 V signaling to the system and potentially other connected eFuse switches that a fault has occurred. The LX8233 latches at this level until reset by the Enable pin or DEVSLP pin, or there is a VCC power recycle.

At device power-up, the user can initialize the DevSleep pin functionality and VOUT slew rate in one of two modes depending on the state of the FET_ON pin. In DevSleep Disabled mode, the slew rate is set to 13 ms, and VOUT shutdown is engaged when the DEVSLP pin is toggled high regardless of the state of the FET_ON pin. In DevSleep Enabled mode, the slew rate is reduced to 1.4 ms, and shutdown is engaged when the DEVSLP pin is toggled high and the FET_ON pin is low.

2.1 Features

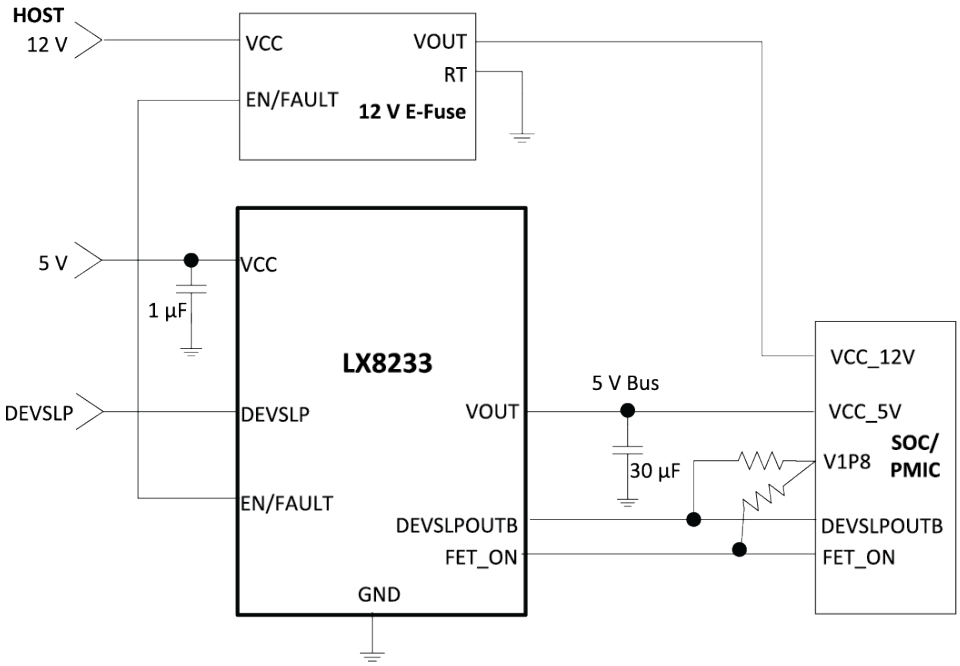
- 50 mΩ (typical) Rdson Internal eFuse FET protected from 15 V
- Bi-directional current blocking switch
- SATA DevSleep support
- SAS-DISABLE support
- Up to 15 V transient input range
- 6 V output voltage clamp
- Continuous operation during VCC surge
- Current limit at overload and short-circuit protection
- Over-temperature protection
- Selectable soft-start, 13 ms or 1.4 ms rise time
- UVLO detection
- VQFN 2 mm x 3 mm 13L package

2.2 Applications

- Hard-disk drive
- Solid-state drive
- Hot swap
- PC cards

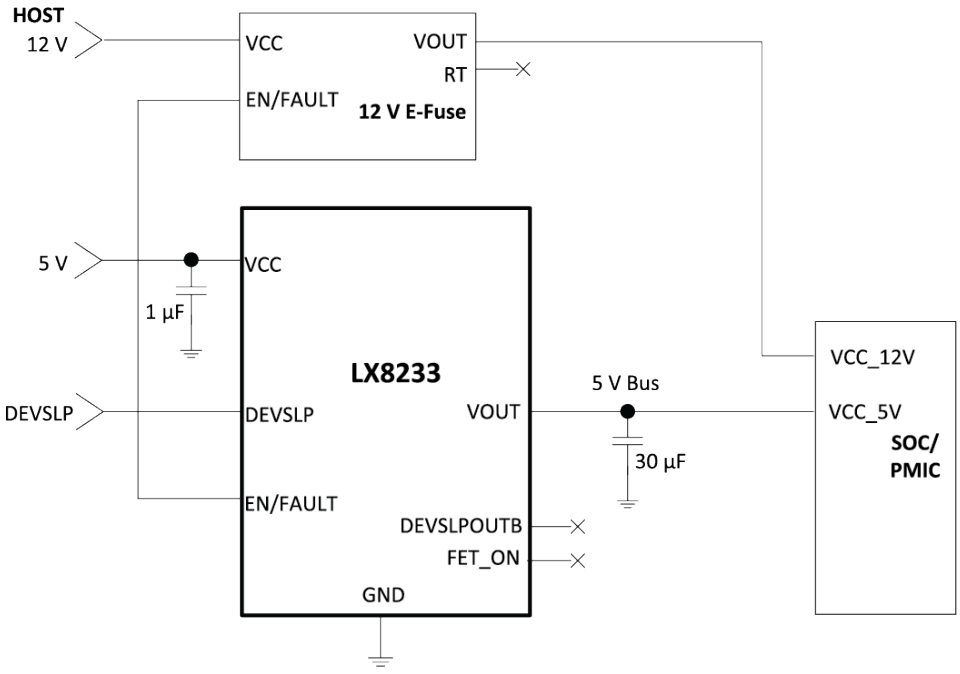
The following illustration shows a typical application of LX8233, DevSleep Enable mode.

Figure 1 • DevSleep Enable Mode



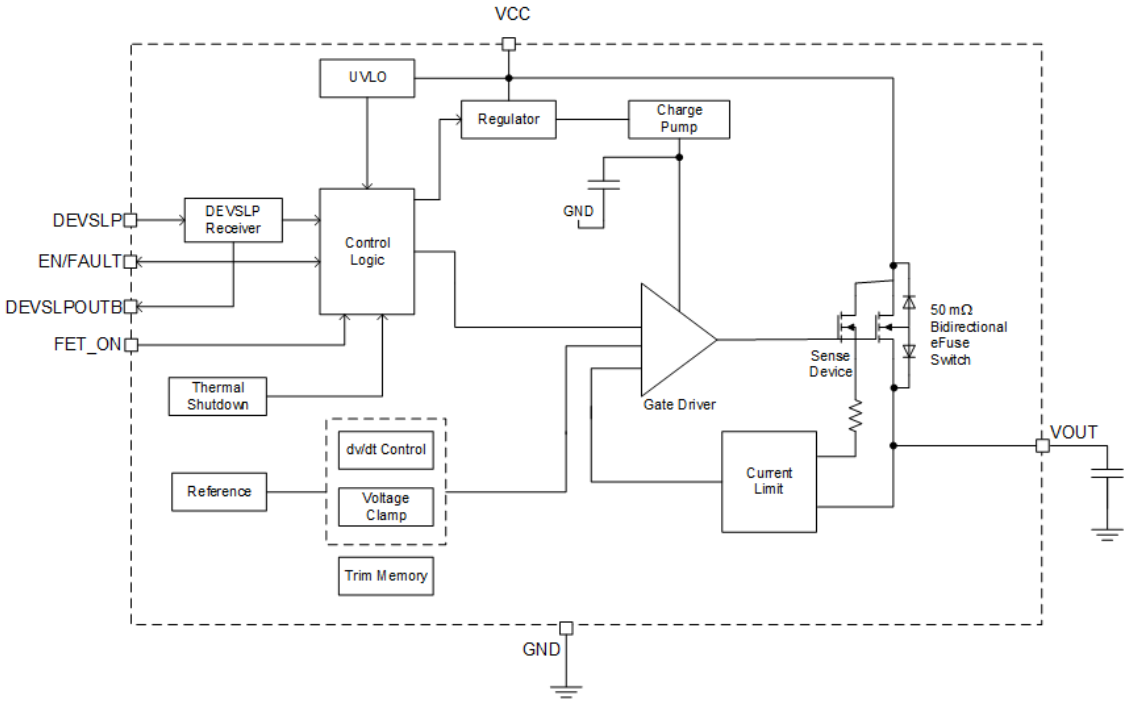
The following illustration shows a typical application of LX8233, DevSleep Disable mode.

Figure 2 • DevSleep Disable Mode



The following illustration shows a simplified block diagram of the LX8233 device.

Figure 3 • Block Diagram

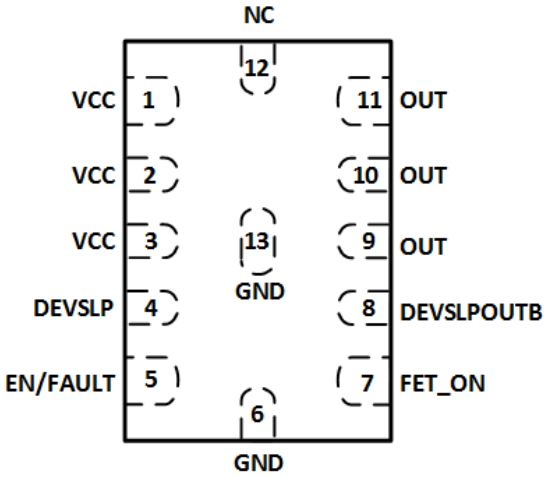


3 Pin Descriptions

The following section describes the pins of the LX8233 device.

The following illustration shows the top view of the pinout for the LX8233 device.

Figure 4 • Pinout VQFN 2 mm × 3 mm 13L



Note: Line: 1 MSC. Line 2: 8233. Line 3: Date/Lot code.

The following table describes the pins of the LX8233 device.

Table 1 • Pin Descriptions

Pin Number	Pin Name	Input /Output	Description
1, 2, 3	VCC	Input	Input of the device.
4	DEVSLP	Input	DevSleep mode input. The following two modes are for the usage of DEVSLP. For more information, see Summary of DEVSLP Disabled vs. Enabled (see page 6). **DEVSLP Enable Mode**—selected by connecting the FET_ON pin of LX8233 to SOC during power on initalization. In this mode, only when FET_ON is low will setting DEVSLP high shut down the LX8233. This handshake feature allows the SOC to override the shutdown process initiated by the host using DevSleep, allowing any necessary housekeeping functions to complete before powering off the switch. In this mode, the VOUT softstart time is programmed to 1.4 ms. **DEVSLP Disabled Mode**—selected by letting FET_ON pin float during power on initalization. In this mode, the LX8233 will shutdown by setting DEVSLP high regardless of the FET_ON state. In this mode, the VOUT softstart time is programmed to 13 ms.

Pin Number	Pin Name	Input /Output	Description
5	EN/FAULT	Input /Output	The EN/FAULT pin is a tri-state, bidirectional interface. It can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state (~1.6 V) to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events. The EN/FAULT pin will stay high current soft start conditions. See simplified schematic in Theory of Operation/ Application section.
6	GND		Ground pin (pin 6 and pin 13 are internally connected).
7	FET_ON	Input	DEVSLP mode is configured by the FET_ON state during power on initializaiton. When FET_ON is floating (50 pf maximum pin capacitance), the LX8233 is set to DEVSLP Disabled mode. In this mode, the LX8233 can be shut down by setting the DEVSLP pin high. When FET_ON is connected to SOC, the LX8233 can only be shut down by setting both DEVSLP high and FET_ON low.
8	DEVSLPOUTB	Output	Open-drain output. A pull-up resistor is connected to the I/O supply of SOC. DEVSLPOUTB is the inversed polarity version of DEVSLP.
9, 10, 11	VOUT	Output	Output of the device, connect to circuitry to be protected. A 10 uF capacitor is needed for over voltage protection stability. The capacitor return should be connected directly to the GND pin.
12	NC		Do not connect.
13	GND		Ground pin (pin 6 and pin 13 are internally connected).

The following table summarizes DEVSLP Disabled vs. Enabled modes.

Table 2 • Summary of DEVSLP Disabled vs. Enabled

Mode	FET_ON	T_{RISE}	Shutdown
DEVSLP Disabled	Float	~13 ms	DEVSLP High
DEVSLP Enabled	Connected to SOC	~1.4 ms	(DEVSLP High) AND (FET_ON Low)

4 Electrical Specifications

The following section describes the electrical specifications of the LX8223 device.

4.1 Absolute Maximum Ratings

Table 3 • Absolute Maximum Ratings

Parameter	Min	Max	Units
VCC to GND (steady state)	–0.3	15	V
VCC to GND (transient 100 ms)	–0.3	15	V
VOUT to GND (steady state)	–0.3	6.5	V
VOUT to GND (transient 100 ms)	–0.3	7	V
EN/FAULT to GND	–0.3	≤VCC	V
EN/FAULT to GND	–0.3	6	V
DEVSLPOUTB to GND	–0.3	6	V
DEVSLP to GND	–0.3	3.6	V
FET_ON to GND	–0.3	3.6	V
ESD (human body model)	2000		V
ESD (charged device model)	1000		V
Power dissipation		1.3	W
Storage temperature	–65	150	°C

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

4.2 Operating Ratings

The following table describes the operating ratings of the LX8233 device.

Table 4 • Operating Ratings

	Min	Max	Units
VCC	4.2	5.75	V
I(VCC)		2.5	A
Junction temperature	–40	125	°C

Note: Performance is generally guaranteed over this range, as further detailed in Electrical Specifications .

4.3 Thermal Properties

The following table describes the thermal properties of the LX8233 device.

Table 5 • Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	40	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

4.4 Electrical Characteristics

The following specifications apply over the operating ambient temperature of –40 °C ≤ T_A ≤ 85 °C except where otherwise noted with the following test conditions: VCC = 5 V. Typical parameter refers to T_J = 25 °C.

Table 6 • eFuse FET

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
T_{ONDLY}	Turn-on delay time	Enable by EN/FAULT with load current 100 mA.		80		µs
R_{DSON}	On resistance	T_A = 25 °C (Note 2)		50		m?
		T_J = 80 °C (Note 1)		95		m?
I_{OFF}	Off state output leakage current	VCC = 5 V_{DC}, EN/FAULT = GND, VOUT = GND Measure I(VOUT)			2.9	µA
I_{DC}	Continuous current	T_A = 25 °C		2		A
T_{RISE}	VOUT rise time	FET_ON = Float (assumes 12 V eFuse will be at maximum rise rate of 15.6 ms)	12.5	14	15.6	ms
		FET_ON = GND		1.4		ms

Table 7 • Thermal Shutdown

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
T_{SD}	Shutdown temperature	VOUT is latched off once thermal shutdown is triggered. It can be reset three ways. 1) EN/FAULT is pulled low then let float. 2) DEVSLP pin is toggled high then low. 3) VCC is recycled.		135		°C

Table 8 • Under/Over Voltage Protection

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
V_{CLAMP}	Output clamping voltage	VCC= 10 V	5.75		6.25	V
	Maximum overshoot during transient	VCC transient from 5 V to the higher than 12 V at 100 V/µs with I_{VOUT} = 0 A. C_{OUT}= 33 uF			6.5	V
	Minimum undershoot during transient	VCC transient from 5 V to the higher than 12 V at 100 V/µs with I(VOUT)= 2.5 A. C_{OUT}= 33 uF	4.5			V
V_{UVLO_TH}	Under-voltage lock-out threshold	Turn-on and voltage increases	3.75		4.2	V
V_{UVLO_HYS}	Under-voltage lock-out hysteresis			0.3		V
	Under-voltage lock-out response time			2		µs

Table 9 • Current Protection

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
I_{SC_LIM}	Short circuit current limit	VOUT is <1 V from GND		2.5		A
I_{AVG_LIM}	Overloading current limit	VOUT is 0.5 V lower than the nominal VOUT	2.5	3		A

Table 10 • Reverse Current Detection

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
$I_{REVERSE}$	Reverse current limit	Temperature range –40 °C to 85 °C	0.5		1.4	A
		Temperature range 0 °C to 85 °C	0.6		1.3	A
$T_{REVERSE}$	Reverse current limit response time	(Note 1)	5		10	µs

Table 11 • DEVSLP

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
DEVSLP $_{TH}$	Logic input threshold	Measure the threshold	0.8		2.0	V
DEVSL P $_{HYS}$	Logic input hysteresis	Measure the threshold of DEVSLP		190		mV

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
$DEVSLP_{MAX}$	Maximum DEVSLP pin voltage	Design target. No test.			3.3	V
DEVSLP-WIN	Input impedance	Output enable, unconnected pin = enable. Internal pull-down resistor test. Measure the impedance from DEVSLP to GND.	350	500	1000	kW
DEVSLP-OFF-TDLY	Turn-off deglitch delay	100 mA VOUT load. Logic Turn off by changing DEVSLP from 0 V to 5 V. Measure the delay from the edge of DEVSLP to 4.5 V (the 10% lower to 5 V VOUT).	2		50	µs
DEVSLP-ON-TDLY	Turn-on deglitch delay	DEVSLP Enabled mode. 100 mA VOUT load. Logic Turn on by changing DEVSLP from 5 V to 0 V. Measure the delay from the edge of DEVSLP to 0.5 V (the 10% of 5 V VOUT).	2		300	µs

Table 12 • EN/FAULT

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
VEN_{DISIL}	Disable logic input level low	Output disabled			0.4	V
VEN_{MIDIL}	Thermal fault input logic level low	EN/FAULT pin is driven by the other eFuse. Thermal fault, output disabled			1.0	V
VEN_{MIDIH}	Thermal fault input logic level high	EN/FAULT pin is driven by the other eFuse. Thermal fault, output disabled	2.1			V
VEN_{ENIH}	Enable logic input level high	Output enabled	3.3			V
	High state max voltage	(Note 1)			5.2	V
VEN_{MIDOL}	Thermal fault output logic level low	LX8233 drives EN/FAULT pin. Thermal fault, output disabled	1.1			V
VEN_{MIDOH}	Thermal fault output logic level low	LX8233 drives EN/FAULT pin. Thermal fault, output disabled			1.9	V
$IIL_{EN/FAULT}$	Logic low input	V_{EN} = GND at the normal operation		10		µA
	Sink current	V_{EN} = GND at the thermal shutdown		20		µA
$IIH_{EN/FAULT}$	Logic high leakage current	V_{EN} = 4.3 V			1	µA

Table 13 • DEVSLPOUTB

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
V_{PGPD}	Pull-down voltage	I_{SINK} = 4 mA, sinking current into DEVSLPOUTB			0.3	V
I_{PGLEAK}	Leakage current	$V_{DEVSLPOUTB}$ = 1.8 V			1	µA

Table 14 • FET_ON

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
	Logic threshold low-to-mid		0.3	0.5	0.7	V
	Logic threshold mid-to-high		0.8	1.0	1.2	V
	Input leakage current	FET_ON = GND			1	µA

For more information on FET_ON, see Note 3.

Table 15 • Total Device

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
I_{Q_OP}	Bias current	Operational		200	250	µA
I_{Q_DIS}		Disable (EN/FAULT = GND or DEVSLP = High)		138		µA
I_{Q_FLT}		Thermal fault latch off		100		µA
V_{MIN}	Minimum operating voltage	(Note 4)			4.2	V
	Reverse bias leakage current	VCC = GND, VOUT = 5 V		17		µA

Note 1: Guaranteed by design.
Note 2: Pulse test. Pulse width= 300 µs, Duty cycle= 2%.
Note 3: Total pin capacitance must be ≤50 pf to be considered floating by the chip.
Note 4: Device may shut down prior to reaching this level based on actual UVLO trip point.

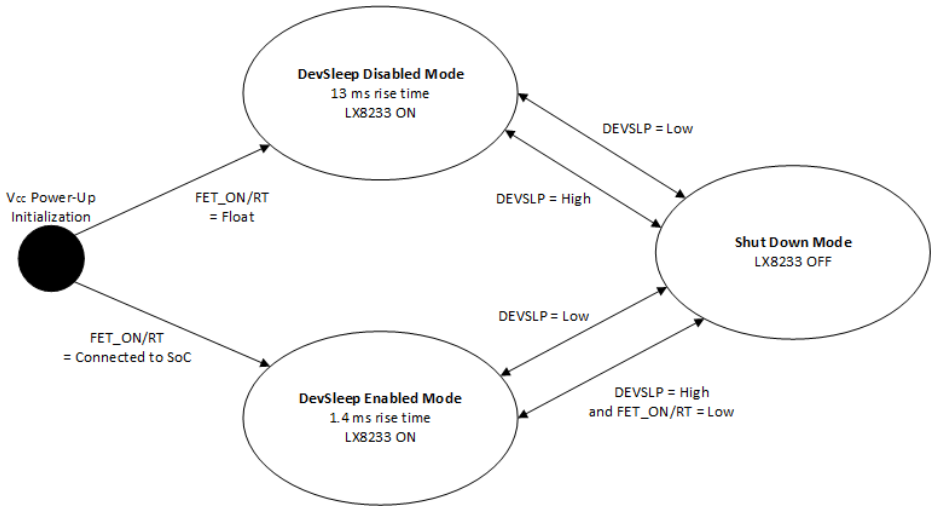
5 Theory of Operation/Application Information

The following section describes the theory of operation and application information for the LX8233 device.

5.1 DevSleep Logic Operation

The following illustration shows DevSleep operation.

Figure 5 • DevSleep Operation



VCC Power-up Initialization: As VCC rises, the LX8233 initializes its internal circuits. Upon reaching the UVLO threshold, the LX8233 also detects the status of FET_ON pin. If FET_ON detects a float condition, it initializes in DevSleep Disabled mode. However, if FET_ON is detected as connected to SOC, then it initializes to DevSleep Enabled mode.

DevSleep Disabled Mode: When VCC reaches the UVLO threshold, VOUT slews for 13 ms from 0 V to VCC. The LX8233 is monitoring the DEVSLP pin and enters Shutdown mode if DEVSLP goes high.

DevSleep Enabled Mode: When VCC reaches the UVLO threshold, VOUT slews for 1.4 ms from 0 V to VCC. In this mode, the LX8233 is monitoring both the DEVSLP and FET_ON pins. When both DEVSLP goes high and FET_ON goes low, LX8233 enters Shutdown mode.

Shutdown Mode: Once LX8233 enters this mode, the chip shuts down VOUT and most internal circuitry, minimizing quiescent current to that required to monitor the DEVSLP pin and maintain state information. When DEVSLP toggles low, the LX8233 restores itself to original DevSleep Disabled/Enabled mode operation mode.

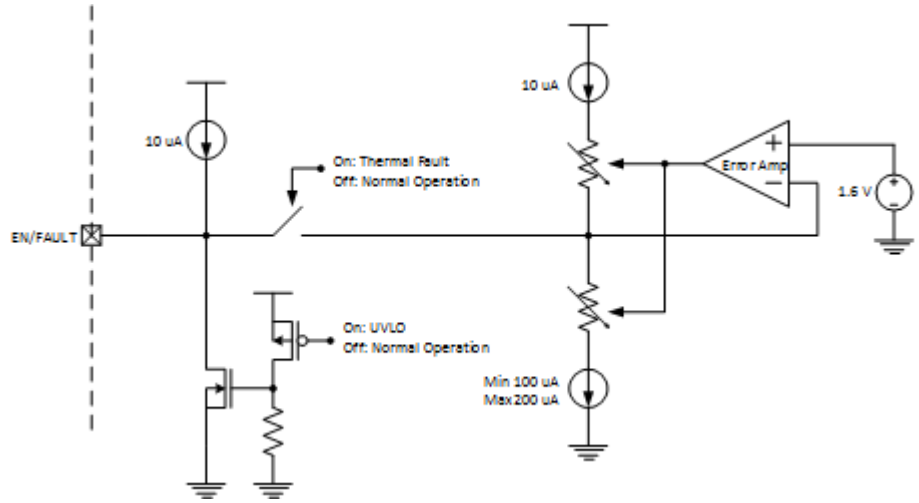
5.1.1 EN/FAULT Operation

The EN/FAULT bidirectional I/O pin is used to synchronize the startup and shutdown the LX8233 with other eFuse devices. When the LX8233 is not in a fault condition, the EN/FAULT pin is pulled up by an internal current. In this condition, the EN/FAULT pin will be pulled to approximately 4.3 V when VCC= 5 V. In cases that the EN/FAULT pin is connected to anther eFuse, as shown in Figure 1, the actual voltage of this pin may vary as a function of the actual voltages and pull-up values of each eFuse.

The EN/FAULT pin can be used to disable the eFuse by pulling the pins' voltage below the VEN_{MIDIH} level.

The EN/FAULT pin is also an FAULT output indicating either a UVLO event, reverse current, over temperature, or a DEVSLP disable event (DEVSLP Disable mode only). In the case of a temperature event, if the IC's junction temperature passes the thermal shutdown threshold, the LX8233 will pull down the EN/FAULT pin to the mid-level fault logic condition. As shown in the following simplified schematic, an internal switch (thermal latch) engages at thermal shutdown driving the EN/FAULT pin to approximately 1.6 V with pulldown capability to drive several parallel connected devices. Thus, if LX8233 reaches thermal shutdown, it will latch off all the parallel connected devices on the same node. It remains at 1.6 V until either the Enable pin is pulled low then left to float, the DEVSLP pin is toggled (high then low, or low to high), or there is a VCC power recycle.

Figure 6 • Simplified EN/FAULT Circuitry



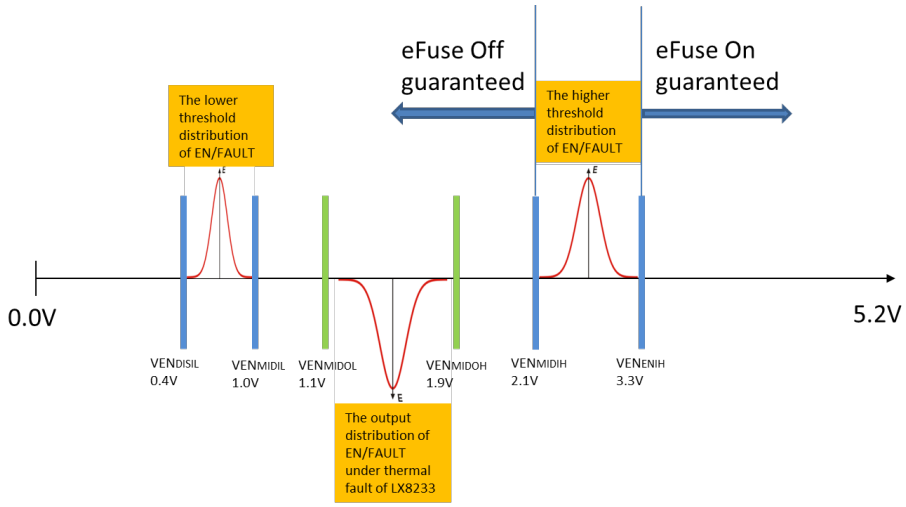
The following table specifies the EN/FAULT pin voltage for each type of shutdown. 1= Pullup, mid= mid voltage, and 0= pulled low.

Table 16 • EN/FAULT Pin Logic

IReverse	UVLO	DEVSLP	THERM	ENABLE
0	0	0	0	1
0	0	0	1	mid
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	mid
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

The following image shows eFuse on and off ranges and the thermal fault range.

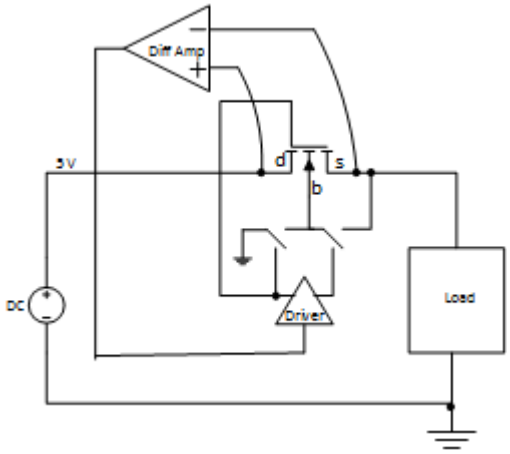
Figure 7 • eFuse On and Off Ranges and Thermal Fault Range



5.2 Reverse Current Protection

While the simplest protection against a reverse current condition may be a diode in-series connection to the load, this method has drawbacks. There is significant power loss in the forward conduction mode, as well as poor supply rail regulation. In order to solve this problem, the LX8233 implements a bidirectional voltage and current-blocking FET switch. The basic concept of this method is to detect the polarity of voltage drop through the FET pass device and open up the switch to block reverse current. This method is very effective for fast slew rate of reverse current blocking. If the slew rate of the reverse current is slower than a certain rate (that is, a slowly reducing input voltage), the reverse current will be allowed until the input voltage reaches the UVLO threshold. Below this level, the switch is quickly turned off and blocks reverse current and voltage.

Figure 8 • Simplified Reverse Current Detection Circuitry

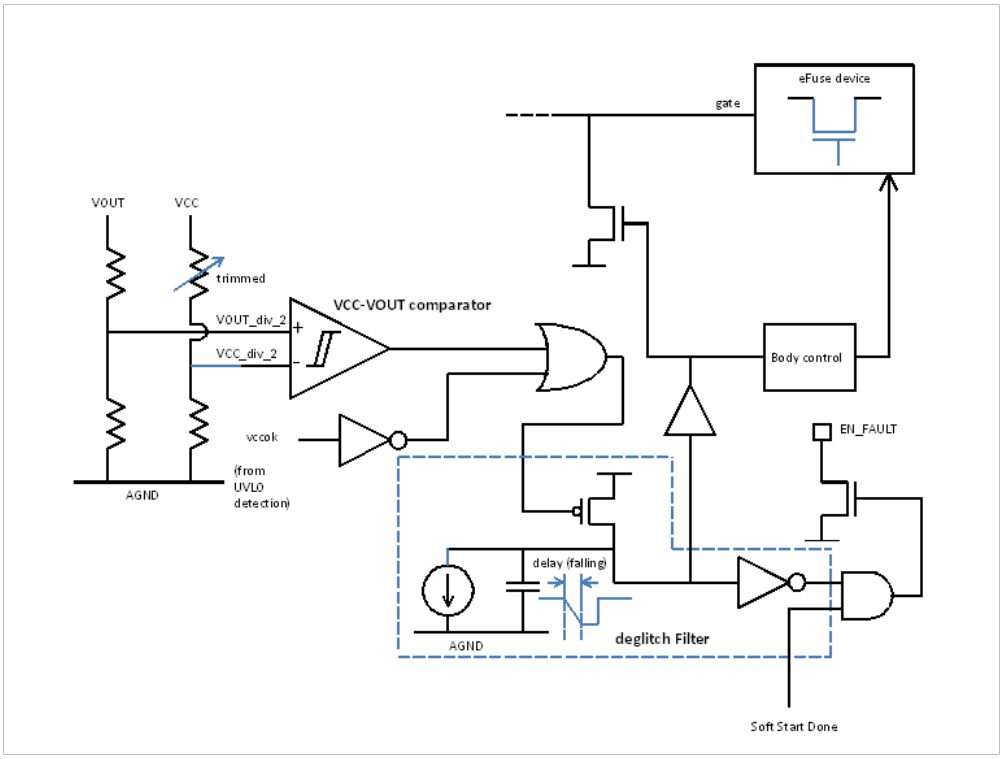


When the reverse current is detected, the eFuse will turn off, the FAULT pin will be triggered, and the soft start reference will be reset.

The detection circuit basic block diagram, shown in the following illustration, comprises a reverse current detector and then a deglitch filter. The reverse current comparator needs to meet the reverse current threshold values over temperature and have a response time of no more than 6.5 us. The deglitch filter has a response of 3.5 uS. The sum of these delays must be bigger than the minimum response time for any value of large reverse currents. This current may be more than 5 A. It must also be less than the maximum response time for at least a range less than the minimum reverse current threshold.

Also as shown in the following illustration, under a soft start, even if the output is greater than the input, the EN/FAULT pin must pulled high by the on board pull-up current.

Figure 9 • Block Diagram of Reverse Current Detection



5.3 Under-Voltage Lock-Out

In LX8233, UVLO plays an important role. It has a high threshold with very little hysteresis and a very fast comparator propagation delay. These features of UVLO circuit maximize the reverse current blocking function capability. This is described in the following table.

Table 17 • UVLO

UVLO	EN/FAULT	DEVSLP	FET_ON	LX8233	DEVSLPOUTB with Pull-up
Violated	*	*	*	Off	Off/High

When the LX8233 input voltage rises above the ULVO threshold, it will start a soft start sequence. During this sequence, the ENABLE must be high. This ensures that a parallel connected eFuse will also be allowed to start.

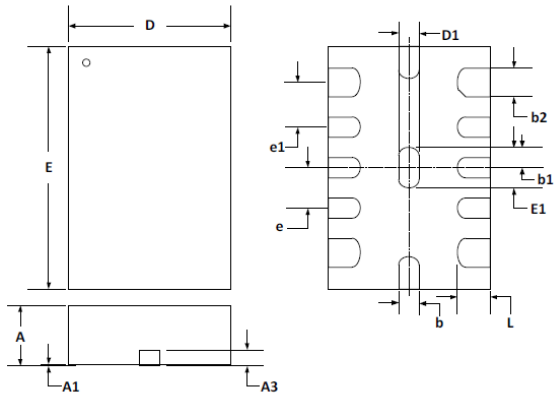
6 Package Specification

The following section describes the package specification for the LX8233 device.

6.1 Package Outline Dimensions

The following illustration shows the package outline dimensions of the LX8233 device.

Figure 10 • LQ 12-Pin VQFN Package Dimensions



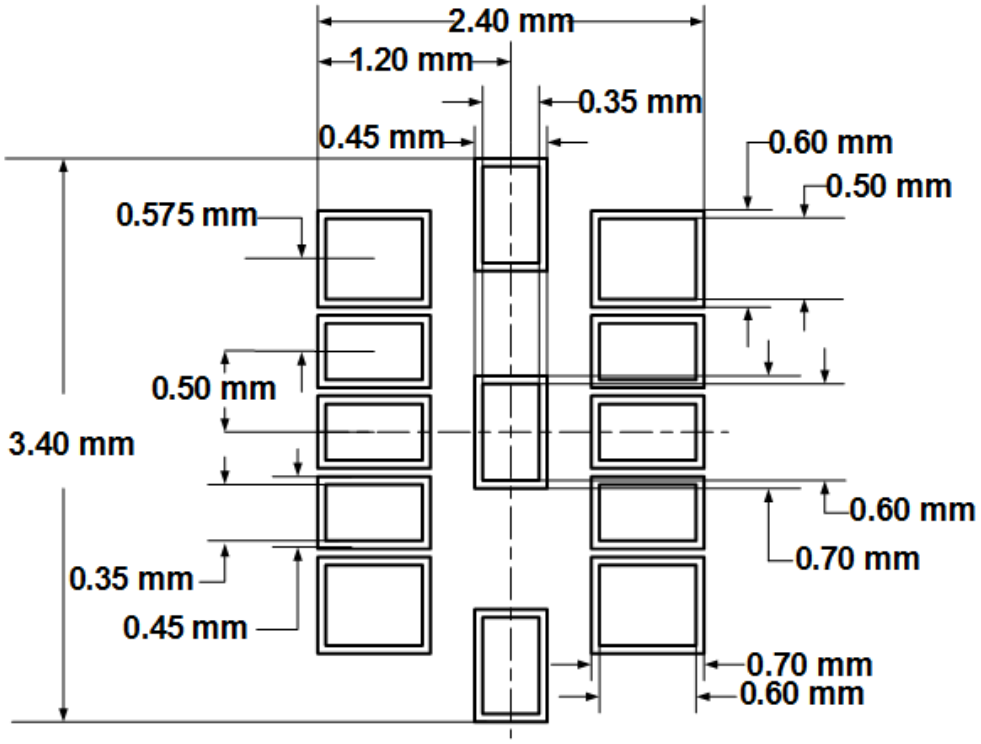
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		1.00		0.039
A1	0.00	0.05	0.000	0.002
A3	0.203 REF		0.008REF	
D	1.95	2.05	0.077	0.081
b	0.20	0.30	0.008	0.012
D1	0.20	0.30	0.008	0.012
L	0.35	0.45	0.014	0.018
E	2.95	3.05	0.116	0.120
e	0.50BSC		0.020BSC	
e1	0.575BSC		0.023BSC	
b1	0.18REF		0.007REF	
b2	0.35	0.45	0.014	0.018
E1	0.38	0.48	0.015	0.019

Note 1: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.
Note 2: Dimensions are in mm, inches are for reference only.

6.2 Land Pattern Recommendations

The following illustration shows the land pattern recommendations for the LX8233 device.

Figure 11 • LQ 12-Pin VQFN Package Land Pattern



Disclaimer: This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly (the end user must account for this in their final layout). Microsemi makes no warranty or representation of performance based on this recommended land pattern.

7 Ordering Information

The following table lists ordering information for the LX8233 device.

Table 18 • Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
–40 °C to 85 °C	RoHS compliant, Pb-free	VQFN 2 mm x 3 mm 13L	LX8233ILQ	Bulk/Tube
			LX8233ILQ-TR	Tape and reel

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