AC468
Application Note
PolarFire FPGA Transceiver Decision Feedback Equalization
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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 3.0
Updated the document for Libero SoC PolarFire v2.3.

1.2 Revision 2.0
Updated the document for Libero SoC PolarFire v2.2.

1.3 Revision 1.0
The first publication of this document.
2 PolarFire FPGA Transceiver Decision Feedback Equalization

The PolarFire® FPGA family includes multiple embedded low-power, performance-optimized transceivers. Each transceiver has both the physical medium attachment (PMA), protocol physical coding sub-layer (PCS) logic, and interfaces to the FPGA fabric.

The transceiver has a multi-lane architecture with each lane natively supporting serial data transmission rates from 250 Mbps to 12.7 Gbps.

At the receiver front end, CTLE (continuous time linear equalization) with optional auto calibration compensates the High Frequency losses to improve the received signal integrity. However, for lossy channels the CTLE technique amplifies the high frequency noise along with the data. This can be overcome by using Decision feedback equalization which mitigates lane noise caused due to ISI (inter symbol interference) or cross-talk without amplifying the high frequency noise within the data.

CTLE technique is sufficient to interpret data up to 8 Gbps for short reach applications. Beyond this DFE is capable of equalizing channel response.

For more information on CTLE, DFE and Transceiver insertion loss, see UG0677: PolarFire FPGA Transceiver User Guide.

An optionally enabled 5-tap decision feedback equalizer (DFE) is available to equalize the lane response in conjunction with the CTLE.

The DFE-based operation uses current bit information to cancel ISI for the following bit through a feedback mechanism, allowing the following bits to be correctly sampled. Using taps to delay and by multiplying the symbols, the DFE effectively cancels out interference on the analog signal.

The operation is nonlinear, allowing it to overcome the notch response that the CTLE does not perform. The DFE also includes an automatic calibration that finds the best possible tuning to match the transceiver lane to the system channel. DFE mode supports serial data transmission rates from 3 Gbps to 12.7 Gbps.

This demo design demonstrates the simple procedure to perform run time DFE calibration using dynamic reconfiguration interface (DRI). It also shows how to plot eye diagram using SmartDebug tool and verify signal integrity in DFE mode.

DFE equalization enables PolarFire transceivers to be efficient for systems running at approximately 10 Gbps or above where channel complexity is higher.

2.1 DFE Calibration

DFE Calibration is carried out by a robust descent algorithm which has been optimized to avoid local minima, achieve predictable results, enable low area, and operate at high clock speeds. It adjusts the feedback coefficients (H1 - H5) by trial-and-error in response to the eye-area.

The algorithm operates on one dimension (a single coefficient) at a time. It takes a step of size 1 in the positive and then the negative direction that is H1+1 and H1-1. If the area improves on either step, it continues to take another step in the same direction. If both directions yield a lower area, it continues to the next coefficient with the same step size. After failing to improve the area on all coefficients, it will increase the step size and continue. If the area is improved the step size immediately reduces to 1.
2.2 Design Requirements

The following table lists the resources required to run the demo.

Table 1 • Design Requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System</td>
<td>64-bit Windows 7, 8.1, or 10</td>
</tr>
<tr>
<td>Hardware</td>
<td></td>
</tr>
<tr>
<td>PolarFire Evaluation Kit (MPF300-EVAL-KIT)</td>
<td>Rev D or later</td>
</tr>
<tr>
<td>-PolarFire evaluation board</td>
<td></td>
</tr>
<tr>
<td>-12 V, 5 A AC power adapter and cord</td>
<td></td>
</tr>
<tr>
<td>-USB 2.0 A to mini-B cable for universal asynchronous receiver-transmitter (UART) and programming</td>
<td></td>
</tr>
<tr>
<td>2 SMA-to-SMA cables with 10 Gbps support (not provided with the kit)</td>
<td></td>
</tr>
<tr>
<td>Host PC</td>
<td></td>
</tr>
<tr>
<td>Software</td>
<td></td>
</tr>
<tr>
<td>FlashPro</td>
<td>v2.3</td>
</tr>
<tr>
<td>Libero® SoC PolarFire Design Suite</td>
<td>v2.3</td>
</tr>
</tbody>
</table>

2.3 Prerequisites

Before you start:

1. Download the demo design files from the following location:
   http://soc.microsemi.com/download/rsc/?f=mpf_ac468_liberosocopolarfirev2p3_df
2. Download and install Libero SoC PolarFire v2.3 on the host PC from the following location.
   https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polarfire#downloads
   The latest versions of ModelSim and Synplify Pro are included in the Libero SoC PolarFire installation package.
2.4 Demo Design

The following steps describe the data flow in the demo design:

1. The reference design uses a transceiver interface (PF_XCVR) configured in native PMA mode running at 10.3125 Gbps data rate, 40-bit PCS fabric interface, and using 125 MHz reference clock.
2. The PRBS_Generator module generates a PRBS-7 pattern and forwards the data to the Transceiver TX end.
3. The differential serial data of TX and RX is looped back using onboard SMA-to-SMA cables.
4. This data is then received by PRBS_checker module which checks for data match. If matched the Lock is asserted, otherwise an error signal is generated.

The above steps ensure the transceiver CDR is locked.

The following steps describe how DFE calibration is triggered.

1. Once the CDR is locked, valid RX_IDLE and RX_READY signals are sent to the Flag_for_RXPLL_lock_0 module. Note that, RX_IDLE is low during data transmission and RX_READY is asserted when CDR is locked to the incoming serial data.
2. Flag_for_RXPLL_lock_0 module determines proper transceiver RX PLL lock using the condition (NOT RX_IDLE) AND RX_READY.
3. When the above condition is true the Flag_o is asserted and sent to CoreABC module.
4. This initiates the DFE calibration sequence using CoreABC interface.
5. CoreABC acts as APB3 master and dynamically performs Read/Write to transceiver registers using PF_XCVR_DRI interface. The transceiver interface is connected as APB3 slave to the PF_XCVR_DRI interface.
6. When the DFE calibration sequence is successful, the DFE_CAL_DONE flag is asserted.

The following figure shows a block diagram of the reference design.

![DFE Block Diagram](image-url)
2.4.1 Design Implementation

The following figure shows the top-level Libero design of the PolarFire Transceiver DFE design.

**Figure 2 • Top Level Libero Design**

The following sections describe the IP cores used in the design and their configurations.

**Note:** The IP cores which are not described in the following section keep the default configuration.

### 2.4.1.1 PF_CCC_0 Configuration

The PF_CCC block provides a clock for CoreABC and Dynamic Configuration Interface. The input for the CCC is from 160 MHz on-chip RC oscillator. In this design, the clock is configured to 50 MHz.
2.4.1.2 CoreABC

The CoreABC is a programmable soft-controller targeted for implementing AMBA (Advanced Microcontroller Bus Architecture) based designs.

CoreABC in this reference design is connected to the Dynamic Reconfiguration Interface (DRI) as an APB3 master. The APB3 slave of DRI is connected to Transceiver. The CoreABC initiates the DFE calibration sequence and dynamically performs Read/Write operation on Transceiver register. Number of APB slots, APB slot size and maximum number of instructions are configured depending on the number of peripherals and address size used. The following figure shows the parameter configuration of CoreABC interface.

Figure 3 • CoreABC Configuration
2.4.1.2.1 CoreABC Program

The following figure illustrates the register settings required for performing DFE calibration.

Note: The register address changes depending on the transceiver Quad and Lanes used. In this demo Q2 Lane0 is used. For more information, see Device Register Map.

Figure 4 • CoreABC Program
2.4.1.3 Dynamic Reconfiguration Interface

DRI performs the run time configuration of transceiver PMA/PCS, PCIe, CCC, and Transmit PLLs after initialization.

In this demo design, DRI is used for performing Run-time calibration of transceiver and CCC. Q2_LANE0 is enabled to expose slave to the Transceiver interface and PLL0_NW is enabled to expose slave to the CCC interface as shown in the following figure.

*Figure 5 • PF_XCVR_DRI Configuration*
2.4.1.4 Transceiver Interface Reconfiguration

The PolarFire transceiver interface configurator is set to 10.3125 Gbps, 40-bit PCS-Fabric interface width and native PMA mode. The following figure shows the PolarFire Transceiver Interface configurator settings and how to enable dynamic reconfiguration interface (DRI).

Figure 6 • PolarFire Transceiver Reconfiguration GUI
### 2.4.1.5 PolarFire Transceiver Reference Clock

The transceiver reference clock can be configured either as a differential clock or as a two single-ended REFCLKS. This design requires a single REFCLK. The REFCLK source the transceivers, and global clock network in this design. The reference clock 0 is configured as a differential reference clock.

### 2.4.1.6 Transmit PLL

The transmit PLL reference clock and desired output clock are set to 125 MHz and 5 MHz, respectively as shown in the following figure. The PolarFire transceiver is a half-rate architecture, that is, the internal high-speed path uses both edges of the clock to keep the clock rates down. The clock thus runs at half of the data rate, thereby consuming less dynamic power.

#### Figure 7 • Transmit PLL Configurator

![Transmit PLL Configurator](image)

### 2.4.1.7 Flag_for_RXPLL_Lock

The Flag_for_RXPLL_Lock looks for signal activity on the transceiver. This is done by looking for RX_READY going HIGH and RX_IDLE going LOW (RX_READY &! RX_IDLE). The flag output is used as an input to the CoreABC to start DFE.

### 2.4.1.8 PRBS Generator and Checker

The generator implements the PRBS polynomial and generates a continuous sequence of PRBS7 patterns of 40 bits each. The PRBS checker receives data from transceiver to generate PRBS data locally, the two are then compared for data integrity. A lock signal is asserted if there is data match otherwise an error signal is asserted to the user.

### 2.5 Port Description

The following table lists the key signals for this design.

#### Table 2 • Port Description

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF_CLK_PAD_P and</td>
<td>Input</td>
<td>Differential reference clock is generated from the on-board</td>
</tr>
<tr>
<td>REF_CLK_PAD_N</td>
<td></td>
<td>125 MHz oscillator</td>
</tr>
<tr>
<td>LANE0_RXD_N</td>
<td>Input</td>
<td>Transceiver receiver differential input.</td>
</tr>
<tr>
<td>LANE0_RXD_P</td>
<td>Input</td>
<td>Transceiver receiver differential input.</td>
</tr>
<tr>
<td>SWITCH</td>
<td>Input</td>
<td>DIP switch setting to initiate DFE calibration. Trigger for</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DFE calibration can also be generated by user design using</td>
</tr>
<tr>
<td></td>
<td></td>
<td>the condition (RX_READY &amp;! RX_IDLE).</td>
</tr>
</tbody>
</table>
### Table 2 • Port Description

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LANE0_TXD_N</td>
<td>Output</td>
<td>Transceiver transmitter differential output.</td>
</tr>
<tr>
<td>LANE0_TXD_P</td>
<td>Output</td>
<td>Error flag generated from PRBS checker module when there is data mismatch</td>
</tr>
<tr>
<td>error_out</td>
<td>Output</td>
<td>Dynamic CCC OUT3 Fabric Clock</td>
</tr>
<tr>
<td>Lock</td>
<td>Output</td>
<td>Lock signal flag generated from PRBS checker module when there is data match</td>
</tr>
</tbody>
</table>


2.6 Clocking Structure

In this reference design, there are two clock-domains. The on-board 125 MHz crystal oscillator drives the XCVR reference clock. The XCVR REFCLK source the transceivers, and global clock network in this design. The on-chip 160 MHz RC oscillator drives the CoreABC, Flag_for_RXPLL_lock, and PF_XCVR_DRI block. The following figure shows the clocking structure in this reference design.

*Figure 8* • Clocking Structure
2.7 Reset Structure

In this reference design, the reset signal of PRBS generator and PRBS checker, are issued using Reset_logic module. Reset_sync_tx_0 (CoreReset_PF) module releases active low reset of data generator block when TX_CLK_STABLE from PF_XCVR interface and DEVICE_INIT_DONE signal from PF_INIT_MONITOR block are asserted.

Similarly, Reset_sync_rx_0 (CoreReset_PF) module releases active low reset of data checker when RX_READY from PF_XCVR interface, DEVICE_INIT_DONE signal from PF_INIT_MONITOR block are asserted.

The previous setup ensures that the PRBS generation and PRBS checker does not start until the TX_clock_stable and RX_READY are asserted respectively.

DEVICE_INIT_DONE signal is asserted when the device initialization is complete. For more information about device initialization, see UG0725: PolarFire FPGA Device Power-Up and Resets User Guide.

For more information on CoreReset_PF IP core, see CoreReset_PF handbook from the Libero catalog.

The following figure shows the reset structure in this reference design.

\textit{Figure 9 • Reset Structure}
The Libero design flow involves running the following processes in the Libero SoC PolarFire:

- Synthesize, page 15
- Resource Utilization, page 15
- Place and Route, page 15
- Verify Timing, page 16
- Design and Memory Initialization, page 16
- Generate Bitstream, page 16
- Run PROGRAM Action, page 17

The following figure shows these options in the Design Flow tab.

*Figure 10 • Libero Design Flow Options*
3.1 Synthesize

To synthesize the design:

1. Double-click Synthesize from the Design Flow tab. When the synthesis is successful, a green tick mark appears as shown in Figure 10, page 14.

2. Right-click Synthesize and select View Report to view the synthesis report and log files in the Reports tab.

3.2 Resource Utilization

The following table lists the resource utilization of the DFE design after synthesis.

Note: These values may vary slightly for different Libero runs, settings, and seed values.

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>992</td>
<td>299544</td>
<td>0.33</td>
</tr>
<tr>
<td>DFF</td>
<td>598</td>
<td>299544</td>
<td>0.20</td>
</tr>
<tr>
<td>Transceiver lanes</td>
<td>1</td>
<td>16</td>
<td>6.25</td>
</tr>
<tr>
<td>TX_PLL</td>
<td>1</td>
<td>11</td>
<td>9.09</td>
</tr>
<tr>
<td>XCVR_REF_CLK</td>
<td>1</td>
<td>11</td>
<td>9.09</td>
</tr>
</tbody>
</table>

3.3 Place and Route

For DFE design, the TX_PLL, XCVR_REF_CLK, and XCVR need to be constrained using the I/O Editor as shown in the following figure.

Figure 11 • I/O Editor-Transceiver View
3.4 Verify Timing

To verify timing:

1. Double-click Verify Timing from the Design Flow tab. When the design successfully meets the timing requirements, a green tick mark appears as shown in Figure 10, page 14.

2. Right-click Verify Timing and select View Report, to view the verify timing report and log files in the Reports tab.

3.5 Design and Memory Initialization

This option is used to create the XCVR initialization client, which is used in the demo design. When the PolarFire device powers up, the transceiver block is initialized by the initialization client generated during the Configure Design Initialization Data and Memories stage in the design flow. For more information about device power-up, see UG0725: PolarFire FPGA Device Power-up and Resets User Guide.

3.6 Generate Bitstream

To generate the bitstream:

1. Right-click Generate Bitstream and select Configure Options... to select the bitstream components—Custom security, Fabric, and sNVM.

2. Double-click Generate Bitstream from the Design Flow tab. When the bitstream is successfully generated, a green tick mark appears as shown in Figure 10, page 14.

Right-click Generate Bitstream and select View Report to view the corresponding log file in the Reports tab.
3.7 Run PROGRAM Action

After generating the bitstream, the PolarFire device must be programmed with the system services design.

Follow these steps to program the PolarFire device:
1. Ensure that the following jumper settings are set on the board.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J18, J19, J20, J21, J22</td>
<td>Short pin 2 and 3 for programming the PolarFire FPGA through FTDI</td>
</tr>
<tr>
<td>J28</td>
<td>Short pin 2 and 3 for programming through the onboard FlashPro5</td>
</tr>
<tr>
<td>J26</td>
<td>Short pin 1 and 2 for programming through the FTDI SPI</td>
</tr>
<tr>
<td>J27</td>
<td>Short pin 1 and 2 for programming through the FTDI SPI</td>
</tr>
<tr>
<td>J4</td>
<td>Short pin 1 and 2 for manual power switching using SW3</td>
</tr>
<tr>
<td>J12</td>
<td>Short pin 3 and 4 for 2.5 V</td>
</tr>
<tr>
<td>J46</td>
<td>Short pin 1 and 2 for routing 125 MHz differential clock oscillator output to the line side. Open pin 1 and 2 for routing 122.88 MHz differential clock oscillator output to the line side.</td>
</tr>
</tbody>
</table>

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the host PC to the J5 (FTDI port) on the board.
4. Power on the board using the SW3 slide switch.
5. Connect TXN to RXN and TXP to RXP using the 2 SMA to SMA cables as shown in the following figure. The following figure shows the board setup.

The following figure shows the board setup after these connections are made.

Figure 14 • Board Setup


The device is successfully programmed and the onboard LEDs 4, 5, 6 and 7 glow. A green tick mark appears next to Run PROGRAM Action as shown in Figure 10, page 14.

Figure 15 • Programming the Device
4 Programming the Device Using FlashPro

This section describes how to program the PolarFire device with the .stp programming file using FlashPro. The .stp file is available at the following design files folder location:

```
mpf_ac468_liberosocpolarfirev2p3_df\PF_XCVR_DFE\Programming_File
```

Follow these steps to program the device:

1. Connect the jumpers and set up the PolarFire Evaluation Kit board according to Table 4, page 17.
2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the Host PC to J5 (FTDI port) on the board.
4. Power on the board using the SW3 slide switch.
5. Connect TXN to RXN and TXP to RXP using the two SMA to SMA cables as shown in the following figure. The following figure shows the board setup.

![Programming the Device with FlashPro](image)

6. Download the demo design from:
   
   `http://soc.microsemi.com/download/rsc/?f=mpf_ac468_liberosocpolarfirev2p3_df`

7. On the host PC, start the FlashPro software.
8. Click **New Project** to create a new project. In the New Project window, enter project name.
9. Click **Browse** and navigate to the location where you want to save the project.
10. Select Single device as the programming mode and click **OK** to save the project.
11. Click **Configure Device**.
12. Click **Browse**, and navigate to the location where the `PF_XCVR_DFE.stp`
13. Click **Program** to program the device. The Programmer List Window in the FlashPro, shows the Programmer Name, Programmer Type, Port, Programmer Status, and the Programmer Enabled information.
The device is successfully programmed and the onboard LEDs 4, 5, 6, and 7 glow. The **RUN PASSED** message is displayed as shown in the following figure.

*Figure 17 • Programming the Device with FlashPro5*
Running the Demo

This section describes how to optimize DFE coefficients, and check the result on board.

Prerequisites for the procedure:

- The PolarFire Evaluation board is connected.
- The PolarFire FPGA is programmed with the DFE design.

To run the demo, perform the following steps:

1. After the device is programmed, change SW11 DIP1 from 0 to 1. This brings CoreABC interface out of reset and starts DFE calibration.

   **Note:** SW11 DIP1 is used for demo. Trigger for DFE calibration can also be generated by monitoring the condition (RX_READY &! RX_IDLE)

2. Observe if LED4 is OFF, and LED10 and LED5 are ON. This signifies that run time DFE calibration is complete and there is no bit error. Where LED4 and LED10 represent bit error status and LED5 represents DFE calibration status.

The following figure shows the eye plot obtained using SmartDebug tool in DFE mode. For more information about how to use SmartDebug, see [TU0804: PolarFire FPGA SmartDebug Hardware Design Tools Tutorial](#).

**Figure 18 • Eye Plot**
6 Appendix- Optimize DFE Coefficients Using Smart Debug

6.1 Optimize DFE Coefficients Using SmartDebug

DEF optimization can also be done using Smart debug. After the optimization is complete, the transceiver lanes are programmed with these coefficients for the user to continue debugging.

**Note:** Optimize DFE Coefficients is only supported for data rates ≥ 5Gbps.

For information about how to use the optimized coefficients without SmartDebug, see the UG0677: PolarFire FPGA Transceiver User Guide.

**Figure 19 • Debug TRANSCEIVER - Optimize DFE**

Click **Optimize DFE**, this opens a Optimize DFE dialog box. Select the **Lane0** and click **Optimize DFE on Selected Lane** as shown in the following figure.

**Figure 20 • Optimize DFE Dialog**